CLAIMS

WHAT IS CLAIMED IS:

1. A memory module, comprising:

a printed circuit board;

a plurality of memory devices coupled to the printed circuit board; and

a processing device coupled to the printed circuit board and connected to the plurality of memory devices,

wherein, when the memory module is powered-up, the processing device performs first memory training on the plurality of memory devices, generates a module ready signal after completing the first memory training, and transmits the module ready signal to a host device that is outside of the memory module, and

the module ready signal causes the host device to perform second memory training on the plurality of memory devices.

2. The memory module as claimed in claim 1, wherein the module ready signal is output to the outside of the memory module through unused pins among connecting pins of the memory module.

3. The memory module as claimed in claim 1, wherein the module ready signal is output to the outside of the memory module through a pin dedicated to the module ready signal among connecting pins of the memory module.

4. The memory module as claimed in any one of claims 1 to 3, wherein:

the processing device includes a memory controller that controls the first memory training for the plurality of memory devices, and

the memory controller performs the first memory training using a training circuitry and generates the module ready signal.

5. The memory module as claimed in any one of claims 1 to 4, wherein the memory module is a dual in-line memory module.

6. A computing system, comprising:

a board;

a host device mounted on the board;

a memory module mounted on the board and connected to the host device, the memory module including a plurality of memory devices and a processing device connected to the plurality of memory devices; and

a basic input/output system (BIOS) memory configured to store BIOS code for booting the computing system,

wherein, when the computing system is powered up, the processing device of the memory module performs first memory training on the plurality of memory devices, generates a module ready signal after completing the first memory training, and transmits the module ready signal to the host device, and

when the host device receives the module ready signal, the host device performs second memory training on the plurality of memory devices.

7. The computing system as claimed in claim 6, wherein the memory module outputs the module ready signal to outside of the memory module through an unused pin among connecting pins of the memory module.

8. The computing system as claimed in claim 6, wherein the memory module outputs the module ready signal to outside of the memory module through a pin dedicated to the module ready signal among connecting pins of the memory module.

9. The computing system as claimed in any one of claims 6 to 8, wherein the module ready signal is transmitted to the host device through an interrupt signal line formed on the board.

10. The computing system as claimed in any one of claims 6 to 8, wherein the module ready signal is transmitted to the host device through a module ready signal line formed on the board.