

ABSTRACT

Techniques and mechanisms for providing at a packaged device an integrated circuit (IC) chip and a chiplet, wherein memory resources of the chiplet are accessible by a processor core of the IC chip. In an embodiment, a hardware interface of the packaged device includes first conductive contacts at a side of the chiplet, wherein second conductive contacts of the hardware interface are electrically interconnected to the IC chip each via a respective path which is independent of the chiplet. In another embodiment, one or more of the first conductive contacts are configured to deliver power, or communicate a signal, to a device layer of one of the IC chip or the chiplet.

Fig. 1A