Method for Bonding of Chips on Wafers

Specification

The invention relates to a method for bonding of chips on wafers.

As a result of the miniaturization pressure which is prevailing in the semiconductor industry, methods are needed with which so-called "3D Integrated Chips" (3D IC) can be produced. 3D ICs consist of chip stacks in which several chips are stacked vertically on top of one another and there are connections through the silicon to the vertically adjacent chips. The connections are called "Through Silicon Vias" (TSV).

These chips promise high packing density and higher performance at lower costs. Moreover, in this way new types and forms of chips can be produced. Fundamentally different methods are possible for producing 3D ICs, specifically the very time-consuming stacking of individual chips on individual chips, also called "Chip-to-Chip" (C2C) methods, or stacking of wafers on wafers, also called "Wafer to Wafer" (W2W) methods. Finally, the so-called "Chip to Wafer (C2W)" method is also discussed. A reasonable technical implementation has not been successful to date due to major technical problems. Embodiments of this invention relate to a technically feasible C2W method for producing 3D ICs.

Due to low throughput, C2C methods cause higher production costs and therefore may hardly be used in mass production.

W2W methods require that the two wafers have the same size and that the chips on the two

wafers have the same size. The problem here is that the silicon utilization especially for higher chip stacks is below average (so-called yield). The attainable yield of functioning chips is lower than in C2C or C2W methods.

Technical problems in the implementation of a C2W method for producing chips stacks or 3D ICs are the handling of the wafers, especially with the chips stacked on them, and the varied requirements, especially temperatures, for the stacking process and for the connectors (interfaces) of the chips for mounting on circuit boards or fundamentally the higher-order packing unit.

Handling of the base wafer therefore acquires great importance because fracture of the base wafer shortly before separation of a plurality of chip stacks on the wafer would lead to scrapping of thousands of expensive chips. Handling of the base wafer with a plurality of chip stacks fixed/bonded thereon becomes more difficult, the thinner and/or greater the area of the base wafer. The base wafer is the wafer on which the chips are stacked in the C2W method.

US 2007/001281 A1 relates to a method for producing a semiconductor memory in which chips are stacked on the base wafer and then potted in resin to simplify production logistics in the production of memory chips. After potting, the memory chips are separated from their adjacent memory chips. In particular, different thermal expansions of the different materials of the diverse components present in the chip stacks are a problem during production, mainly when potting the memory chips and in the release from the carrier, and possible subsequent process steps.

Embodiments of the invention disclose a method as free of scrap as possible for producing chip stacks (3D ICs) which are positioned as exactly as possible, with a throughput as high as possible.

According to an aspect, there is provided a method for bonding a plurality of chips onto a base wafer, the chips being arranged on the base wafer in at least one layer, wherein electrically conductive connections are established for connecting vertically adjacent chips, said method comprising: a) fixing the base wafer on a carrier, b) placing the chips being arranged in at least one layer, in defined positions on the base wafer, and c) heat treating the chips on the base wafer fixed on the carrier, wherein prior to step c) a separation of the base wafer into separated chip stack sections of the base wafer takes place.

All combinations of at least two of the features given in the specification, in the claims and/or the drawings lie within the framework of the invention. For the given value ranges values within the indicated limits will also be considered disclosed as boundary values and can be claimed in any combination.

Embodiments of the invention are based on the idea of fixing the base wafer at least during the stacking of chips on the base wafer, and during the heat treatment of the chips for bonding, fixing the wafer on a carrier or connecting it to the carrier, and of at least partially separating the base wafer at latest before heat treatment, especially into chip stack sections which have preferably been separated from one another.

By fixing the base wafer on the carrier it is possible with a surprising advantage for the throughput of the C2W method to separate the process steps of stacking or placing the chips in defined positions on the base wafer and the process step(s) of heat treatment or bonding of the chips on the base wafer. While heat treatment or the bonding step, depending on the material used, can take a very long time, the positioning or stacking and placement of the chips on the base wafer is a process step which can proceed very promptly, for example with several thousand chips per hour. When the base wafer is moreover present separated into smaller parts during heat treatment, thermal expansion of the different components/materials has a much smaller effect on the quality of the chip stacks. As a result of separation, the chips stacks are less stressed by the different expansions.

In this way, the throughput can be increased by there being several heat treatment chambers/bonding stations and/or by several base wafers with stacked chips being processed in a heat treatment chamber/bonding station. Heat treatment chambers can be hot plates, continuous

the chips it is watched that chips are placed only on functioning chips of the underlying layer of chips. Even more preferably the function of all chips which are functionally joined to the chip to be placed is checked and a chip is placed only with the function of all chips which are to be functionally joined to the chip.

In heat treatment or the bonding step electrically conductive connections are produced between the wafer and the chip which has been placed on it or between the placed chips. Here it is advantageous if heating takes place in a suitable atmosphere which is preferably free of oxygen, so that oxidation of the metal contact surfaces is avoided. In particular this can be achieved by the use of a nitrogen atmosphere or another inert atmosphere, for example argon, for many applications not only an inert, but also a reducing atmosphere being especially advantageous. This property can be achieved for example by forming gas or formic acid vapor. Forming gas can be formed by mixing H2 with N2, especially between 2% H2 to 98% H2 and 15% H2 to 85% N2. In this mixture N2 can also be replaced by other inert gases.

So that the chips can be handled better and do not slide after they are placed, it is advantageous to pre-fix the chips after placement, especially to adhere them, preferably with an organic adhesive which vaporizes during the following bonding step. Alternatively the chips can be fixed by a molecular connection which advantageously forms spontaneously at room temperature, for example between the Si surfaces, SiO2 surfaces or SiN surfaces. Another alternative is ultrasonic welding.

Advantageously heat treatment takes place especially continuously, at a temperature $< 280^{\circ}C$, especially $< 250^{\circ}C$, preferably $< 220^{\circ}C$. The adhesives used as per embodiments the invention must be suitable for the aforementioned temperatures, these adhesives only recently being available

at all. An example of these adhesives is the HAT series from Brewer-Science Inc., USA.

The base wafer in one embodiment of the invention, especially by back grinding, has a thickness of less than 200 μm, especially less than 100 μm, preferably less than 50 μm, still more preferably less than 20 μm.

Especially many chips can be accommodated on a base wafer with a diameter of at least 200 mm, especially at least 300 mm, preferably at least 450 mm.

In one embodiment of the invention it is possible to apply solder bumps or C4 bumps after step b or c for connecting each chip stack to a board or fundamentally the next higher-order packing unit.

The solder bumps consist of a metal alloy with a low melting point and are generally used to connect the chips/chip stacks to other electrical/electronic components.

In particular, when using a base wafer with electrically conductive connections which penetrate the base wafer (TSVs) it is advantageous to pot the chips or chip stacks after step b or c in a mass which is characterized especially by high thermal and/or mechanical stability and/or water-repellent properties, especially a mass of organic and/or of ceramic material. An embodiment is especially preferred in which at least in part epoxy resin is contained in the mass or the mass is formed entirely from epoxy resin. The epoxy resin-containing mass can be fiber-reinforced in one embodiment of the invention.

Advantageously the mass is poured in liquid form at room temperature or at a higher temperature.

In one advantageous embodiment of the invention, the mass is pressurized after potting, especially by relief to atmospheric pressure after carrying out the potting below atmospheric

Claims:

1. Method for bonding a plurality of chips (9) onto a base wafer (1), the chips (9) being arranged on the base wafer (1) in at least one layer, wherein electrically conductive connections (7) are established for connecting vertically adjacent chips, said method comprising:

a) fixing the base wafer (1) on a carrier (5),

b) placing the chips (9) being arranged in at least one layer, in defined positions on the base wafer (1), and

c) heat treating the chips (9) on the base wafer (1) fixed on the carrier (5),

wherein prior to step c) a separation of the base wafer (1) into separated chip stack sections of the base wafer (1) takes place.

2. Method as claimed in claim 1, wherein said steps b) and c) are carried out in different devices.

3. Method as claimed in claim 1 or 2, wherein fixing means are used for fixing.

4. Method as claimed in any one of claims 1 to 3, wherein, during the placement of the chips (9) in the defined positions, an electrically conductive laminae (3) applied to the chips (9) are aligned and contacting to a corresponding electrically conductive laminae (8) for connection to an underlying layer of the chips.

5. Method as claimed in any one of claims 1 to 4, said chips (9) are adhered with an organic adhesive or fixed by molecular connection, after said placing.

6. Method as claimed in any one of claims 1 to 5, wherein said step of the heat treating takes place at a temperature <280° C.

7. Method as claimed in any one of claims 1 to 6, wherein the chips (9) or chip stacks (16) after steps b) or c) is potted in a mass which is characterized by high thermal and/or mechanical and/or chemical stability and/or water-repellent properties, of organic material or ceramic material.

8. Method as claimed in claim 7, wherein the base wafer (1) is removed from the carrier (5) after potting.

9. Method as claimed in claim 7 or 8, wherein the base wafer (1) with the mass (11) and the chips (9) potted in the mass (11) after potting or during potting is brought into basic form corresponding to the base wafer (1) and/or the mass (11) is removed as far as an uppermost layer of the chips (9).

10. Method as claimed in any one of claims 1 to 9, wherein after step b) or c), solder bumps (12) are applied for connection of each chip stack (16) to a board or another chip (9).

11. Method as claimed in any one of claims 1 to 10, wherein the base wafer (1) and/or the carrier (5) consist at least predominantly of silicon.

12. Method as claimed in any one of claims 1 to 11, wherein at least two layers of the chips (9) are applied to the base wafer (1).

13. Method as claimed in any one of claims 1 to 12, wherein the base wafer (1) with the chips (9) stacked on it is fixed on a dicing frame (13) before the chip stack (16) is separated from adjacent chip stacks (16).

14. Method as claimed in any one of claims 1 to 13, wherein the base wafer (1) is separated during back-grinding.