

write parameters to account for physical degradation of the cells of the device. Write parameters can include, for example write voltages, such as the voltages applied to memory cells through word lines and/or the bit lines during a write operation. Other internal parameters can be adjusted as well. Example parameters include, but are not limited to pulse shape, leading edge, trailing edge, duration, etc. In general, write parameters may include any configurable settings in the memory device that can be adjusted as the cell ages in order to improve the probability of a successful write operation. Disclosed herein are various apparatuses and methods for tracking the age of a device based on the number of write operations performed on the device, and adjusting write parameters based on the age of the device and a set of bins defined by ranges of write operations. Bins are specified ranges of the numbers of write operations. At any given point in time, the device may fit into one or more bins based on the number of write operations that have been performed on the memory device. For example, one bin may be defined by a range of between 0 and 1,000 write operations. Write operations may include programming operations, erase operations, or both.

[15] Fig. 1A is a functional block diagram of a memory system, generally designated 100, in accordance with an embodiment of the present invention. Memory system 100 includes a processor 102 coupled to a memory device 104. The processor 102 can be any type of controlling circuitry configured to transmit instructions to the memory device 104. In various embodiments, the processor may be one or more microprocessors, an application specific integrated circuit, or other type of controlling circuitry. The memory device 104 includes various circuits for memory operations. As discussed in further detail below with respect to Fig. 1B, the memory device 104 can include input/output (I/O) control circuitry, control logic, and a memory array comprising a plurality of memory cells. Commands, address information, and write data may be provided to the memory device 104 as sets of sequential input/output (I/O) transmitted through an I/O bus 128. Similarly, read data may be provided from the memory device 104 through the I/O bus 128.

[16] The processor 102 may be further coupled to a write count circuit 106. The write count circuit 106 may be a register, a cache, or any other type of temporary memory configured to store a number of write operations executed by the memory

processor 102 to transmit the current write count value to the control logic 110 during the set write cycle bin operation.

[25] In operation 304, the control logic 110 determines the applicable write cycle bin based on the parameter table 162 and the current write count value, as received in operation 302. As described above, the parameter table 162 generally defines a number of write cycle bins based on the number of write operations that have been performed by the memory array 160. The control logic 110 compares the current write count (as stored in the write count circuit 106 and received in operation 302) with the write cycle bins in the parameter table 162 to determine into which bin or bins the current write count falls. For example, the current write count may be 10,560 write operations. The parameter table 162 may include a first bin having a range of 0 to 10,000 write operations and a second bin having a range of 1,000 to 100,000 write operations. In such an embodiment, the control logic 110 determines that the current write count (10,560) is between 1,000 and 100,000, but not between 0 and 10,000. Therefore, the control logic 110 determines that the second bin is an applicable bin and the first bin is not an applicable bin.

[26] Referring now to Fig. 4, an example parameter table 400 is shown, in accordance with an embodiment of the present invention. In various embodiments, the parameter table 400 may be implemented as the parameter table 162 in the embodiment of Fig. 1. The parameter table 400 generally includes a plurality of bins 402, a maximum (max) write count 404, and a minimum (min) write count 406. In the embodiment of Fig. 4, the parameter table 400 has four bins: bins 0, 1, 2, and 3. Each of the bins 0, 1, 2, and 3 has an associated max write count 404 and min write count 406. The max write count 404 and min write count 406 define the size of each bin (i.e., the range over which each bin applies to the write count). For example, bin 0 has a min write count 404 of 0 write operations (i.e., a memory array that has never been written) and a max write count 406 of 10,000 write operations. Accordingly, if the control logic 110 determines in operation 304 that the write count has a value of between 0 and 10,000, then the control logic 110 identifies bin 0 as the applicable bin. Although four bins are shown in Fig. 4, those skilled in the art will appreciate that any number of bins may be used.