

Description

This invention relates generally to charge pump circuitry for generating positive and negative voltage potentials using a single supply voltage source, and more particularly the invention is directed to a charge pump integrated circuit.

The technique of doubling a voltage from a supply voltage source by switchably charging a capacitor and altering the capacitor terminals with respect to the voltage source is well known. Such a charge pump enables flexibility in circuit operation by providing a plurality of voltage potentials to circuit elements.

For example, the product designated ICL7660, manufactured by Maxim Integrated Products, Inc., of Sunnyvale, California, is a charge pump circuit operative in an inverting mode to produce voltage polarities opposite to that of the supply voltage from which they are generated. As a further example, a charge pump power supply disposed to operate in both inverting and non-inverting modes is described in U.S. Patent 4,636,930. This dual-mode charge pump circuit is designed to convert a unipolar supply voltage to a bipolar supply voltage of greater magnitude.

The present invention is directed to an integrated circuit functioning with discrete capacitors as a charge pump in doubling a voltage from a voltage source and providing both positive and negative voltages therefrom. A preferred feature of the invention is the use of a transistor switch having a low saturation voltage. Another preferred feature of the invention is a switch that is current-limited and thus limits the supply current when charging a capacitor.

The invention provides that within a charge pump circuit having a supply terminal for connecting to a voltage source, V_{cc} , a ground terminal for connecting to a ground potential, a first capacitor serially connected with first and second switch means between said supply terminal and said ground terminal, a third switch means connected in parallel with said first switch means and said first capacitor, a second capacitor serially connected with fourth and fifth switch means between the common terminal of said first switch means and said first capacitor and said ground terminal, a third capacitor serially connected between a positive voltage ($+2V_{cc}$) terminal and said ground terminal, a fourth capacitor serially connected with a sixth switch means between said ground potential and the common terminal of said second capacitor and said fifth switch means, the common terminal of said fourth capacitor and said sixth switch means connected to a negative voltage ($-2V_{cc}$) terminal, and a seventh switch means connected in parallel with said second capacitor and said fifth switch

means, whereby closure of said first and second switch means during a first operational phase generates a voltage V_{cc} across said first capacitor, characterised by an eighth switch means connected between said positive voltage ($+2V_{cc}$) terminal and the common terminal of said first switch means and said first capacitor, whereby closure of said third, fourth, fifth and eighth switch means during a second operational phase transfers a voltage $+2V_{cc}$ to said second and third capacitors, and during a subsequent first operational phase closure of said sixth and seventh switch means induces a voltage $-2V_{cc}$ to be transferred to said fourth capacitor.

The invention also provides a method of operating the charge pump circuit wherein said third switch means comprises a dual-emitter bipolar transistor, a method of limiting source current comprising the steps of providing bias circuitry for said bipolar transistor switch with the base bias for said bipolar transistor switch being derived from said second capacitor ($2V_{cc}$), and a collector voltage derived from said voltage source (V_{cc}), thereby operating said bipolar transistor with low saturation voltage, and

connecting one emitter of said dual-emitter bipolar transistor switch to said bias circuitry whereby operation of said transistor is current-limited.

The invention and objects of features thereof will be more readily apparent from the following detailed description of an example taken with the drawings, in which:

Figs. 1A and 1B are schematics illustrating operation of a charge pump integrated circuit embodying the invention.

Fig. 2 is a schematic of one embodiment of a charge pump integrated circuit in accordance with the invention.

Referring now to the drawings, Figs. 1A and 1B illustrate operation of a charge pump integrated circuit in accordance with the invention. The circuit has two-phase operation in charging a capacitor and then transferring charge from the capacitor to generate positive and negative voltage potentials from a single voltage source. The circuit comprises a terminal connected to a voltage source, V_{cc} , and a terminal connected to a circuit ground potential. Four discrete capacitors C1-C4 are interconnected between the supply voltage V_{cc} and the ground potential by eight switches S1-S8 that are selectively closed in response to the two-phase clock 10.

During phase ϕ_1 , as illustrated in Fig. 1A, switches S1 and S2 serially interconnect capacitor C1 between the supply voltage V_{cc} and circuit ground, thereby developing a voltage potential across capacitor C1 of V_{cc} . Switch S7 connects one terminal of capacitor C2 to ground, and switch S8

connects the other terminal of capacitor C2 to a -V terminal, at which a voltage of $-2V_{cc}$ will be generated.

During Phase ϕ_2 , as illustrated in Fig. 1B, switches S1, S2, S7 and S8 are opened, and switch S3 connects the source voltage V_{cc} to the negative terminal of capacitor C1. The positive terminal of capacitor C1 is interconnected through switch S4 to a +V terminal and charges capacitor C3 to a voltage potential of twice the supply voltage or $2V_{cc}$. The doubled supply voltage, $2V_{cc}$, is applied also through switch S5 to a terminal of capacitor C2, the other terminal of which is interconnected to ground through switch S6. Thus, a voltage potential of $2V_{cc}$ is stored on capacitor C2 and capacitor C3.

On the following Phase ϕ_1 of the clock, the positive terminal of capacitor C2 is tied to ground through switch S7, thereby causing the doubled voltage stored on capacitor C2 to appear on the negative terminal of capacitor C2. The doubled negative voltage is then stored in capacitor C4 through switch S8. Thus, a V+ voltage of $2V_{cc}$ and a V- voltage of $-2V_{cc}$ are provided across capacitors C3 and C4, respectively.

In designing the circuitry of Figs. 1A and 1B (less capacitors C1-C4) in integrated circuit form, it is important to have a switch S3 transistor with a low saturation voltage and which is current-limited in operation. This is achieved in the circuitry of Fig. 2 which corresponds to the circuitry of Figs. 1A and 1B. In this circuit, a Schottky diode D1 functions as switch S1, transistor Q4 functions as switch S2, a dual-emitter transistor Q1 functions as switch S3, a Schottky diode D2 functions as switch S4, a transistor Q5 functions as switch S5, Schottky diode D3 functions as switch S6, transistor Q6 functions as switch S7 and Schottky diode D4 functions as switch S8.

In this embodiment, the dual-emitter transistor Q1 is an NPN transistor; a PNP transistor could be employed but would be larger in size. In order for an NPN transistor to have a low saturation voltage, the base of the transistor must be driven by a voltage that is greater than the collector voltage. This is accomplished in Fig. 2 with the base drive circuitry comprising transistors Q2 and Q3 which are interconnected to the self-generated V+ supply ($2V_{cc}$), thus providing transistor Q1 with a base voltage greater than the collector voltage (V_{cc}). Accordingly, the dual-emitter transistor Q1 will function with low saturation voltage.

Due to the nature of the circuit design, the current drawn from the V+ potential will be one-half of the supply current from V_{cc} . Thus, in order to keep the supply current at its lowest, the transistor Q1 must be current-limited. This is accomplished by connecting one emitter of transistor Q1

to the base drive circuitry comprising transistors Q2 and Q3. Thus, when transistor Q1 saturates, the second emitter acts as a collector and limits the base drive, thereby causing current-limiting.

Charge pump circuitry in accordance with the invention has proved to be particularly advantageous in an integrated circuit. As described, the circuit functions with low saturation voltage and is current-limited, thereby limiting the supply current.

Claims

1. In a charge pump circuit comprising a supply terminal for connecting to a voltage source, V_{cc} , a ground terminal for connecting to a ground potential, a first capacitor (C1) serially connected with first and second switch means (S1,S2) between said supply terminal and said ground terminal, a third switch means (S3) connected in parallel with said first switch means (S1) and said first capacitor (C1), a second capacitor (C2) serially connected with fourth and fifth switch means (S5,S6) between the common terminal of said first switch means (S1) and said first capacitor (C1) and said ground terminal, a third capacitor (C3) serially connected between a positive voltage ($+2V_{cc}$) terminal and said ground terminal, a fourth capacitor (C4) serially connected with a sixth switch means (S8) between said ground potential and the common terminal of said second capacitor (C2) and said fifth switch means (S6), the common terminal of said fourth capacitor (C4) and said sixth switch means (S8) connected to a negative voltage ($-2V_{cc}$) terminal, and a seventh switch means (S7) connected in parallel with said second capacitor (C2) and said fifth switch means (S6), whereby closure of said first and second switch means (S1,S2) during a first operational phase generates a voltage V_{cc} across said first capacitor (C1), characterised by

an eighth switch means (S4) connected between said positive voltage ($+2V_{cc}$) terminal and the common terminal of said first switch means (S1) and said first capacitor (C1), whereby closure of said third, fourth, fifth and eighth switch means (S3,S5,S6,S4) during a second operational phase transfers a voltage $+2V_{cc}$ to said second and third capacitors (C2,C3), and during a subsequent first operational phase closure of said sixth and seventh switch means (S8,S7) induces a voltage $-2V_{cc}$ to be transferred to said fourth capacitor (C4).

2. The charge pump circuit as defined by claim 1 wherein said third switch means comprises a bipolar transistor (Q1), and further including



connects the other terminal of capacitor C2 to a -V terminal, at which a voltage of $-2V_{cc}$ will be generated.

During Phase ϕ_2 , as illustrated in Fig. 1B, switches S1, S2, S7 and S8 are opened, and switch S3 connects the source voltage V_{cc} to the negative terminal of capacitor C1. The positive terminal of capacitor C1 is interconnected through switch S4 to a +V terminal and charges capacitor C3 to a voltage potential of twice the supply voltage or $2V_{cc}$. The doubled supply voltage, $2V_{cc}$, is applied also through switch S5 to a terminal of capacitor C2, the other terminal of which is interconnected to ground through switch S6. Thus, a voltage potential of $2V_{cc}$ is stored on capacitor C2 and capacitor C3.

On the following Phase ϕ_1 of the clock, the positive terminal of capacitor C2 is tied to ground through switch S7, thereby causing the doubled voltage stored on capacitor C2 to appear on the negative terminal of capacitor C2. The doubled negative voltage is then stored in capacitor C4 through switch S8. Thus, a V+ voltage of $2V_{cc}$ and a V- voltage of $-2V_{cc}$ are provided across capacitors C3 and C4, respectively.

In designing the circuitry of Figs. 1A and 1B (less capacitors C1-C4) in integrated circuit form, it is important to have a switch S3 transistor with a low saturation voltage and which is current-limited in operation. This is achieved in the circuitry of Fig. 2 which corresponds to the circuitry of Figs. 1A and 1B. In this circuit, a Schottky diode D1 functions as switch S1, transistor Q4 functions as switch S2, a dual-emitter transistor Q1 functions as switch S3, a Schottky diode D2 functions as switch S4, a transistor Q5 functions as switch S5, Schottky diode D3 functions as switch S6, transistor Q6 functions as switch S7 and Schottky diode D4 functions as switch S8.

In this embodiment, the dual-emitter transistor Q1 is an NPN transistor; a PNP transistor could be employed but would be larger in size. In order for an NPN transistor to have a low saturation voltage, the base of the transistor must be driven by a voltage that is greater than the collector voltage. This is accomplished in Fig. 2 with the base drive circuitry comprising transistors Q2 and Q3 which are interconnected to the self-generated V+ supply ($2V_{cc}$), thus providing transistor Q1 with a base voltage greater than the collector voltage (V_{cc}). Accordingly, the dual-emitter transistor Q1 will function with low saturation voltage.

Due to the nature of the circuit design, the current drawn from the V+ potential will be one-half of the supply current from V_{cc} . Thus, in order to keep the supply current at its lowest, the transistor Q1 must be current-limited. This is accomplished by connecting one emitter of transistor Q1

to the base drive circuitry comprising transistors Q2 and Q3. Thus, when transistor Q1 saturates, the second emitter acts as a collector and limits the base drive, thereby causing current-limiting.

Charge pump circuitry in accordance with the invention has proved to be particularly advantageous in an integrated circuit. As described, the circuit functions with low saturation voltage and is current-limited, thereby limiting the supply current.

Claims

1. In a charge pump circuit comprising a supply terminal for connecting to a voltage source, V_{cc} , a ground terminal for connecting to a ground potential, a first capacitor (C1) serially connected with first and second switch means (S1,S2) between said supply terminal and said ground terminal, a third switch means (S3) connected in parallel with said first switch means (S1) and said first capacitor (C1), a second capacitor (C2) serially connected with fourth and fifth switch means (S5,S6) between the common terminal of said first switch means (S1) and said first capacitor (C1) and said ground terminal, a third capacitor (C3) serially connected between a positive voltage ($+2V_{cc}$) terminal and said ground terminal, a fourth capacitor (C4) serially connected with a sixth switch means (S8) between said ground potential and the common terminal of said second capacitor (C2) and said fifth switch means (S6), the common terminal of said fourth capacitor (C4) and said sixth switch means (S8) connected to a negative voltage ($-2V_{cc}$) terminal, and a seventh switch means (S7) connected in parallel with said second capacitor (C2) and said fifth switch means (S6), whereby closure of said first and second switch means (S1,S2) during a first operational phase generates a voltage V_{cc} across said first capacitor (C1), characterised by
an eighth switch means (S4) connected between said positive voltage ($+2V_{cc}$) terminal and the common terminal of said first switch means (S1) and said first capacitor (C1), whereby closure of said third, fourth, fifth and eighth switch means (S3,S5,S6,S4) during a second operational phase transfers a voltage $+2V_{cc}$ to said second and third capacitors (C2,C3), and during a subsequent first operational phase closure of said sixth and seventh switch means (S8,S7) induces a voltage $-2V_{cc}$ to be transferred to said fourth capacitor (C4).
2. The charge pump circuit as defined by claim 1 wherein said third switch means comprises a bipolar transistor (Q1), and further including



biasing circuitry (Q2,Q3) interconnecting said positive voltage $+2V_{cc}$ to the base of said bipolar transistor (Q1) whereby said bipolar transistor has a low saturation voltage.

3. The charge pump circuit as defined by claim 2 wherein said bipolar transistor (Q1) comprises a dual-emitter transistor, one emitter being connected to said biasing circuitry (Q2,Q3) whereby saturation of said transistor limits base drive and thereby causes current-limiting in said transistor.

4. The charge pump circuit as defined in any preceding claim wherein said circuitry comprises an integrated circuit and discrete capacitors.

The charge pump circuit as defined by claim 4 wherein said first switch means comprises a Schottky diode, said second switch means comprises a bipolar transistor, said fourth switch means comprises a bipolar transistor, said fifth switch means comprises a bipolar transistor, said sixth switch means comprises a Schottky diode, said seventh switch means comprises a Schottky diode, and said eighth switch means comprises a Schottky diode.

6. A method of limiting source current using a dual-emitter bipolar transistor in a charge pump circuit according to Claim 3 comprising the steps of providing bias circuitry for said bipolar transistor switch with the base bias for said bipolar transistor switch being derived from said second capacitor ($2V_{cc}$), and a collector voltage derived from said voltage source (V_{cc}), thereby operating said bipolar transistor with low saturation voltage, and

connecting one emitter of said dual-emitter bipolar transistor switch to said bias circuitry whereby operation of said transistor is current-limited.

7. The method as defined by claim 6 wherein said dual-emitter bipolar transistor is an NPN transistor, said step of providing bias circuitry comprising providing a PNP bipolar transistor and an NPN transistor, the emitter of said PNP transistor and the collector of said NPN transistor of said bias circuitry transistors being connected to receive the voltage ($2V_{cc}$), the collector of said PNP transistor being connected to the base of said NPN transistor, the emitter of said NPN transistor being connected to the base of said dual-emitter transistor, and an emitter of said dual-emitter transistor being connected to the base of said NPN transistor

and the collector of said PNP transistor.

Patentansprüche

1. Kapazitiver Spannungswandler mit einer Speiseklemme zum Verbinden mit einer Spannungsquelle V_{cc} ; einer Masseklemme zur Verbindung mit dem Massepotential; einem ersten, zwischen der Speiseklemme und der Masseklemme in Serie mit einer ersten und einer zweiten Schalteinrichtung (S1, S2) verbundenen Kondensator (C1); einer dritten, parallel zu der ersten Schalteinrichtung (S1) und dem ersten Kondensator (C1) geschalteten Schalteinrichtung (S3); einem zweiten, zwischen der gemeinsamen Klemme der ersten Schalteinrichtung (S1) und des ersten Kondensators (C1) und der Masseklemme in Serie mit einer vierten und einer fünften Schalteinrichtung (S5, S6) geschalteten Kondensator (C2); einem dritten, zwischen einer positiven Spannungs-klemme ($+2V_{cc}$) und der Masseklemme angeordneten Kondensator (C3); einem vierten, zwischen dem Massepotential und der gemeinsamen Klemme des zweiten Kondensators (C2) und der fünften Schalteinrichtung (S6) mit einer sechsten Schalteinrichtung (S8) in Serie geschalteten Kondensator (C4), wobei die gemeinsame Klemme des vierten Kondensators (C4) und der sechsten Schalteinrichtung (S8) mit einer negativen Spannungs-klemme ($-2V_{cc}$) verbunden ist; und einer siebenten, parallel zu dem zweiten Kondensator (C2) und der fünften Schalteinrichtung (S6) geschalteten Schalteinrichtung (S7), wobei das Schließen der ersten und zweiten Schalteinrichtung (S1, S2) während einer ersten Operationsphase am ersten Kondensator (C1) eine Spannung V_{cc} erzeugt; gekennzeichnet durch eine achte, zwischen die positive Spannungs-klemme ($+2V_{cc}$) und die gemeinsame Klemme der ersten Schalteinrichtung (S1) und des ersten Kondensators (C1) geschaltete Schalteinrichtung (S4), wobei das Schließen der dritten, vierten, fünften und achten Schalteinrichtungen (S3, S5, S6, S4) während einer zweiten Operationsphase eine Spannung $+2V_{cc}$ zu den zweiten und dritten Kondensatoren (C2, C3) überträgt und während einer nachfolgenden ersten Operationsphase das Schließen der sechsten und siebenten Schalteinrichtungen (S8, S7) das Übertragen einer Spannung $-2V_{cc}$ zum vierten Kondensator (C4) bewirkt.
2. Kapazitiver Spannungswandler nach Anspruch 1, bei dem die dritte Schalteinrichtung (S3) einen bipolaren Transistor (Q1) enthält und der weiterhin eine Vorspannschaltung (Q2, Q3) ein-



schließt, die die positive Spannung $+2V_{CC}$ mit der Basis des bipolaren Transistors (Q1) verbindet, wobei der bipolare Transistor (Q1) eine niedrige Sättigungsspannung hat.

3. Kapazitiver Spannungswandler nach Anspruch 2, bei dem der bipolare Transistor (Q1) einen Doppelemitter-Transistor aufweist, wobei ein Emitter mit der Vorspannschaltung (Q2, Q3) verbunden ist, wodurch die Sättigung des Transistors die Basisansteuerung begrenzt und damit eine Strombegrenzung im Transistor bewirkt wird.
4. Kapazitiver Spannungswandler nach einem der vorangegangenen Ansprüche, bei dem die Schaltung einen integrierten Schaltkreis und getrennte Kondensatoren aufweist.
5. Kapazitiver Spannungswandler nach Anspruch 4, bei dem die erste Schalteinrichtung (S1) eine Schottky-Diode, die zweite Schalteinrichtung (S2) einen bipolaren Transistor, die vierte Schalteinrichtung (S5) einen bipolaren Transistor, die fünfte Schalteinrichtung (S6) einen bipolaren Transistor, die sechste Schalteinrichtung (S8) eine Schottky-Diode, die siebente Schalteinrichtung (S7) eine Schottky-Diode und die achte Schalteinrichtung (S4) eine Schottky-Diode enthalten.
6. Verfahren zum Begrenzen des Speisestroms durch Verwendung eines bipolaren Doppelemitter-Transistors in einem kapazitiven Spannungswandlerschaltkreis nach Anspruch 3, mit den Schritten: Versorgen des Vorspannschaltkreises für den bipolaren Transistorschalter mit der vom zweiten Kondensator abgeleiteten Grundvorspannung für den bipolaren Transistorschalter ($2V_{CC}$) und einer von der Spannungsquelle gelieferten Kollektorspannung (V_{CC}), wodurch der bipolare Transistor mit einer niedrigen Sättigungsspannung betrieben wird und Verbinden eines Emitters des bipolaren Doppelemitter-Transistorschalters mit dem Vorspannschaltkreis, wodurch der Betrieb des Transistors mit einer Strombegrenzung durchgeführt wird.
7. Verfahren nach Anspruch 6, bei dem der bipolare Doppelemitter-Transistor ein NPN-Transistor ist, der Schritt des Vorsehens der Vorspannschaltung das Vorsehen eines bipolaren PNP-Transistors und eines NPN-Transistors enthält, wobei der Emitter des PNP-Transistors und der Kollektor des NPN-Transistors der Transistoren der Vorspannschaltung zum Aufnehmen der Spannung ($2V_{CC}$) geschaltet sind,

der Kollektor des PNP-Transistors mit der Basis des NPN-Transistors verbunden ist, der Emitter des NPN-Transistors mit der Basis des Doppelemitter-Transistors verbunden ist, und ein Emitter des Doppelemitter-Transistors mit der Basis des NPN-Transistors sowie dem Kollektor des PNP-Transistors verbunden ist.

Revendications

1. Un circuit de pompe de charge comprenant une borne d'alimentation destinée à être connectée à une source de tension, V_{CC} , une borne de masse destinée à être connectée à un potentiel de masse, un premier condensateur (C1) connecté en série avec des premier et second éléments de commutation (S1, S2) entre la borne d'alimentation et la borne de masse, un troisième élément de commutation (S3) connecté en parallèle avec le premier élément de commutation (S1) et le premier condensateur (C1), un second condensateur (C2) connecté en série avec des quatrième et cinquième éléments de commutation (S5, S6) entre la borne commune du premier élément de commutation (S1) et du premier condensateur (C1), et la borne de masse, un troisième condensateur (C3) connecté en série entre une borne de tension positive ($+2V_{CC}$) et la borne de masse, un quatrième condensateur (C4) connecté en série avec un sixième élément de commutation (S8) entre le potentiel de masse et la borne commune du second condensateur (C2) et du cinquième élément de commutation (S6), la borne commune du quatrième condensateur (C4) et du sixième élément de commutation (S8) étant connectée à une borne de tension négative ($-2V_{CC}$), et un septième élément de commutation (S7) connecté en parallèle avec le second condensateur (C2) et le cinquième élément de commutation (S6), grâce à quoi la fermeture des premier et second éléments de commutation (S1, S2) pendant une première phase de fonctionnement produit une tension V_{CC} aux bornes du premier condensateur (C1), caractérisé par
un huitième élément de commutation (S4) connecté entre la borne de tension positive ($+2V_{CC}$) et la borne commune du premier élément de commutation (S1) et du premier condensateur (C1), grâce à quoi la fermeture des troisième, quatrième, cinquième et huitième éléments de commutation (S3, S5, S6, S4) pendant une seconde phase de fonctionnement transfère une tension $+2V_{CC}$ vers les second et troisième condensateurs (C2, C3), et pendant une première phase de fonctionnement suivante, la fermeture des sixième et



septième éléments de commutation (S8, S7) induit une tension $-2V_{cc}$ qui sera transférée vers le quatrième condensateur (C4).

2. Le circuit de pompe de charge défini par la revendication 1, dans lequel le troisième élément de commutation consiste en un transistor bipolaire (Q1), et il existe en outre un circuit de polarisation (Q2, Q3) qui applique la tension positive $+2V_{cc}$ à la base de ce transistor bipolaire (Q1), grâce à quoi ce transistor bipolaire a une faible tension de saturation. 5
3. Le circuit de pompe de charge défini par la revendication 2, dans lequel le transistor bipolaire (Q1) consiste en un transistor à deux émetteurs ayant un émetteur connecté au circuit de polarisation (Q2, Q3), grâce à quoi la saturation de ce transistor limite le niveau d'attaque de base et produit ainsi une limitation de courant dans le transistor. 10
4. Le circuit de pompe de charge défini dans l'une quelconque des revendications précédentes, comprenant un circuit intégré et des condensateurs discrets. 15
5. Le circuit de pompe de charge défini par la revendication 4, dans lequel le premier élément de commutation consiste en une diode Schottky, le second élément de commutation consiste en un transistor bipolaire, le quatrième élément de commutation consiste en un transistor bipolaire, le cinquième élément de commutation consiste en un transistor bipolaire, le sixième élément de commutation consiste en une diode Schottky le septième élément de commutation consiste en une diode Schottky et le huitième élément de commutation consiste en une diode Schottky. 20
6. Un procédé de limitation de courant de source utilisant un transistor bipolaire à deux émetteurs dans un circuit de pompe de charge selon la revendication 3, comprenant les étapes suivantes : on établit un circuit de polarisation pour l'élément de commutation à transistor bipolaire, en obtenant la polarisation de base pour l'élément de commutation à transistor bipolaire à partir du second condensateur ($2V_{cc}$), et en obtenant une tension de collecteur à partir de la source de tension (V_{cc}), ce qui fait fonctionner le transistor bipolaire avec une faible tension de saturation, et 25
- on connecte au circuit de polarisation un émetteur de l'élément de commutation à transistor bipolaire à deux émetteurs, grâce à quoi ce transistor fonctionne avec une condition de 30

limitation de courant.

7. Le procédé défini par la revendication 6, dans lequel le transistor bipolaire à deux émetteurs est un transistor NPN, l'étape d'établissement d'un circuit de polarisation comprend l'incorporation d'un transistor bipolaire PNP et d'un transistor NPN, l'émetteur du transistor PNP et le collecteur du transistor NPN des transistors du circuit de polarisation étant connectés de façon à recevoir la tension ($2V_{cc}$), le collecteur du transistor PNP étant connecté à la base du transistor NPN, l'émetteur du transistor NPN étant connecté à la base du transistor à deux émetteurs, et un émetteur du transistor à deux émetteurs étant connecté à la base du transistor NPN et au collecteur du transistor PNP. 35