METHOD AND SYSTEM FOR BUFFERING INSTRUCTIONS IN A PROCESSOR

ABSTRACT OF THE DISCLOSURE

According to one embodiment of the invention, a method of buffering instructions in a processor having a pipeline having a decode stage includes detecting stalling of the decode stage, reissuing a previous fetch for an instruction in a memory until the decode stage is no longer stalled, and writing the fetch instruction into an instruction buffer after the decode stage is no longer stalled.

Figure 1