SUMMARY

Embodiments of the invention overcome at least one of the disadvantages of the prior art.

According to a first aspect of the present invention, there is provided a method for decoding a video including: decoding a partitioning tree structure corresponding to a partitioning process of a block of an image of the video; decoding said block based at least on said partitioning tree structure; wherein the partitioning tree structure has a switching node representing a predetermined partitioning block size, such that, above the switching node, luma blocks and chroma blocks share a single partitioning tree structure, and at or below the switching node, luma blocks and chroma blocks have separate partitioning tree structures.

According to a second aspect of the present invention, there is provided an apparatus including a memory and one or more processors configured to decode a video, wherein the one or more processors are further configured to: decode a partitioning tree structure corresponding to a partitioning process of a block of an image of the video; decode said block based at least on said partitioning tree structure; wherein the partitioning tree structure has a switching node representing a predetermined partitioning block size, such that, above the switching node, luma blocks and chroma blocks share a single partitioning tree structure, and at or below the switching node, luma blocks and chroma blocks have separate partitioning tree structures.

According to a third aspect of the present invention, there is provided a method including encoding a video, said encoding including: determining a partitioning tree structure corresponding to a partitioning process of a block of an image of the video; coding said block based at least on said partitioning tree structure; wherein the partitioning tree structure has a switching node representing a predetermined partitioning block size, such that, above the switching node, luma blocks and chroma blocks share a single partitioning tree structure, and at or below the switching node, luma blocks and chroma blocks have separate partitioning tree structures.

According to a fourth aspect of the present invention, there is provided an apparatus including a memory and one or more processors configured to encode a video, wherein the one or more processors are further configured to: determine a partitioning tree structure corresponding to a partitioning process a block of an image of the video, code said block based at least on said partitioning tree structure, wherein the partitioning tree structure has a switching node representing a predetermined partitioning block size, such that, above the switching node,

luma blocks and chroma blocks share a single partitioning tree structure, and at or below the switching node, luma blocks and chroma blocks have separate partitioning tree structures.

According to a fifth aspect of the present invention, there is provided a non-transitory program storage device, readable by a computer, tangibly embodying a program of instructions executable by the computer for performing the method according to the first aspect or the second aspect.

According to one embodiment, the partially shared partitioning tree structure is used for coding or decoding a block belonging to a part of the video image coded in Intra, for instance a tile or a tiles group.

According to one embodiment, the partially shared partitioning tree structure is used for coding or decoding a block belonging to a part of the video image coded in Inter, for instance a tile or a tiles group.

According to one embodiment, the switching node is implicitly determined. According to a variant of this embodiment, the switching block node is determined based on a partitioning block size. Advantageously, the partitioning block size corresponds to the decoding pipeline unit size and is, for instance, set to 64x64. According to another variant of this embodiment, the switching node is determined based on a partitioning depth level. Advantageously, the partitioning depth level is set to one depth of quad-tree split of the partitioning tree and corresponds to the quad-tree split of a 128x128 CTU into 4 sub-CUs of size 64x64 thus compatible with the decoding pipeline unit size.

A decoding pipeline unit may also be called a Virtual Decoding Pipeline Unit (VPDU).

According to another embodiment, the switching node is signaled. Advantageously, this embodiment allows to adapt the switching node for each CTU, for instance based on RD cost.

According to another embodiment, a signal is provided comprising video data generated according to the method or the apparatus of any of the preceding descriptions. According to another embodiment, the signal data is interleaved based on a partitioning block size. The signal data is thus advantageously arranged for the decoding pipeline unit.

One or more of the present embodiments also provide a computer readable storage medium having stored thereon instructions for encoding or decoding video data according to any of the methods described above. The present embodiments also provide a computer readable storage medium having stored thereon a bitstream generated according to the methods

described above. The present embodiments also provide a method and apparatus for transmitting the bitstream generated according to the methods described above. The present embodiments also provide a computer program product including instructions for performing any of the methods described.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 illustrates an example of Coding Tree Unit (CTU) and Coding Tree (CT) concepts to represent a compressed HEVC picture.

FIG. 2 illustrates an example of partitioning of a Coding Unit and associated Coding Tree in the Quad-Tree plus Binary-Tree (QTBT) scheme.

FIGs. 3 and 4 illustrate examples of some CU binary or triple tree partitioning.

FIGs. 5 and 6 illustrate examples of partitioning of a non-limiting embodiment of CTU, respectively in Luma and Chroma components according to a general aspect of at least one embodiment.

FIG. 7 and 8 illustrate various examples of an encoding method according to a general aspect of at least one embodiment.

FIG. 9, 10, 11 and 12 illustrate various examples of a decoding method according to a general aspect of at least one embodiment.

FIG 13 illustrates a block diagram of an embodiment of video encoder in which various aspects of the embodiments may be implemented.

FIG. 14 illustrates a block diagram of an embodiment of video decoder in which various aspects of the embodiments may be implemented.

FIG. 15 illustrates a block diagram of an example apparatus in which various aspects of the embodiments may be implemented.

DETAILED DESCRIPTION

It is to be understood that the figures and descriptions have been simplified to illustrate elements that are relevant for a clear understanding of the present principles, while eliminating, for purposes of clarity, many other elements found in typical encoding and/or decoding devices. It will be understood that, although the terms first and second may be used herein to describe various elements, these elements should not be limited by these terms. These terms are only used to distinguish one element from another.

CLAIMS

1. A method for decoding a video comprising:

- decoding a partitioning tree structure corresponding to a partitioning process of a block of an image of the video;

- decoding said block based at least on said partitioning tree structure;

wherein the partitioning tree structure has a switching node representing a predetermined partitioning block size, such that, above the switching node, luma blocks and chroma blocks share a single partitioning tree structure, and at or below the switching node, luma blocks and chroma blocks have separate partitioning tree structures.

2. The method according to claim 1 wherein said partitioning tree structure is used for decoding a block belonging to a part of the video image coded in Intra mode.

3. The method according to claim 1 wherein said partitioning tree structure is used for decoding a block belonging to a part of the video image coded in Inter mode.

4. The method according to claim 1 wherein the switching node is implicitly determined.

5. The method according to claim 1 wherein said partitioning block size is set to 64x64.

6. The method according to claim 1 wherein the switching node is signaled.

7. An apparatus comprising a memory and one or more processors configured to decode a video, wherein the one or more processors are further configured to:

- decode a partitioning tree structure corresponding to a partitioning process of a block of an image of the video;

- decode said block based at least on said partitioning tree structure;

wherein the partitioning tree structure has a switching node representing a predetermined partitioning block size, such that, above the switching node, luma blocks and chroma blocks share a single partitioning tree structure, and at or below the switching node, luma blocks and chroma blocks have separate partitioning tree structures.

8. The apparatus according to claim 7 wherein said partitioning tree structure is used for decoding a block belonging to a part of the video image coded in Intra mode.

9. The apparatus according to claim 7 wherein said partitioning tree structure is used for decoding a block belonging to a part of the video image coded in Inter mode.

10. The apparatus according to claim 7 wherein the switching node is implicitly determined.

11. The apparatus according to claim 7 wherein said partitioning block size is set to 64x64.

12. The apparatus according to claim 7 wherein the switching node is signaled.

13. A method comprising encoding a video, said encoding comprising:

- determining a partitioning tree structure corresponding to a partitioning process of a block of an image of the video;
- coding said block based at least on said partitioning tree structure;

wherein the partitioning tree structure has a switching node representing a predetermined partitioning block size, such that, above the switching node, luma blocks and chroma blocks share a single partitioning tree structure, and at or below the switching node, luma blocks and chroma blocks have separate partitioning tree structures.

14. The method according to claim 13 wherein said partitioning tree structure is used for coding a block belonging to a part of the video image coded in Intra mode.

15. The method according to claim 13 wherein said partitioning tree structure is used for coding a block belonging to a part of the video image coded in Inter mode.

16. The method according to claim 13 wherein the switching node is implicitly determined.

17. The method according to claim 13 wherein said partitioning block size is set to 64x64.

18. The method according to claim 13, wherein the switching node is signaled.

19. An apparatus comprising a memory and one or more processors configured to encode a video, wherein the one or more processors are further configured to:

- determine a partitioning tree structure corresponding to a partitioning process a block of an image of the video,
- code said block based at least on said partitioning tree structure,

wherein the partitioning tree structure has a switching node representing a predetermined partitioning block size, such that, above the switching node, luma blocks and chroma blocks share a single partitioning tree structure, and at or below the switching node, luma blocks and chroma blocks have separate partitioning tree structures.

20. The apparatus according to claim 19 wherein said partitioning tree structure is used for coding a block belonging to a part of the video image coded in Intra mode.

21. The apparatus according to claim 19 wherein said partitioning tree structure is used for coding a block belonging to a part of the video image coded in Inter mode.

22. The apparatus according to claim 19 wherein the switching node is implicitly determined.

23. The apparatus according to claim 19 wherein said partitioning block size is set to 64x64.

24. The apparatus according to claim 19 wherein the switching node is signaled.

25. A non-transitory program storage device, readable by a computer, tangibly embodying a program of instructions executable by the computer for performing the method according to any one of claims 1 to 6 or claims 13 to 18.