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FLOATING GATE MEMORY DEVICE USING COMPOSITE MOLECULAR MATERIAL

RELATED APPLICATIONS

[01] This application contains subject matter related to the subject matter disclosed in copending U.S. Provisional Patent Application Serial No. 60/289,091, filed on May 7, 2001, entitled "Floating Gate Memory Device Using Composite Molecular Material".

FIELD OF THE INVENTION

[02] The invention relates to a floating gate memory cell for data storage applications, and more particularly, to a floating gate memory device having a variable resistance dielectric as a gate insulator.

BACKGROUND OF THE INVENTION

[03] Computer data storage, in particular random access memory (RAM) has become an increasingly important component of electronic hardware. There are various distinct types of memory devices, distinguished by their speed and data retention characteristic. Dynamic random access memory (DRAM) is a volatile memory characterized by a destructive read. This means that it is necessary to supply voltage to the memory bits at all times, or the information will disappear. Furthermore, each memory element has associated with it a transistor. Static random access memory (SRAM) stores data in a bistable flip-flop, commonly consisting of cross-coupled inverters. It is called "static" because it will retain a value as long as power is supplied. It is still volatile, i.e. it will lose its contents when the power is switched off, in contrast to ROM. SRAM is usually faster than DRAM, but each bit requires several transistors (about six), so that a lesser number of bits of SRAM fit in the same area as compared to DRAM.

[04] When the gate electrode of a conventional MOSFET is modified so that semi-permanent charge storage inside the gate is possible, the new structure becomes a nonvolatile memory device (floating gate transistor). Nonvolatile memory devices have been extensively used in integrated circuits, such as the electrically alterable read-only memory (EAOM), the erasable-programmable read-only memory (EPROM), and the nonvolatile random-access memory (NVRAM).

[05] In a floating gate transistor, charges are injected from the silicon across a first insulator and stored in the floating gate or at the insulator-oxide interface. The stored charge gives rise to a threshold voltage shift, and the device is at a higher-threshold voltage state. A long retention time is required for nonvolatile memory operation. The retention time is defined as a time when the stored charge decreases to 50% of its initial value. For a well-designed memory device, the charge retention time can be over 100 years. To erase the stored charge and return the device to a "low-threshold voltage state," a high reverse voltage is applied to the gate and/or the device is exposed to UV light. The conventional erase process is relatively slow.

[06] There is a need for a floating gate memory device with decreased erase time and that does not require the application of UV light.

SUMMARY OF THE INVENTION

[07] These and other needs are met by embodiments of the present invention which provide a floating gate memory device comprising a substrate and a first insulating layer on the substrate. A floating gate is provided on the first insulating layer, and a second insulating layer is on the floating gate. A control gate is formed on the second insulating layer. At least one of the first or the second insulating layers has a controllably variable resistivity.

[08] In certain embodiments, at least one of the first and second insulating layers consists of a molecular matrix with ionic complexes distributed through the molecular matrix .

[09] With the present invention, the resistivity (or conductivity) can be changed in response to the application of an electric field. By switching the resistivity from a highly

resistive state, where charge is retained by the floating gate, to a lower resistivity state, the charge stored on the floating gate can be drained off to the gate electrode.

[10] Other embodiments of the invention also satisfy the above-stated needs by providing a memory device comprising a first insulating layer, a floating gate on the first insulating layer, a second insulating layer on the floating gate, and a control gate on the second insulating layer. At least one of the first and second insulating layers comprises a material switchable between low and high conductivity states in response to an applied electric field.

[11] The earlier stated needs are also met by further aspects of the present invention which provide a memory device comprising a floating gate, an insulating layer on the floating gate, and a control gate on the insulating layer. The insulating layer comprises a molecular matrix with ionic complexes distributed in the molecular matrix.

[12] The earlier stated needs are also met by a still further aspect of the invention which provides a method of operating a floating gate memory device. This method comprises the steps of maintaining an insulating layer between a floating gate and a control gate in a first conductivity state that is sufficient to retain a floating gate charge for at least a predetermined period of time. An electric field is applied to the insulating layer to place the insulating layer in a second conductivity state having at least an order of magnitude greater conductivity than the first conductivity state sufficient to discharge the floating gate charge.

[13] The foregoing and other features, aspects and advantages of the present invention will become more apparent from the following detailed description of the present invention when taken in conjunction with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

[14] Fig. 1 shows a nonvolatile memory device that is a floating gate transistor constructed in accordance with an embodiment of the present invention;

[15] Fig. 2a-d show a molecular composite material between two electrodes in various operational states according to a current theoretical understanding of the invention;

[16] Fig. 3 shows a voltage-current characteristic for write and erase operation of the memory device of the present invention; and

[17] Fig. 4 shows the dependence on writing pulse critical amplitude on writing pulse time.

DETAILED DESCRIPTION OF THE INVENTION

[18] Referring first to Fig. 1, a floating gate transistor may be considered to be a modified MOSFET transistor with a floating conductive pad embedded in the dielectric that insulates the gate from the source/drain. Because of the very high resistivity of commonly used dielectrics, such as SiO_2 and Si_3O_4, any electric charge deposited on the floating gate will remain there during the retention time of the device, which can be years. However, it is difficult to discharge the floating gate simply by applying a reverse external electric field because of the large electrical resistance of the tunnel barrier in the reverse direction. For this reason, the conductivity of the dielectric is typically enhanced by illuminating the dielectric with UV light. The present invention provides a structure that avoids the need for UV light.

[19] The present invention address and solves problems related to the control and structure of a floating gate memory device. In particular, the present invention provides for a floating gate memory device that has an insulating layer that acts to either electrically insulate the floating gate from a control gate, or has an increased conductivity to allow for a rapid discharge of the floating gate charge. This is achieved, in part, by employing a floating gate transistor having an insulating layer between the control gate and the floating gate that comprises a composite material that exhibits structural electronic instability in one dimension and enables static and dynamic control over the conductivity of the composite material. As an exemplary composite material, a molecular matrix is employed with ionic complexes in the matrix. Under the application of an electric field, the ionic complexes dissociate controllably to change the electrical conductivity of the insulating layer.

[20] Figure 1 depicts an exemplary embodiment of the floating gate memory device constructed in accordance with present invention. The floating gate memory device includes substrate 12 in which are formed source and drain regions 14, 16, respectively.

[21] A first insulator 18 is formed on the substrate 10 and spans the source and drain regions 14, 16. A floating gate 20 formed of conductive material, is formed on the first

insulating layer 18. A second insulating layer 22 is formed on the floating gate 20, followed by the formation of gate electrode 24 on the second insulating layer 22. The gate electrode 24 and the drain region 16 are depicted as being connected to voltages V_g and V_d, respectively. The gate electrode 24, like the floating gate 20, comprises a conductive material.

[22] According to certain embodiments, at least one of the two dielectric layers 18, 22 depicted in Fig. 1 comprise a one-dimensional molecular system exhibiting a transition from a low electrical conductivity to a high electrical conductivity and *vice versa*. This transition is typically manifested by an S-shaped (reentrant) voltage-current characteristic with metastable or stable memory. The impedance of such memory cells can be between ~10 MΩ and ~100 Ω for example, depending on the switching condition. Examples of such molecular systems are systems with a low dimensionality exhibiting a so-called Peierls transition.

[23] A number of different materials may be used as the insulating layers 18, 22. Exemplary materials are described in more detail below, but are also discussed in an article by Yu H. Krieger, entitled "Structural Instability of One-Dimensional Systems as a Physical Principle Underlying the Functioning of Molecular Electronic Devices", Journal of Structural Chemistry, Vol. 40, No. 4, 1999 (Yu H. Krieger), expressly incorporated by reference herein.

[24] There are two predominant types of structural organization of such systems. First, there are strands of linear conjugated polymers, which are weakly bonded to each other and whose mutual arrangement is generally poorly organized. Second, there are crystal structures, where the individual molecules form one-dimensional columns and interact with each other much more actively than molecules from different columns do.

[25] Polyconjugated systems primarily involve polyvinylenes, i.e., polymers with an acyclic conjugation system, in which the one-dimensional character of structure is dictated by the mechanism of conjugation in linear macromolecules. Polyacetylene is a classical representative of this class of polymers. Its electronic structure is a prototype for many other conjugated polymers.

[26] Another wide class of molecular compounds are formed from aromatic and heterocyclic molecules which possess high electric conductivity due to π-bonds between molecules. Such molecular systems are called π-complexes or charge transfer complexes,

with those systems whose structure involves isolated one-dimensional columns or strands possessing pronounced electro-physical properties of interest for switching and memory applications. Molecular charge transfer complexes are donor–acceptor systems formed from two molecules: one possessing donor and another acceptor properties. Among the well-defined complexes with a one-dimensional structure, tetra-cyano-quino-dimethane (TCNQ) are planar molecules with unsaturated bonds, arranged in a crystal as parallel stacks forming a quasi-one-dimensional system.

[27] In another class of one-dimensional systems, the cations are dynamically disordered. It involves molecular compounds having the general formula $(TMTSF)_2X$. Transition metal salts of $K_2\ Pt(CN)_4\ Br_{0.3}\times\ 3H_2O$ (KCP) type are also the typical representatives of mixed-valence quasi-one-dimensional complexes, as are phthalocyanines and porphyrins. Moreover, pure inorganic compounds, such as $NbSe_3$, are also interesting examples of compounds with quasi-one-dimensional structure.

[28] While not being bound by theory, the following is currently believed by the inventors to describe the mechanism for the conductivity change in the material in the present invention. An exemplary molecular composite that can be applied as at least one of the insulating layers 18, 22 in the floating gate transistor 10 is shown in Figs. 2a – 2d. The molecular composite includes a quasi-one-dimensional, or at least structurally and electrically anisotropic, molecular matrix, wherein ionic complexes are distributed in the matrix. Polyconjugated compounds, such as the exemplary quasi-one-dimensional systems described above, for example, polyphenylacetylene, can be used as the anisotropic molecular matrix. The ionic complex can be a salt, such as sodium chloride (NaCl), or any other material that can dissociate in an applied electric field. The exemplary anisotropic molecular matrix is depicted in Figs. 2 a-d as comprising an assembly of chain-like molecules oriented perpendicular to the electrode surfaces. However, other orientations of those molecules or of anisotropic "channels" are possible as long as a charge separation of the type depicted in Figs. 2 a-d is enabled.

[29] Electric switching in the molecular thin films depicted in Figs. 2a-d is characterized by the existence of two stable states, a high impedance state ("off" state) and a low

impedance state ("on" state). The impedance of this "off" state is usually more than ~10 MΩ., for example. Switching from the "off" state to the "on" state occurs when an applied electric field exceeds a threshold value. The impedance of this "on" state can be less than ~100 Ω., for example. A transition from "on" state back to the "off" state can take place by reversing the polarity of the electric field.

[30] Two modes of the "on" state are identifiable: a metastable mode (Fig.2b) and a stable mode (Fig.2c). The metastable mode of the memory cell function is characterized by the low P_W and P_{ER} value (0.1-0.5V), high impedance of the "ON" state (wide region, about 1kΩ - 1MΩ), short switching time (less than 1μs), and short retention time between about 10 s or several hours. Conversely, the stable mode of the memory cell operation shows the high P_W and P_{ER} value (3-10V), low impedance of the "ON" state (less than 100 Ω), long switching time (1 ms and more) and long storage time (between several months and years). Some memory cells made from this material have been observed to exhibit substantially unchanged electrical properties in the stable mode after storage for six years.

[31] Fig. 2a illustrates the "off" state, where the electrical conductivity is essentially zero, assuming that the anisotropic molecular matrix itself is a good electrical insulator. When an external electric field E is applied, as indicated in Fig. 2b, the sodium salt dissociates into sodium and chlorine ions, and the ions are displaced from their original position in the anisotropic molecular matrix, resulting in an increase in the electrical conductivity to the metastable "on" state. Upon further increase of the electric field, the ions become more strongly separated (Fig. 2c), accompanied by a still further increase in the conductivity of the "on" state to the above-described stable state . When a very large field is applied over a long time, the anions and cations accumulate at the electrodes (Fig. 2d), resulting in a sharp decrease in the electrical conductivity due to the absence of mobile charges ("off" state).

[32] The electrode material can be, for example, a metal, such as Al or Cu, ITO, a semiconductor or a conducting polymer. The transition from the "off" state depicted in Fig. 2a to the "on" state depicted in Fig. 2b requires application of an external voltage of approximately 3-5 V for a time period of approximately 10-100 ns. The transition from the "off" state depicted in Fig. 2a to the "on" state depicted in Fig. 2c having a higher electrical

conductivity and longer retention time is achieved by applying an external voltage of approximately 3-5 V for a time period of approximately 300 ns – 1 μs. A molecular composite comprising polyphenylacetylene and ~5-7% NaCl as the ionic complex are described in these figures as an exemplary embodiment.

[33] In an application as a variable conductivity gate insulator with a floating gate transistor, replacing at least one of the traditional dielectrics (e.g., insulating layer 22), the conductivity is switched between a low conductivity state, where charge is retained by the floating gate, and a higher conductivity state, where the charge stored on the floating gate 20 can be drained off to the gate electrode 27. The floating gate 20 can thereafter be restored to its original state, i.e., isolated from the gate 24, by applying a reverse potential between the source/drain 14, 16 and the gate electrode 24.

[34] The current-voltage (I-V) characteristic of a floating gate transistor, as it applies to the state of the composite material forming, for example, insulating layer 22, is shown in Fig. 3. The positive voltage applied to the gate electrode with respect to the ground will be referred to as write voltage (in pulsed experiments, as write pulse) (P_W), which renders the insulating layer 22 conductive, and the negative voltage, which restores the insulating properties of insulating layer 22, as erase voltage (or erase pulse) (P_{ER}), respectively.

[35] Fig. 3 shows a typical I-V curve for write (positive applied voltage) and erase operation (negative applied voltage). The device is in the "off" state, until the applied voltage reaches a critical value of approximately 0.3 V. In the "off" state, the electric current through the memory cell is essentially zero. When the applied voltage exceeds the critical voltage of 0.3V, the memory cell 10 approaches zero resistance, with the voltage across the cell dropping to a very small value and the current increasing to more than 120 μA, with the cell attaining the "on" state. The cell remains in the "on" state until a negative voltage is applied, which in the present example is approximately -1 V. This represents the erase cycle. After the erase cycle is completed, the cell is again in the "off" state. The parameters (voltage, pulse duration) used for the erase operation depend on the characteristic values of the "on" state of the device.

[36] Referring now to Fig. 4, the pulse duration of a write pulse required to change the conductivity of the insulating layer 22 is related to the amplitude of the write pulse. For example, insulating layer 22 may be switched from the "off" state to the "on" state by applying a pulse of 4 V for 10 μs, whereas a pulse duration of more than 1 ms may be required when writing with a voltage of approximately 1 V. Accordingly, the speed with which the conductivity of the insulating layer 22 of the device 10 changes can be adapted to specific applications.

[37] The present invention thus provides an easily erasable floating gate transistor memory chip for systems, employing molecular memory cells. The electronic circuitry of the erasable floating gate transistor memory chip can be based on that of well-developed DRAM chips. Depending on the "state" of the memory cell, i.e., a metastable or stable state, the circuit can work as either SRAM or DRAM.

[38] Although the present invention has been described and illustrated in detail, it is to be clearly understood that the same is by way of illustration and example only and is not to be taken by way of limitation, the scope of the present invention being limited only by the terms of the appended claims.

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What is Claimed is:

1. (Amended) A floating gate memory device, comprising:

a substrate;

a first insulating layer on the substrate;

a floating gate in electrical contact with the first insulating layer;

a second insulating layer in electrical contact with the floating gate; and

a control gate on the second insulating layer;

wherein at least one of the first and second insulating layers has a controllably variable resistivity.

2. The device of claim 1, wherein at least one of the first and second insulating layers comprises a molecular matrix.

3. The device of claim 2, wherein the at least one of the first and second insulating layers further comprises ionic complexes distributed through the molecular matrix.

4. The device of claim 3, wherein the ionic complexes are dissociable in the molecular matrix under the influence of an applied electronic field.

5. The device of claim 4, wherein the molecular matrix comprises a polyconjugated compound.

6. The device of claim 5, wherein the polyconjugated compound is one of: polyparaphenylene, polyphenylvenyene, polyaniline, polythiopene, or polypyrrole.

7. The device of claim 4, wherein the molecular matrix comprises aromatic and heterocyclic molecules.

8. The device of claim 4, wherein the molecular matrix comprises a quasi-one-dimensional complex.

9. The device of claim 8, wherein the quasi-one-dimensional complex is a phtalocyanine.

10. The device of claim 8, wherein the quasi-one-dimensional complex is a porphyrin.

11. (Amended) The device of claim 4, wherein the molecular matrix is an anisotropic inorganic material.

12. (Amended) The device of claim 11, wherein the anisotropic inorganic material is $NBSe_3$.

13. The device of claim 4, wherein the molecular matrix is a molecular compound of $(TMTSF)_2X$.

14. The device of claim 4, wherein the molecular matrix is a transition metal salt of $K_2Pt(CN)_4Br_{0.3}x3H_2O$(KCP) type.

15. (Amended) A memory device comprising:

a first insulating layer;

a floating gate in electrical contact with the first insulating layer;

a second insulating layer in electrical contact with the floating gate; and

a control gate on the second insulating layer;

wherein at least one of the first and second insulating layers comprises a material switchable between low and high conductivity states in response to an applied electric field.

16. The device of claim 15, wherein the material is a molecular matrix.

17. The device of claim 16, further comprising ionic complexes distributed through the molecular matrix.

18. The device of claim 17, wherein the ionic complexes are dissociable in the molecular matrix under the influence of an applied electric field.

19. The device of claim 18, wherein the molecular matrix comprises a polyconjugated compound.

20. The device of claim 18, wherein the molecular matrix comprises aromatic and heterocyclic molecules.

21. The device of claim 18, wherein the molecular matrix comprises a quasi-one-dimensional complex.

22. The device of claim 21, wherein the quasi-one-dimensional complex is at least one of phtalocyanine or a porphyrin.

23. (Amended) A memory device comprising:

a floating gate;

an insulating layer in electrical contact with the floating gate; and

a control gate on the insulating layer;

wherein the insulating layer comprises a molecular matrix that provides the insulating layer with a variable electric conductivity.

24. The memory device of claim 23, wherein the insulating layer further comprises ionic complexes distributed in the molecular matrix.

25. The device of claim 24, wherein the molecular matrix comprises a polyconjugated polymer.

26. The device of claim 24, wherein the molecular matrix comprises aromatic and heterocyclic molecules.

27. The device of claim 24, wherein the molecular matrix comprises a quasi-one-dimensional complex.

28. The device of claim 27, wherein the quasi-one-dimensional complex is at least one of a phtalocyanine or a porphyrin.