

The invention concerns a method for converting a digital signal to an analog signal. Such a method is known from EP-A-0280321, in which only a part of the digitalized signal or of the dual number is combined with at least one correction factor. The correction factor is selected by the part of the digitalized signal or the dual number which is not combined with the correction factor. Also, the digital-to-analog converter arrangement according to EP-A-0280321 comprises two separate D/A converters with a downstream connected analog adder. Moreover, it is only possible to perform a D/A conversion of fixed point dual numbers, with no exact D/A conversion of floating point dual numbers, however.

EP-A-0329148 describes a D/A converter arrangement for floating point numbers. A correction is performed by using as mantissa a part only of the digital signal. For improving accuracy the mantissa to be converted is selected by a digital shift circuit from the incoming digital signal. However, by doing this the mantissa is not combined arithmetically with a correction factor.

According to the present invention, the digital signal is generated as a dual number, preferably a floating point dual number. A floating point dual number consists of a mantissa with M bits and an exponent on the base of a power of two with E conditions. Using a D/A converter arrangement, consisting of, for example, a D/A converter, to which the mantissa of the floating point dual number is fed, and a switchable evaluator downstream of the D/A converter, which evaluator is controlled by the exponent of the floating point dual number, in which the D/A converter arrangement may be subject to tolerance errors, the digital signal is converted to a corresponding analog signal.

Such a floating point dual number representation as described above is not only incorporated in computer systems but also in PCs, all-digital amplifiers, digital pre-amplifiers and in signal processors as well, and is frequently supported by arithmetic processors.

In order for the floating point dual number representation to be correct, the evaluator should be divisible or switchable exactly in powers of the base of the exponent (e.g. 1, $1/2$, $1/4$, $1/8$, $1/16$), which is frequently ensured by a very precisely balanced divider circuit in the evaluator.

The switchable evaluator, which is also designated as switchable amplification means, is controlled by the exponent of the floating point dual number so that the correct scaling of the converter values is always carried out or the correct switching stage is always selected.

The problem and the disadvantage with this sort of digital-to-analog conversion is that the accuracy of the D/A conversion is very strongly dependent on the accuracy of the scaling of the switching stages of the evaluator because otherwise the analog scaling does not correspond to the conversion in the digital range when forming the floating point dual number. However, the switching stages are frequently subject to tolerance errors. In order to guarantee a sufficiently high accuracy and therewith, as few tolerance steps or errors as possible of the switching stages or the scaling stages, the switching stages are either realized using very accurate precision components or constructed by means of (trimming) potentiometers for precise balancing after the construction of the divider circuit (e.g. $1:1/2:1/4:1/8:1/16$) for the amplification.

While the solution using high-precision components is very cost-intensive because these components are very expensive, the solution using the potentiometers has problems in the mechanical and thermal long-term stability of the components.

It is the object of the invention to develop and improve a method according to the preamble of claim 1, which guarantees an essentially exact conversion of digital signals to analog signals.

In principle, this task is solved in that the dual number is arithmetically combined with at least one correction factor compensating tolerance errors, and selected by the dual number to be converted itself. Every or each required correction factor is preferably stored, assigned to one or more different dual numbers.

If the dual number is generated as a floating point dual number, the mantissa of the floating point dual number is arithmetically combined with one or more correction factor or factors compensating tolerance errors, in which advantageously the arithmetic combination is a multiplication and/or addition.

Use of the invention means that the precise balancing of the scaling stages in the analog section of the D/A converter arrangement is no longer necessary. Instead, the mantissa value, which is supplied to the D/A converter, is (pre-)matched, through an arithmetic combination with a correction factor, to the inaccurate scaling of the switching stage controlled by the exponent of the floating point dual number in such a way that after the scaling, the correct, analog output value is obtained. Thus a tolerance error in a switching stage no longer has an adverse effect on the evaluation

of a floating point dual number or on a digital signal.

Thus, instead of an analog balancing of the scaling stages, a digital balancing is performed.

Moreover, using the invention one (or more) systematic conversion error(s) of the D/A converter itself can be so corrected by a suitable correction on the digital side of the D/A converter that an exact conversion value of a digital input value is available at the output.

Through the prematching of the mantissa value to the inaccuracy or tolerance error of the respectively selected switching stage of the amplifier or the D/A converter, a simple process is surprisingly made available which is not sensitive as regards faults in components, and thermal and mechanical influences, and enables expensive elements or components to be avoided in a simple manner.

With the floating point representation of the dual number, it is advantageous that the correction factor for correcting the error or errors of the evaluator is stored and the corresponding correction factor is selected like the switching stages of the evaluator by the exponent of the floating point dual number. Multiplication is logical for the arithmetic combination of these so selected correction factors.

The mantissa of the floating point dual number is preferably always arithmetically combined with two correction factors, in which the first correction factor is selected by the exponent (as described above) and the second correction factor by the mantissa of the floating point dual number. Addition is advantageous for the arithmetic combination of the second correction factor

with the mantissa. The second correction factor serves for the (pre-) correction of a systematic conversion error in the D/A converter itself.

If the dual number is generated in a fixed point representation, the correction factor is selected by the fixed point dual number itself. This shows that the invention is in no way limited to dual numbers in floating point representation, for a correction of systematic D/A converter errors can also be carried out with the invention through the fixed point number value.

Furthermore, the invention is based on a D/A converter arrangement for the conversion of a digital signal into an analog signal, in which the digital signal is preferably generated as a floating point dual number or fixed point dual number, and the D/A converter arrangement essentially consists of a D/A converter, the output of which is connected to the input of a switchable evaluator, which contains at least two switching stages, which may be subject to tolerance errors. The switching stages can be controlled by the exponent of the floating point dual number.

With regard to this, it is the further object of the invention to provide a D/A converter arrangement which executes an essentially reliable conversion of a digital signal to an analog signal.

In principle, this object is achieved with an above described D/A converter arrangement in that the input of the D/A converter is connected to the output of an arithmetic computational unit, which combines the dual number to be converted or the mantissa of the floating point dual number, with at least one correction factor compensating tolerance errors.

For this it is an advantage that the correction factors assigned to the switching stages are stored in a memory which can be addressed or controlled by the exponent and/or the mantissa of the floating point dual number, said memory preferably being a programmable read only memory (PROM).

Controllable memories, in particular PROMS, can be affordably obtained as reliable standard components in many different types and dimensions. Their programming is easily and directly possible as is the arrangement of the computational unit or the computational units.

Moreover, it is advantageous if the switchable evaluator consists of a resistor network which divides the output voltage of the D/A converter in steps of powers of two and the taps of which are fed to a multiplexer which can be controlled by the exponent of the floating point dual number. For this, the output of the multiplexer is preferably connected to the input of an impedance converter, the output of which represents the analog output of the D/A converter arrangement.

Furthermore, it is of advantage if a digital signal processor is provided which executes the control of the D/A converter and the switchable evaluator in the digital section of the converter arrangement, contains the memory with the correction data and the computational unit, and performs the correction of the dual number or the mantissa data and therewith a semi-automatic or fully automatic balancing and correction of the switching stage errors of the evaluator and/or the systematic errors of the D/A converter.

Further developments and advantageous arrangements of the method and the D/A converter arrangement follow from

the subclaims, the further description and embodiments shown in drawings.

The drawings show in:

Fig.1 a circuit diagram of a known D/A converter arrangement with a switchable evaluator;

Fig.2 a circuit diagram of the converter arrangement as in Fig.1 with an embodiment of a switchable evaluator;

Fig.3 a circuit diagram of a D/A converter arrangement according to the invention;

Fig.4 a circuit diagram of a D/A converter arrangement with a digital signal processor for the automatic compensation of the scaling error;

Fig.5 a flow chart for a digital signal processor for generating a floating point dual number from a fixed point dual number and the correction of the mantissa;

Fig.6 a circuit diagram of a D/A converter arrangement with a precorrection of systematic D/A conversion errors;

Fig.7 a circuit diagram with the combination of Fig.3 and Fig.6.

Fig.1 shows a D/A converter device with a conventional D/A converter 1 having a resolution of M bits which receives the mantissa of a floating point dual number with M bits on the input side. A switchable evaluator or amplifier 2 is connected downstream of the D/A

converter on the output side, is controlled by the exponent of the floating point dual number and can assume E switching conditions.

As can be seen in Fig.1, the floating point dual number is generated by means of a processing logic unit 3 from a digital signal 4 with N bits in a fixed point dual number representation. To do this, the upper E bits of the signal 4 are checked. If (in two's complement representation) the upper X bits of these E bits are the same, then the exponent takes the value E-X and the two's complement number is shifted by X-1 bits to the left (see Fig.5). Then the upper M bits of the number shifted in this way form the mantissa. If the upper two bits of the number are not equal (no bits the same), then the exponent is zero and no shifting occurs because all bits are significant (see also Fig.5).

In order to take account of the floating point dual number representation, the switchable amplification or the evaluator 2 must be capable of being switched exactly in powers of the number two, as shown in Fig. 2 ($1, 1/2, 1/4$). This arrangement then covers a range of values corresponding to a linear converter with a resolution of M+E-1 bits. For the D/A converter 1 in Fig.2 the mantissa is 16 bits, the exponent is 2 bits and the digital signal 4 is 19 bits wide. Thus, the exponent can assume a maximum of four different states. The accuracy of this representation depends very much on the accuracy and, therewith, the tolerance errors of the evaluator stages/amplifier stages.

One possibility of realising the switchable evaluator 2 is, as shown in Fig.2, a resistor network 5 which divides the output voltage of the D/A converter 1 in steps of powers of two and the individual taps of which

are fed to a multiplexer 6 (CMOS switch). The multiplexer 6 is controlled by the exponent of the floating point dual number so that the correct scaling of the converter value is always carried out. In doing this, the multiplexer 6 can assume four different switching conditions in this case (Fig.3). However, the resistors 7 of the divider network 5 must be very precise because otherwise, the analog scaling does not correspond to the conversion in the digital range when forming the floating point dual number. This accuracy was up to now achieved through a precise balancing of the resistors 7 during manufacture or through subsequent balancing during assembly, by means of trimming potentiometers 7, as shown in Fig.2. However, balancing by means of potentiometers is difficult because balancing of one potentiometer alters the entire dividing ratio of one switching stage relative to the other switching stages. The output of the multiplexer 6 is connected to the input of an impedance converter 11, the output 12 of which is in turn connected to the input of a holding element 17.

In the D/A converter arrangement shown in Fig.3, the precise balancing of the scaling stages, i.e. the resistors 13-16 of resistor network 5 in the analog section of the converter, is omitted. Instead, the mantissa value of each floating point number fed to the conventional D/A converter is matched, through multiplying by a correction factor in a multiplier 8, to the inaccurate scaling in such a way that after scaling, the correct output value results. In doing this, each of the switching stages selected by the exponent is assigned a corresponding correction factor compensating the tolerance error of this switching stage, and the factor is stored in a memory unit, in this case the read only memory 9.

Thus, instead of an analog scaling, a digital scaling is used. This process is not sensitive as regards thermal or mechanical influences and enables, in addition, simple semi-automatic or fully automatic compensation.

It is possible, for example, to determine the correction factors when assembling the network 5 and to store them in a read only memory 9 (e.g. PROM/ROM, etc.) which is addressed by the exponent E of the floating point dual number and feeds its data to the multiplier 8 which in turn corrects the mantissa data.

The arrangement of the processing logic unit 3 and read only memory 9/multiplier 8 can be replaced in an advantageous manner by a digital signal processor (DSP) 10 which takes over the decoding in exponent and mantissa and the correction in one unit, as shown in Fig.4. Fig.5 shows the flow diagram for a DSP for generating the floating point dual number from the fixed point dual number and the correction of the mantissa. Furthermore, the DSP 10 is able, through its supplementary logic circuitry (not shown), to carry out a semi-automatic or fully automatic compensation of the scaling errors via measurement results, for example, from a distortion factor analyzer or another suitable device, fed in from outside.

For this, the correction factors are altered step by step until the error in the signal is a minimum. The final values are then permanently stored. This is possible for example, in an EEPROM, EPROM or SRAM with a battery buffer.

In the following the example for a correction is described:

As shown in Fig.3, the digital signal 4 has a width of 19 bits, the mantissa 16 bits and the exponent 2 bits (all two's complement). The D/A converter has a resolution of 16 bits. The multiplier multiplies a 16-bit mantissa piece of data with a 15-bit wide correction piece of data to form a new 16-bit wide mantissa piece of data. The output voltage of the converter is 1 V with full modulation (32768).

Let it be assumed that the basic accuracy of the resistors in the divider chain is $\pm 1\%$.

The resistors 13,14 and 15 deviate by 1% upwards (sum 7.07R), the resistor 16 deviates by 1% downwards (0.99R).

The result is a divider ratio of $Tv1 = 0.99/8.06$ for the lowest stage with the exponent 0 (desired ratio $Tv=1/8$). Therefore, this stage has a deviation of -1.74%.

Calculating the correction factors:

With a fixed point multiplication, only correction factors with values < 1 are possible.

In order that deviations upwards and downwards may be corrected, the correction factor for the error-free direct stage 17 (exponent 3) is set to the value 32000. The remaining correction factors are to be calculated relative to this factor. Consequently, corrections by approx. 2% upwards are possible.

There results for all values a change in amplification of $32000/32768$ which, however, reduces only the amplitude of the signal slightly; the quality of the signals is, however, not impaired.

The correction factor for the stage 0 is thus calculated as $K_0 = K_3 * T_{v0} / T_i = 32000 * 8.06 / 0.99 / 8 = 32566$ (rounded to 15 bits).

For the input piece of data 32767 it follows:
mantissa = 32767; exponent = 0

The mantissa must be multiplied with the factor $K_0 = 32566$. With a fixed point multiplication with subsequent cutting to 16 bits, the value 32565 results for the converter. The output voltage generated is 0.993804932 V.

This voltage is now divided by the divider stage 0 to 0.122067851.

The desired value for the output (taking into account the correction factor for stage 3 which manifests itself by way of a change in the amplification) is
 $32767 / 8 * 1V / 32768 * 32000 / 32768 = 0.122066587$ V.

The error, with reference to the full modulation, is -0.0001265% (= 19 bits).

If it is now assumed that the D/A converter itself also carries out a systematically faulty conversion of some or all of the digital signals - these faults are designated as systematic errors - then such a faulty conversion may be avoided also with the principle of the invention, namely the digital pre-compensation. In doing this, the type of digital signal is unimportant, also the correction of the digital signals is not limited to a particular representation of the dual numbers.

As shown in Fig.6, the mantissa value or the fixed point number value is used for addressing a memory. In the memory, suitable correction factors for all D/A conversion errors are stored and, via a corresponding addressing, the appropriate correction factors are selected by the incoming digital signal. The correction factors chosen are combined with a selected mantissa value or fixed point number value in a further arithmetic computational unit 21. It is logical for this combination to be an addition and/or a subtraction. Thus a mantissa value or fixed point number value preset correspondingly to errors of the D/A converter is fed to the D/A converter so that the analog value at the output of the D/A converter corresponds exactly with the digital value at the input of the circuit in Fig.6.

Finally, Fig.7 illustrates a combination of the two correction types described above, in which the computational unit 21 can be located in the signal path to the D/A converter before or after the computational unit. It is very useful if a common computational unit takes over the task of the above-mentioned computational units and precompensates digital signals to be corrected for errors in the D/A converter arrangement by means of multiplication and/or addition/subtraction using selected correction factors so that a highly accurate analog value is available at the output of the circuit.

The enumeration of the errors in the D/A converter arrangement is in no way complete. By using the invention, further errors, not mentioned here, in the D/A to-analog converter arrangement can also be corrected. Further, the method of the invention and the device are not limited to the conversion of a single

digital signal; on the contrary, they can be used in the conversion of a multitude of digital data or a digital data stream.



Claims

1. A method for converting a digital signal to an analog signal by means of a D/A converter arrangement to which the digital number is fed, in which the digital signal is generated as a fixed point dual number and the D/A converter arrangement may be subject to a systematic conversion error which can be compensated by a correction factor, characterised in that the D/A converter arrangement consists of a single D/A converter (1) and in that before the D/A conversion the entire fixed point dual number is arithmetically combined with the correction factor compensating the conversion error, the correction factor being selected by the entire fixed point dual number.
2. A method according to claim 1, characterised in that the correction factor is stored and is in each case assigned to at least one fixed point dual number.
3. A method for converting a digital signal to an analog signal by means of a D/A converter arrangement to which the digital signal is fed, in which the D/A converter arrangement may be subject to a tolerance error and the digital signal is generated as a floating point dual number consisting of a mantissa and an exponent on the base of a power of two with E conditions, characterised in that the mantissa of the floating point dual number is arithmetically combined with at least one correction factor compensating tolerance errors, on which the correction factor is selected by the whole exponent.
4. A method according to claim 3, characterised in that the mantissa of the floating point dual number is arithmetically combined with two correction factors, in which the first correction factor is selected by the



exponent and the second correction factor by the mantissa of the floating point dual number.

5. A method according to claim 4, characterised in that a multiplication is performed to combine the first correction factor with the mantissa, and in that an addition is performed to combine the second correction factor with the mantissa.

6. A D/A converter arrangement (1,2) for executing the process according to any one of claims 1-5, characterised in that the input of a D/A converter (1) is connected to the output of a first and/or second arithmetic computational unit (8,21) which combines a digital signal to be converted with at least one correction factor compensating a tolerance error and/or a systematic conversion error, in which the digital signal is generated as a fixed point or floating point dual number and in which the correction factor is selected by the entire exponent or by the entire fixed point dual number.

7. A D/A converter arrangement according to claim 6, characterised in that the correction factors are stored in an addressable memory (9,20) which can be addressed by the digital signal itself and the correction factor assigned to a digital signal can be selected by the digital signal itself.

8. A D/A converter arrangement according to claim 6 or 7 but excluding 1 and 2, characterised in that the digital signal is generated as a floating point dual number which consists in each case of a mantissa and an exponent on the base of a power of two with E conditions, and in that the D/A converter arrangement consists of a D/A converter (1) which may be subject to



systematic conversion errors and the output of which is connected to the input of a switchable evaluator (2) containing at least two switching stages which may be subject to tolerance errors, and in that the input of the D/A converter (1) is connected to the output of the first arithmetic computational unit (8) which combines the mantissa of the floating point dual number with at least one correction factor compensating tolerance errors.

9. A D/A converter arrangement according to claim 8, characterised in that the correction factors are stored in a memory (9,20) which can be addressed or controlled by the exponent and/or the mantissa of the floating point dual number, said memory preferably being a programmable read only memory (PROM).

10. A D/A converter arrangement according to claim 8 or 9, characterised in that the switchable evaluator (2) consists of a resistor network (5) which divides the output voltage of the D/A converter in steps of powers of the base of the exponent and the taps of which are fed to a multiplexer (6) which can be controlled by the exponent of the floating point dual number.

11. A D/A converter arrangement according to claim 10, characterised in that the output of the multiplexer (6) is connected to the input of an impedance converter (11), and in that the output of the impedance converter is connected to a holding element (17).

12. A D/A converter arrangement according to any one of claims 7-11, characterised in that a digital signal processor (10) is provided which performs a semi-automatic or fully automatic compensation of the switching stage errors in the digital section of the



converter arrangement and contains the first and/or second arithmetic computational unit (8,21) and the addressable or controllable memory (9,20).

13. A D/A converter arrangement according to any one of claims 7-12, characterised in that the memory (9) is controlled by the exponent of the floating point dual number which selects the first correction factor which is combined through multiplication in the first computational unit (8) with the mantissa of the floating point dual number, and/or in that the mantissa of the floating point dual number selects the second correction factor from the addressable or controllable memory (20) which can be supplied through addition to the mantissa of the floating point dual number in the second computational unit (21).

14. A D/A converter arrangement according to claim 13, characterised in that the second arithmetic computational unit (21) is located in the signal path to the D/A converter before or after the first arithmetic computational unit (8).