WRITE COPYING METHOD, PROCESSOR CORE, STORAGE CONTROLLER, AND COMPUTER SYSTEM AND DEVICE

[0001] This application claims priority to Chinese Patent Application No. 202310006110.8, filed with the China National Intellectual Property Administration on January 04, 2023 and entitled "WRITE COPYING METHOD, PROCESSOR CORE, STORAGE CONTROLLER, AND COMPUTER SYSTEM AND DEVICE", which is hereby incorporated by reference in its entirety.

TECHNICAL FIELD

[0002] Embodiments of the present application relate to the field of chip technologies and, in particular, to a write copying method, a processor core, a storage controller, and a computer system and device.

BACKGROUND

[0003] In a computer system architecture, since a storage is taken as an important component for storing data, it is necessary to provide a storage fault-tolerant mechanism to reduce the probability of loss of the data when writing to the storage due to faults or other reasons. Write copying, as an important technique of the storage fault-tolerant mechanism, can copy a write operation (the write operation is used to write data to the storage); thus, on the basis of saving the data written by the write operation in the storage, the copying the write operation is further utilized to save mirror data in the storage; and then the storage can utilize the mirror data to achieve data backup, reducing the probability of loss of the data written to the storage.

[0004] In the computer system architecture, a component that initiates a write

operation to the storage may be a processor core or an extended PCIE (Peripheral Component Interconnect Express) device. In this context, how to implement write copying for a write operation initiated by a processor core has become an urgent technical problem that needs to solved by those skilled in the art.

SUMMARY

[0005] In view of this, embodiments of the present application provide a write copying method, a processor core, a storage controller, and a computer system and device, so as to implement write copying for a write operation initiated by a processor core, and reduce usage limitations of write copying.

[0006] To achieve the above purposes, embodiments of the present application provide the following technical solutions.

[0007] In a first aspect, an embodiment of the present application provides a write copying method, applied to a processor core, where the method includes:

initiating a write operation, where the write operation indicates at least a write address and write data; determining whether existing a target address range that matches the write address in an address range indicated by a mirror address table; where the mirror address table is set in the processor core; the mirror address table indicates at least one address range where write copying is allowed, and indicates a mirror address corresponding to each address range; a type of a storage pointed to by the address range is the same as or different from a type of a storage pointed to by the mirror address corresponding to the address range; the type of the storage is a memory and an extended storage; if the target address range that matches the write address exists, determining, according to a target mirror address corresponding to the target address range, a destination address of a copy write operation; where a type of a storage pointed to by the write address is the same as or different from a type of a storage pointed to by the destination address; generating, according to the destination address, the copy write operation, where the copy write operation is used to write mirror data of the write data at the destination address; and issuing the write operation

and the copy write operation.

[0008] In a second aspect, an embodiment of the present application provides a write copying method, applied to a first storage controller, where the first storage controller controls a first storage, and the method includes:

obtaining a write operation of a processor core to the first storage; where the write operation indicates at least write data and a write address of the write data in the first storage; determining whether existing a target address range that matches the write address in an address range indicated by a mirror address table; where the mirror address table is set in the first storage controller, the mirror address table indicates at least one address range where write copying is allowed in the first storage, and indicates a mirror address corresponding to each address range; where a type of a storage pointed to by the mirror address corresponding to the address range is the same as or different from a type of the first storage; the type of the storage is a memory and an extended storage; determining, according to a target mirror address corresponding to a target address range, a destination address of a copy write operation; where a type of a storage pointed to by the destination address is the same as or different from a type of the first storage; generating, according to the destination address of the copy write operation, the copy write operation, where the copy write operation is used to write mirror data of the write data at the destination address; and performing the write operation and processing the copy write operation.

[0009] In a third aspect, an embodiment of the present application provides a processor core, where the processor core is configured with a mirror address table, the mirror address table indicates at least one address range where write copying is allowed, and indicates a mirror address corresponding to each address range; a type of a storage pointed to by the address range is the same as or different from a type of a storage pointed to by the mirror address corresponding to the address range; the type of the storage is a memory and an extended storage; and the processor core is configured to perform the write copying method as described in the first aspect.

[0010] In a fourth aspect, an embodiment of the present application provides a storage controller, where the storage controller controls a first storage; the storage

controller is configured with a mirror address table, the mirror address table indicates at least one address range where write copying is allowed in the first storage, and indicates a mirror address corresponding to each address range; a type of a storage pointed to by the mirror address corresponding to the address range is the same as or different from a type of the first storage; the type of the storage is a memory and an extended storage; and the storage controller is configured to perform the write copying method as described in the second aspect.

[0011] In a fifth aspect, an embodiment of the present application provides a computer system, including: the processor core as described in the third aspect, a memory controller, a memory controlled by the memory controller, an expansion controller, and an extended storage controlled by the expansion controller.

[0012] In a sixth aspect, an embodiment of the present application provides a computer device, including: the computer system as described in the fifth aspect.

[0013] The above overview is only for the purpose of the specification and is not intended to limit thereto in any way. In addition to the illustrative aspects, implementations, and features described above, further aspects, implementations, and features of the present application will be easily understood by referring to the accompanying drawings and the following detailed description.

BRIEF DESCRIPTION OF DRAWINGS

[0014] In the accompanying drawings, unless otherwise specified, the same reference numbers throughout multiple accompanying drawings represent the same or similar components or elements. These accompanying drawings may not necessarily be drawn to scale. It should be understood that these accompanying drawings only depict some implementations disclosed according to the present application, and should not be regarded as limiting the scope of the present application.

[0015] FIG. 1 is a block diagram of a computer system architecture.

[0016] FIG. 2 is an example diagram of a mirror address table provided in an embodiment of the present application.

[0017] FIG. 3 is another example diagram of a mirror address table provided in an embodiment of the present application.

[0018] FIG. 4 is a flowchart of a write copying method provided in an embodiment of the present application.

[0019] FIG. 5A is an implementation example diagram of write copying method provided in an embodiment of the present application.

[0020] FIG. 5B is another implementation example diagram of a write copying method provided in an embodiment of the present application.

[0021] FIG. 5C is a further implementation example diagram of a write copying method provided in an embodiment of the present application.

[0022] FIG. 5D is a yet another implementation example diagram of a write copying method provided in an embodiment of the present application.

[0023] FIG. 6 is another flowchart of a write copying method provided in an embodiment of the present application.

[0024] FIG. 7 is a still another implementation example diagram of a write copying method provided in an embodiment of the present application.

[0025] FIG. 8 is a still further implementation example diagram of a write copying method provided in an embodiment of the present application.

DESCRIPTION OF EMBODIMENTS

[0026] In order to make the above purposes, features, and advantages of the present application more obvious and understandable, the technical solutions in embodiments of the present application will be clearly and completely described in conjunction with the accompanying drawings of the present application. Obviously, the described embodiments are only a part of the embodiments of the present application, not all of them. Based on the embodiments in the present application, all other embodiments obtained by those of ordinary skill in the art without creative effort are within the protection scope of the present application.

[0027] For the convenience of understanding the computer system architecture,

FIG. 1 exemplarily illustrates an optional block diagram of the computer system architecture, where the computer system architecture may be, for example, a chip structure. A chip is an integrated circuit that integrates important components in the computer device, in an optional implementation, a processor core, a memory controller, a PCIE controller and other important devices in the computer device can be integrated in the chip.

[0028] In some implementations, the computer system architecture shown in FIG. 1 may consist of a plurality of different functional tiles, where these functional tiles include: a processor core, a memory controller, a PCIE controller, a UPI (Ultra Path Interconnect), a CHA (Caching and Home Agent), a SF (Snoop Filter), a LLC (Last Level Cache), etc.

[0029] As shown in FIG. 1, there can be a plurality of processor cores 110 in the computer system architecture, and the plurality of processor cores 110 can be connected via a bus. In an optional implementation, the plurality of processor cores 110 can be connected via a Mesh bus. For example, the plurality of processor cores 110 are connected via a Mesh structure, and each processor core 110 is located at a mesh intersection of the Mesh bus and is distributed in a mesh like pattern. In an implementation example, each processor core can be distributed into functional tiles in a distributed manner, and the functional tiles of each processor core are organized and connected through a Mesh architecture. It should be noted that the number of the plurality of processor cores 110 can be determined according to the architectural design of the computer system architecture, which is not limited in embodiments of the present application.

[0030] Furthermore, as shown in FIG. 1, each processor core 110 is paired with the CHA, the SF, and the LLC, such as L3 cache. In an implementation example, under the connection architecture of the Mesh bus, one CHA, one SF, and one LLC can be paired with functional tiles of a processor core to form a node and be attached to the Mesh bus.

[0031] It should be noted that the processor core as well as the CHA, the SF, and the LLC paired with the processor core can be considered as core components in the

computer system architecture. In addition to the aforementioned core components, the computer system architecture can also have non-core components. Further combining with FIG. 1, the computer system architecture can be provided with at least one memory controller 120, at least one PCIE controller 130, and at least one UPI 140 and other non-core components in the form of functional tiles.

[0032] Where the memory controller 120 is an optional form of a storage controller, which can control memory and is used to control memory and be responsible for data exchange between the memory and the processor core. The number of the memory controller 120 can be one or more, and one memory controller 120 can control one or more memories. The PCIE controller 130 is another optional form of the storage controller, which can be connected to a PCIE EP (End Point) and other PCIE storages to achieve data reading and writing in the PCIE storage. The number of the PCIE controller 130 can be one or more, and one PCIE controller 130 can control one or more PCIE storages. The PCIE controller 130 can be, for example, a PCIE root complex. UPI can be regarded as a consistent interconnect component in the computer system architecture, which can provide high-speed and low latency data transmission between processor cores. The quantity of the UPI can be one or more.

[0033] It should be noted that PCIE is only one type of extension bus standard supported by the computer system architecture, and the computer system architecture can also support other forms of extension bus standards. Based on the expansion bus standard, the computer system architecture can be provided with a corresponding expansion device (such as a PCIE device), a corresponding expansion controller (such as a PCIE controller), and a corresponding extended storage (such as a PCIE storage).

[0034] It should be further noted that the computer system architecture shown in FIG. 1 is only an optional example, and embodiments of the present application may also support other forms of computer system architectures.

[0035] From the above introduction, it can be seen that in the computer system architecture, the storage can be a memory and an extended storage, where the extended storage can be, for example, the PCIE storage, etc. Correspondingly, the write operation to the storage may be a write operation to the memory or a write

operation to the extended storage (such as a write operation to the PCIE storage). The write operation to the memory can be regarded as a write operation to write data to the memory, and a write address of the write operation belongs to a memory address. The write operation to the extended storage can be regarded as a write operation to write data to the extended storage (such as a write operation to write data to the PCIE storage), and a write address of the write operation belongs to a storage address of the extended storage.

[0036] In some implementations, for the write operation to the memory, the write copying manner for implementing the write copying may be as follows.

[0037] Based on the memory being controlled by the memory controller, control logic is added to the memory controller. When the processor core initiates a write operation that writes data to the memory, the memory controller can obtain the write operation and copy the write operation to obtain a copy write operation. Therefore, when writing the write data corresponding to the write operation to the memory, the memory controller can additionally write mirror data of the copy write operation to the memory, thereby achieving data backup in the memory.

[0038] However, there are usage limitations of the above write copying manner: the write copying in the above write copy manner is implemented by the memory controller, therefore, the above write copy manner is only applicable to the case where the write operation initiated by the processor core is for the memory (that is, the write address of the write operation initiated by the processor core belongs to the memory address), and is not applicable to the case where the processor core initiates a write operation to an extended storage such as a PCIE storage (that is, the write address of the write operation initiated by the processor core cannot belong to the storage address of the extended storage). And the mirror data of the above write copying manner can only be saved in the memory and cannot be saved in the extended storage.

[0039] It can be seen that there are usage limitations of the write operation manner in the above example for the write operation initiated by the processor core (the write operation initiated by the processor core may target the memory or the extended storage such as the PCIE storage). Based on this, an embodiment of the present

application provides an improved write copying scheme, where through setting a mirror address table (mirror addr tbl) in the processor core, write copying is performed on the write operation initiated by the processor core when the write address of the write operation is within an address range where the write copying is allowed as indicated by the mirror address table, and the destination address of the copy write operation is determined. The write copying scheme provided in an embodiment of the present application can reduce the usage limitations of write copying through configuring the mirror address table, without limiting whether the write operation initiated by the processor core is directed to the memory or the extended storage, and without limiting whether the destination address of the copy write operation points to the memory or the extended storage.

[0040] As an optional implementation, an embodiment of the present application can configure a mirror address table (mirror addr tbl) to determine whether the write address of the write operation initiated by the processor core is within the address range where the write copying is allowed; if the write address of the write operation initiated by the processor core is within the address range where the write copying is allowed as indicated by the mirror address table, an embodiment of the present application can perform write copying on the write operation initiated by the processor core, and determine the destination address of the copy write operation based on the mirror address configured in the mirror address table.

[0041] Under the above concepts, an embodiment of the present application can reduce the restriction between the write address of the write operation and the destination address of the copy write operation through configuring the mirror address table. For example, if the write address of the write operation points to the memory, the destination address of the copy write operation can point to the extended storage such as the PCIE storage, or to the memory. For another example, if the write address of the write operation points to the extended storage, the destination address of the copy write operation can be either to the extended storage or to the memory. That is, the destination address of the copy write operation is no longer limited to the storage pointed to by the write address of the write operation, but is determined by the mirror

address table. Thereby, through configuring the mirror address table, it is possible to make the write address of the write operation and the destination address of the copy write operation change arbitrarily between the memory address and the storage address of the extended storage, thereby reducing the usage limitations of the write copying technique for the write operation initiated by the processor core. The types of the storage referred to in the embodiment of the present application can be the memory and the extended storage (such as the PCIE storage) and other types of storages.

[0042] As an optional implementation, the mirror address table can indicate at least the address range where the write copying is allowed, and indicate the corresponding mirror address, where the mirror address is used to determine the destination address of the copy write operation. Therefore, for the write operation initiated by the processor core, an embodiment of the present application can determine whether the write address of the write operation is within the address range where the write copying is allowed as indicated by the mirror address table; if so, an embodiment of the present application can determine the destination address of the copy write operation according to the corresponding mirror address, and generate the copy write operation based on the destination address of the copy write operation, thereby achieving the write copying of the write operation initiated by the processor core.

[0043] In some implementations, FIG. 2 illustrates an optional example diagram of a mirror address table provided in an embodiment of the present application. As shown in FIG. 2, the mirror address table can include at least one table entry record, one table entry record can indicate an address range where write copying is allowed and a corresponding mirror address. Therefore, for the write operation initiated by the processor core, an embodiment of the present application can determine whether existing a table entry record with an address range that matches the write address in the mirror address table; if so, an embodiment of the present application can determine that the write address of the write operation is within the address range where the write copying is allowed as indicated by the mirror address table. Thus, an

embodiment of the present application can determine the destination address of the copy write operation based on the mirror address indicated by the matched table entry record, and generate the copy write operation based on the destination address of the copy write operation, thereby achieving the write copying of the write operation initiated by the processor core.

[0044] To reduce the usage limitation of write copying technology on the write operation initiated by the processor core, as an optional implementation, an embodiment of the present application can configure the mirror address table without restricting the address range indicated by the table entry record and the type of the storage pointed to by the mirror address. That is, the address range of any type of storage and the mirror address of any type of storage can be recorded in the same table entry record.

[0045] In some implementations, the address range indicated by the mirror address table can be determined by a source address and a total address length, for example, an address range obtained by combining the source address and the total address length is the address range of the write copying indicated by the mirror address table. Thus, any table entry record in the mirror address table can be composed of the source address, the total address length, and the mirror address. Under this concept, as an optional implementation, FIG. 3 exemplarily illustrates another optional example diagram of a mirror address table provided in an embodiment of the present application. As shown in FIG. 3, the mirror address table can include a source address (src_add) field, a mirror address (dst_dedr) field, and a total address length (len) field. The source address field can record the source address that allows write copying; the total address length field can record the total length of the address that allows write copying, so that the source address and the total address length determine the address range where the write copying is allowed; and the mirror address field can record the mirror address of the copy write operation, which is used to generate the destination address of the copy write operation.

[0046] The mirror address table can have a plurality of table entry records, each table entry record records one source address of the source address field, one total

address length of the total address length field, and one mirror address of the mirror address field. That is, one table entry record records one source address, one total address length, and one mirror address. At least one of the source address, the total address length, and the mirror address recorded in different table entry records is mutually different, and a plurality of table entry records form the mirror address table.

[0047] An embodiment of the present application can configure the mirror address table through configuring the source address, the total address length, and the mirror address recorded in each table entry record of the mirror address table. To reduce the usage limitation of write copying technology on the write operation initiated by the processor core, as an optional implementation, an embodiment of the present application can configure the mirror address table without restricting the type of the storage pointed to by the source address and mirror address. That is, the source address of any type of storage and the mirror address of any type of storage can be recorded in the same table entry record. Optionally, the storage can be a memory and an extended storage based on the type of storage. For any table entry record in the mirror address table, an embodiment of the present application can set the source address belong to any one of the memory address and the storage address of the extended storage, and the mirror address belong to any one of the memory address and the storage address of the extended storage. That is, in a possible implementation, the write operation of the processor core to the memory may be copied as a copy write operation to the extended storage, or as a copy write operation to the memory, which depends on the configuration purpose and specific configuration of the mirror address table, and is not limited in embodiments of the present application. In other possible implementations, the write operation of the processor core to the extended storage may be copied as a copy write operation to the memory, or as a copy write operation to the extended storage, which depends on the configuration purpose and the specific configuration of the mirror address table, and is not limited in embodiments of the present application.

[0048] After completing the configuration of the mirror address table, as an optional implementation, the mirror address table can be set in the processor core, so

that when initiating a write operation, the processor core can determine whether the write copying can be performed on the write operation through the internally set mirror address table; and, the processor core can determine the destination address of the copy write operation through the mirror address table when the write copying can be performed on the write operation. Optionally, FIG. 4 exemplarily illustrates an optional flowchart of a write copying method provided in an embodiment of the present application, which can be implemented by the processor core. Referring to FIG. 4, the method flowchart may include the following steps.

[0049] In step S410, initiating a write operation, where the write operation indicates at least a write address and write data.

[0050] When writing data to the storage, the processor core can initiate the write operation to the storage, and the write operation can indicate the write address of the storage and the write data written at the write address.

[0051] In some implementations, the write operation initiated by the processor core can be the write operation to the memory. For example, when writing data to the memory, the processor core can initiate the write operation to the memory; correspondingly, the write address of the write operation belongs to the memory address of the memory. It should be noted that the write operation of the processor core to the memory can be transmitted to the memory controller through a bus (such as a Mesh bus) for the memory controller to perform the write operation.

[0052] In some implementations, the write operation initiated by the processor core can be the write operation to the extended storage (such as the PCIE storage). For example, when writing data to the extended storage, the processor core can initiate the write operation to the extended storage; correspondingly, the write address of the write operation belongs to the storage address of the extended storage. It should be noted that the write operation of the processor core to the extended storage can be transmitted to the expansion controller through a bus (such as a Mesh bus) for the expansion controller to perform the write operation. For example, the write operation of the processor core to the PCIE storage can be transmitted to the PCIE controller through a Mesh bus for the PCIE controller to perform the write operation to the PCIE

storage.

[0053] In step S411, determining whether existing a target address range that matches the write address in an address range indicated by a mirror address table; if so, performing step S412, if not, performing step S415.

[0054] In some implementations, the mirror address table is set in the processor core; the mirror address table indicates at least one address range where write copying is allowed, and indicates a mirror address corresponding to each address range; where a type of a storage pointed to by the address range is the same as or different from a type of a storage pointed to by the mirror address corresponding to the address range.

[0055] When initiating the write operation, the processor core can determine whether existing a target address range that matches the write address based on the address range indicated by the mirror address table; for example, determine whether the write address of the write operation is within any address range where the write copying is allowed (for ease of explanation, the address range that matches the write address can be referred to as the target address range). If there is a target address range that matches the write address in the address range indicated by the mirror address table, it indicates that the write copying can be performed on the write operation. If there is no a target address range that matches the write address in the address range indicated by the mirror address table, it indicates that the write copying can not be performed on the write operation.

[0056] Based on the previous description, the address range indicated by the mirror address table is used to match the write address of the write operation. Therefore, when the write copying is allowed for the write operation, the target address range points to the storage targeted by the write operation, while the mirror address is used to determine the destination address of the copy write operation. Therefore, the mirror address corresponding to the target address range points to the storage targeted by the copy write operation. Based on this, in order to reduce the usage limitations of the write copying, embodiments of the present application do not restrict the storage targeted by the write operation and the storage targeted by the copy write operation, which can be configured by a designer for the computer system

architecture or a user of the computer device according to the specific goal of the write copying. For example, the designer for the computer system architecture or the user of the computer device can configure, in the mirror address table, the storage type pointed to by the address range and the storage type pointed to by the mirror address corresponding to the address range, without limiting the storage type pointed to by the address range and the mirror address. That is, the designer for the computer system architecture or the user of the computer device can configure the storage type pointed to by the address range in the mirror address table according to the specific target of the write copying, which is the same as or different from the storage type pointed to by the mirror address corresponding to the address range.

[0057] It can be understood that if the storage type pointed to by the address range is the same as the storage type pointed to by the mirror address corresponding to the address range, it means that the write operation and the copy write operation target the same storage type. For example, both the write operation and the copy write operation target the memory or the extended storage. If the storage type pointed to by the address range is different from the storage type pointed to by the mirror address corresponding to the address range, it means that the write operation and the copy write operation target different storage types. For example, the write operation targets the memory, and the copy write operation targets the extended storage. For another example, the write operation targets the extended storage, and the copy write operation targets the memory.

[0058] In some implementations, as shown in FIG. 2, the mirror address table can include at least one table entry record, one table entry record indicates an address range where write copying is allowed and a corresponding mirror address. Based on this, in some implementations of performing step S411, an embodiment of the present application can search for each table entry record in the mirror address table according to the write address of the write operation, and determine whether existing a target table entry record with an address range that matches the write address. That is, an embodiment of the present application can determine whether the write address of the write operation is within the address range indicated by any table entry record; if the

write address of the write operation is within an address range indicated by a certain table entry record in the mirrored address table, it can be confirmed that the write copying is allowed for the write operation (accordingly, this table entry record can be referred to as the target table entry record, and the address range indicated by the target table entry record is a target address range that matches the write address); otherwise, it can be confirmed that the write copying is not allowed for the write operation.

[0059] In some implementations, as shown in FIG. 3, the address range indicated by the table entry record can be determined by the source address and the total address length. Correspondingly, one table entry record can record one source address, one total address length, and one mirror address; and the source address and the total address length in the table entry record determine the address range where the write copying is allowed as indicated by the table entry record. Based on this, an embodiment of the present application can determine the address range indicated by each table entry record according to the source address and the total address length recorded in each table entry record; where the source address of the table entry record is a starting address of the address range indicated by the table entry record, an address obtained by combining the source address and the total address length of the table entry record is an ending address of the address range indicated by the table entry record; thus, an embodiment of the present application can determine whether existing a target table entry record with an address range that matches the write address according to the address range indicated by each table entry record; so as to determine whether existing a target table entry record with an address range that matches the write address in the mirror address table.

[0060] In some implementations, for any table entry record in the mirror address table, the source address in the table entry record can be used as a starting address indicated by the table entry record, and an address obtained by combining the source address and the total address length in the table entry record can be used as an ending address indicated by the table entry record. Thus, the address range formed by the starting address and the ending address indicated by the table entry record can be used

as the address range where the write copying is allowed as indicated by the table entry record. For ease of understanding, if the source address of the table entry record is defined as src_addr, and the total address length is defined as len, then the address range formed by [src_addr, src_addr+len] is the address range where the write copying is allowed as indicated by the table entry record. For the write operation initiated by the processor core, the processor core can search for each table entry record in the mirror address table, compare and match the write address of the write operation with the address range [src_addr, src_addr+len] indicated by each table entry record; if the write address is within the address range indicated by a certain table entry record, the write address of the write operation hits the mirror address table; correspondingly, the table entry record corresponding to the address range that matches the write address can be referred to as the target table entry record, and the address range that matches the write address can be referred to as the target address range.

[0061] In some implementations, the address range where the write copying is allowed can be an address range where user sensitive data and user critical data are stored in the storage. The address range where the write copying is allowed as indicated by the mirror address table can be determined according to the needs of the designer or the user of the computer system architecture, which is not limited in this embodiment of the present application.

[0062] In step S412, determining, according to a target mirror address corresponding to a target address range, a destination address of a copy write operation; where a type of a storage pointed to by the write address is the same as or different from a type of a storage pointed to by the destination address.

[0063] The judgment result based on step S411 is yes (that is, there is a target address range that matches the write address in the mirror address table), an embodiment of the present application can confirm that the write copying is allowed for the write operation initiated by the processor core. At this time, an embodiment of the present application can copy the write operation to obtain the copy write operation. In order to obtain the copy write operation, an embodiment of the present application

needs to determine the destination address of the copy write operation. As an optional implementation, the destination address of the copy write operation can be determined by the target mirror address corresponding to the target address range (for ease of explanation, in an embodiment of the present application, the mirror address corresponding to the target address range is referred to as the target mirror address). Therefore, an embodiment of the present application can determine the target mirror address corresponding to the target address range from the mirror address table, and determine the destination address of the copy write operation according to the target mirror address.

[0064] In some implementations, it is assumed that the mirror address table records n table entry records, each table entry records one source address src_addr, one total address length len, and one mirror address dst_dedr, and the address range where the write copying is allowed as indicated by each table entry record is [src_addr, src_addr+len]; if the write address of the write operation is within an address range indicated by a table entry record k (k belongs to 1 to n), the table entry record k is the target address range, the address range indicated by entry record k is the target address range, and the mirror address indicated by the table entry record k is the target mirror address. Therefore, an embodiment of the present application can determine the destination address of the copy write operation according to the target mirror address indicated by the table entry record k.

[0065] As an optional implementation, an embodiment of the present application can determine the destination address of the copy write operation according to the target mirror address, the write address, and the source address recorded in the target table entry record; for example, the destination address of the copy write operation is obtained by adding the target mirror address to the write address, and subtracting the source address indicated by the target table entry record. In an implementation example, it is assumed that the table entry record k is the target table entry record, an embodiment of the present application can add the target mirror address dst_addr indicated by the target table entry record k to the write address raw_addr, and then subtract the source address src_addr indicated by the target table entry record k from

it, so as to obtain the destination address dest_addr of the copy write operation. For example, the destination address of the copy write operation dest_addr="target mirror address dst_addr"+"write address raw_addr" - "source address src_addr".

[0066] It should be noted that since the address range indicated by the table entry record is used to compare and match with the write address of the write operation, when there is a target address range that matches the write address, the write address points to the same storage as that pointed to by the target address range. Furthermore, when configuring the mirror address table, an embodiment of the present application does not limit the storage type pointed to by the address range recorded in each table entry record and the storage type pointed to by the mirror address corresponding to the address range; thus, when determining the destination address of the copy write operation, an embodiment of the present application does not limit to the storage type pointed to by the write address or the storage type pointed to by the destination address, adaptively. That is, the type of storage pointed to by the write address of the write operation can be the same as or different from the type of storage pointed to by the destination address of the copy write operation.

[0067] For example, if the write address of the write operation points to the memory, an embodiment of the present application does not limit whether the destination address of the copy write operation points to the extended storage or the memory, which depends on the configuration target and the configuration purpose of the mirror address table. For another example, if the write address of the write operation points to the extended storage, an embodiment of the present application does not limit whether the destination address of the copy write operation points to the memory or the extended storage, which depends on the configuration target and the configuration purpose of the mirror address table.

[0068] In step S413, generating, according to the destination address of the copy write operation, the copy write operation, where the copy write operation is used to write mirror data of the write data at the destination address.

[0069] After determining the destination address of the copy write operation, an embodiment of the present application can generate the copy write operation that

writes mirror data to the destination address based on the destination address. Since the storage type pointed to by the write address can be the same as or different from the storage type pointed to by the destination address, the storage type targeted by the write operation can be the same as or different from the storage type targeted by the copy write operation. It should be noted that the generated copy write operation can be used to write mirror data at the destination address, where the mirror data, for example, is copied data of the write data.

[0070] In step S414, issuing the write operation and the copy write operation.

[0071] In some implementations, the processor core can issue the write operation to write data at the write address. At the same time, the processor core can issue the copy write operation after generating the copy write operation to write the mirror data at the destination address. In an embodiment of the present application, the processor core can issue the write operation and the copy write operation via a bus (such as a Mesh bus), and the storage types pointed to by the write operation and the copy write operation can be the same or different, the processor core can transmit the write operation and the copy write operation to the same storage controller or different storage controllers via the bus. For example, if the write operation is targeted for the memory and the copy write operation is targeted for the PCIE storage, the processor core can transmit the write operation to the memory controller and transmit the copy write operation to the PCIE controller via the bus. Of course, the write operation can also be targeted for the PCIE storage, while the copy write operation is targeted for the memory. It is also possible that both the write operation and the copy write operation are targeted for the memory or the PCIE storage.

[0072] In step S415, issuing the write operation.

[0073] The judgment result based on step S411 is not (that is, there is no target address range that matches the write address in the mirror address table), an embodiment of the present application can confirm that the write copying is not allowed for the write operation initiated by the processor core; at this time, the processor core can issue the write operation to write the write data at the write address.

[0074] The write copying method provided in an embodiment of the present application can configure the mirror address table, the mirror address table can indicate at least one address range where the write copying is allowed, and the mirror address corresponding to each address range, and the mirror address is used to determine the destination address of the copy write operation; and, when configuring the mirror address table, an embodiment of the present application can configure the type of storage pointed to by the address range, which is the same as or different from the type of storage pointed to by the mirror address corresponding to the address range, and the type of storage is the memory and the extended storage. Therefore, the embodiments of the present application can support copying the write operation for any type of storage into the copy write operation for any type of storage, that is, the storage types pointed to by the write operation and the copy write operation can be the same or different, thereby reducing the usage limitations of the write copying.

[0075] Based on this, for the write operation initiated by the processor core, an embodiment of the present application can determine whether existing a target address range that matches the write address of the write operation in the address range where the write copying is allowed indicated by the mirror address table; if so, it indicates that the write copying can be allowed for the write operation, so that the embodiment of the present application can determine the destination address of the copy write operation according to the mirror address corresponding to the target address range; the storage types pointed to by the write operation and the copy write operation can be the same or different, thus, the type of storage pointed to by the write address of the write operation can be the same as or different from the type of storage pointed to by the destination address of the copy write operation; then an embodiment of the present application can generate, according to the destination address of the copy write operation, the copy write operation for writing mirror data at the destination address. After generating the copy write operation, an embodiment of the present application can issue the write operation and the copy write operation, so as to write the write data at the write address indicated by the write operation and write the mirror data at the destination address indicated by the copy write operation, thereby achieving the write

copying for the write operation.

[0076] The solution provided in an embodiment of the present application can support copying the write operation for any type of storage into the copy write operation for any type of storage through configuring the mirror address table; thus, for the write operation initiated by the processor core, if the write copying is allowed for the write operation, an embodiment of the present application can copy the write operation to obtain the copy write operation, and make that the type of storage pointed to by the write address of the write operation is the same as or different from the type of storage pointed to by the destination address of the copy write operation, thereby achieving the write copying for the write operation initiated by the processor core, and reducing the usage limitations of the write copying.

[0077] Since an embodiment of the present application supports copying the write operation for any type of storage into the copy write operation for any type of storage, there may be the following several possible situations for write copying in an embodiment of the present application.

[0078] Situation 1: the write operation is targeted for the memory, and the copy write operation is targeted for the extended storage.

[0079] Situation 2: the write operation is targeted for the extended storage, and the copy write operation is targeted for the memory.

[0080] Situation 3: the write operation is targeted for the memory, and the copy write operation is also targeted for the memory.

[0081] Situation 4: the write operation is targeted for the extended storage, and the copy write operation is also targeted for the extended storage.

[0082] For ease of explanation, the following will take an extended bus standard of the PCIE as an example to introduce the implementation examples of the above situations.

[0083] Regarding situation 1, on the basic of the computer system architecture shown in FIG. 1, FIG. 5A exemplarily illustrates a diagram of an implementation example of the write copying method provided in an embodiment of the present application. As shown in FIG. 5A, in the computer system architecture, when writing

data to the memory, the processor core can initiate a write operation to the memory. At this time, the write address of the write operation belongs to the memory address of the memory, and the write data of the write operation is the data written to that memory address. For ease of example, the write address of the write operation can be set to a memory address 511. Therefore, the processor core can search for each table entry record in the mirror address table according to the memory address 511 of the write operation. It is assumed that the target table entry record hit by the memory address 511 of the write operation in the mirror address table is shown as FIG. 5A, and it is further assumed that the source address recorded in the target table entry record is a memory address 512, the total address length is L1, and the mirror address is a storage address 513 of the PCIE storage. That is, the memory address 512 and the total address length L1 can indicate a range of addresses of the memory, and the memory address 511 of the write operation is within this range of addresses of the memory; furthermore, an embodiment of the present application can determine that the write copying can be performed on the write operation of the processor core to the memory, and the destination address of the copy write operation is obtained by adding the memory address 511 of the write operation to the mirror address (the of the PCIE storage) of the target table entry record, and subtracting the source address (the memory address 512) of the target table entry record. Since the mirror address of the target table entry record belongs to the storage address of the PCIE storage, the destination address of the copy write operation points to the PCIE storage and belongs to the storage address of the PCIE storage. For ease of example, the destination address of the copy write operation can be set to a storage address 514 of the PCIE storage.

[0084] After determining the destination address of the copy write operation (the storage address 514 of the PCIE storage), the processor core can generate the copy write operation, where the copy write operation can be used to write mirror data to the storage address 514 of the PCIE storage.

[0085] Furthermore, the processor core can transmit the write operation targeted for the memory to the memory controller via a bus (such as a Mesh bus), so that the

memory controller can write the write data to the memory address 511; while the processor core can transmit the copy write operation targeted for the PCIE storage to the PCIE controller via the bus, so that the PCIE controller writes the mirror data to the storage address 514 of the PCIE storage.

[0086] Regarding situation 2, on the basic of the computer system architecture shown in FIG. 1, FIG. 5B exemplarily illustrates a diagram of another implementation example of the write copying method provided in an embodiment of the present application. As shown in FIG. 5B, in the computer system architecture, when writing data to the PCIE storage, the processor core can initiate a write operation to the PCIE storage. At this time, the write address of the write operation belongs to the storage address of the PCIE storage, and the write data of the write operation is the data written to that storage address. For ease of example, the write address of the write operation can be set to a storage address 521 of the PCIE storage. Therefore, the processor core can search for each table entry record in the mirror address table according to the storage address 521 of the write operation. It is assumed that the target table entry record hit by the storage address 521 of the write operation in the mirror address table is shown as FIG. 5B, and it is further assumed that the source address recorded in the target table entry record is a storage address 522 of the PCIE storage, the total address length is L2, and the mirror address is a memory address 523. That is, the storage address 522 of the PCIE storage and the total address length L2 can indicate a range of storage addresses of the PCIE storage, and the storage address 521 of the write operation is within this range of storage addresses; furthermore, an embodiment of the present application can determine that the write copying can be performed on the write operation of the processor core to the PCIE storage, the destination address of the copy write operation is obtained by adding the storage address 521 of the write operation to the mirror address (the memory address 523) of the target table entry record, and subtracting the source address (the storage address 522 of the PCIE storage) of the target table entry record. Since the mirror address of the target table entry record belongs to the memory address, the destination address of the copy write operation points to the memory and belongs to the address in the

memory. For ease of example, the destination address of the copy write operation can be set to a memory address 524.

[0087] After determining the destination address of the copy write operation (the memory address 524), the processor core can generate the copy write operation, where the copy write operation can be used to write mirror data to the memory address 524.

[0088] Furthermore, the processor core can transmit the write operation targeted for the PCIE storage to the PCIE controller via a bus (such as a Mesh bus), so that the PCIE controller can write the write data to the storage address 521 of the PCIE storage; while the processor core can transmit the copy write operation targeted for the memory to the memory controller via the bus, so that the memory controller can write the mirror data to the memory address 524.

[0089] Regarding situation 3, FIG. 5C exemplarily illustrates a diagram of a further implementation example of the write copying method provided in an embodiment of the present application. As shown in FIG. 5C, when writing data to the memory, the processor core can initiate a write operation to the memory. For ease of example, the write address of the write operation can be set to a memory address 531. Therefore, the processor core can search for each table entry record in the mirror address table according to the memory address 531 of the write operation. It is assumed that the target table entry record is shown as FIG. 5C, the source address recorded in the target table entry record is a memory address 532, the total address length is L3, and the mirror address is a memory address 533. That is, the memory address 531 of the write operation is within a range of addresses of the memory indicated by the memory address 532 and the total address length L3; furthermore, an embodiment of the present application can determine that the write copying can be performed on the write operation of the processor core to the memory, the destination address of the copy write operation is obtained by adding the memory address 531 of the write operation to the mirror address (the memory address 533) of the target table entry record, and subtracting the source address (the memory address 532) of the target table entry record. Since the mirror address of the target table entry record

belongs to the memory address, the destination address of the copy write operation points to the memory and belongs to the address in the memory. For ease of example, the destination address of the copy write operation can be set to a memory address 534.

[0090] After determining the destination address of the copy write operation (the memory address 534), the processor core can generate the copy write operation, where the copy write operation can be used to write mirror data to the memory address 534.

[0091] Furthermore, the processor core can transmit the write operation targeted for the memory to the memory controller via a bus (such as a Mesh bus), so that the memory controller can write the write data to the memory address 531; while the processor core can transmit the copy write operation targeted for the memory to the memory controller via the bus, so that the memory controller can write the mirror data to the memory address 534.

[0092] Regarding situation 4, FIG. 5D exemplarily illustrates a diagram of a yet another implementation example of the write copying method provided in an embodiment of the present application. As shown in FIG. 5D, when writing data to the PCIE storage, the processor core can initiate a write operation to the PCIE storage. For ease of example, the write address of the write operation can be set to a storage address 541 of the PCIE storage. Therefore, the processor core can search for each table entry record in the mirror address table according to the storage address 541 of the write operation. It is assumed that the target table entry record is shown as FIG. 5D, the source address recorded in the target table entry record is a storage address 542 of the PCIE storage, the total address length is L4, and the mirror address is a storage address 543 of the PCIE storage. That is, the storage address 542 of the PCIE storage and the total address length L4 can indicate a range of storage addresses of the PCIE storage, and the storage address 541 of the write operation is within this range of storage addresses; furthermore, an embodiment of the present application can determine that the write copying can be performed on the write operation of the processor core to the PCIE storage, the destination address of the copy write operation

is obtained by adding the storage address 541 of the write operation to the mirror address (the storage address 543) of the target table entry record, and subtracting the source address (the storage address 542) of the target table entry record. The destination address of the copy write operation points to the PCIE storage and belongs to the storage address of the PCIE storage. For ease of example, the destination address of the copy write operation can be set to a storage address 544 of the PCIE storage.

[0093] After determining the destination address (the storage address 544) of the copy write operation, the processor core can generate the copy write operation, where the copy write operation can be used to write mirror data to the storage address 544 of the PCIE storage.

[0094] Furthermore, the processor core can transmit the write operation targeted for the PCIE storage to the PCIE controller via a bus (such as a Mesh bus), so that the PCIE controller can write the write data to the storage address 541 of the PCIE storage; while the processor core can transmit the copy write operation targeted for the PCIE storage to the PCIE controller via the bus, so that the PCIE controller can write the mirror data to the storage address 544 of the PCIE storage.

[0095] Based on the write copying method performed and implemented by the processor core provided in the embodiment of the present application, an embodiment of the present application may also provide a processor core for performing and implementing this method.

[0096] As an optional implementation, the processor core provided in an embodiment of the present application can configure a mirror address table, where the mirror address table indicates at least one address range where write copying is allowed, and indicates a mirror address corresponding to each address range; where a type of a storage pointed to by the address range is the same as or different from a type of a storage pointed to by the mirror address corresponding to the address range. On the basis of configuring the mirror address table, the processor core provided in an embodiment of the present application can be configured to perform the method flow performed and implemented by the processor core provided in an embodiment of the

present application.

[0097] An embodiment of the present application further provides a computer system, and the computer system may include the processor core provided in an embodiment of the present application described above. Furthermore, an embodiment of the present application may also provide a computer device, such as a terminal device or a server device, and the computer device may include the computer system provided in an embodiment of the present application described above.

[0098] In other possible alternative implementations, the mirror address table can be set in the first storage controller, so that the first storage controller performs and implements the write copying method provided in an embodiment of the present application. In a possible example, the first storage controller can be a memory controller or an extended storage (such as a PCIE controller), which means that the mirror address table can be set in the memory controller or the extended storage. For ease of explanation, an embodiment of the present application may refer to the storage controlled by the first storage controller as a first storage. For example, if the first storage controller is a memory controller, the first storage can be understood as the memory. For another example, if the first storage controller is an expansion controller (such as the PCIE controller), the first storage can be understood as the extended storage (such as the PCIE storage).

[0099] In a case that the first storage controller performs and implements the write copying method provided in an embodiment of the present application, based on the first storage controller controlling the first storage, the first storage controller can obtain the write operation of the processor core to the first storage, and copy the write operation based on the mirror address table. And, the type of memory targeted by the copy write operation can be the same as or different from the type of the first storage. That is, the first storage controller can copy the write operation of the processor core to the first storage, and the type of memory targeted by the copy write operation is not limited.

[0100] Based on the above concepts, FIG. 6 exemplarily illustrates another optional flowchart of the write copying method provided in an embodiment of the

present application, where the method flow can be performed and implemented by the first storage controller, and the first storage controller controls the first storage. The first storage controller can be any type of storage controller, such as any one of the memory controller and the expansion controller. Referring to FIG. 6, the method flow can include the following steps.

[0101] In step S610, obtaining a write operation of a processor core to the first storage; where the write operation indicates at least write data and a write address of the write data in the first storage.

[0102] Based on that the first storage controller controls the first storage, when the processor core initiates the write operation to the first storage, the write operation can be transmitted to the first storage controller via a bus (such as a Mesh bus), so that the first storage controller obtains the write operation of the processor core to the first storage. The write operation of the processor core to the first storage can indicate at least write data that the processor core needs to write to the first storage, as well as the write address at which the write data is written to the first storage.

[0103] In some implementations, if the first storage controller is a memory controller, then the first storage is the memory. When the processor core issues the write operation to the memory, the memory controller can obtain the write operation of the processor core to the memory via the bus. This write operation can indicate at least the write data that the processor core needs to write to the memory, as well as the write address at which the write data is written to the memory, that is, at this time, the write address belongs to the memory address. In other possible implementation examples, if the first storage controller is an expansion controller, the first storage is the extended storage. When the processor core issues the write operation to the extended storage, the expansion controller can obtain the write operation of the processor core to the extended storage via the bus. This write operation can indicate at least the write data that the processor core needs to write to the extended storage, as well as the write address at which the write data is written to the extended storage, that is, at this time, the write address belongs to the storage address of the extended storage.

[0104] In step S611, determining whether existing a target address range that matches the write address in an address range indicated by a mirror address table; if so, performing step S612, if not, performing step S615.

[0105] In some implementations, the mirror address table is set in the first storage controller, and the mirror address table indicates at least one address range where the write copying is allowed in the first storage and a mirror address corresponding to each address range; where a type of a storage pointed to by the mirror address corresponding to the address range is the same as or different from a type of the first storage.

[0106] In a case that the first storage controller performs and implements the write copying method provided in an embodiment of the present application, the mirror address table is set in the first storage controller, and the address range where the write copying is allowed indicated by the mirror address table is an address range where the write copying is allowed in the first storage. In a possible implementation example, if the first storage controller is a memory controller, the mirror address table is set in the memory controller and indicates the address range where the write copying is allowed in the memory. In other possible implementation examples, if the first storage controller is an expansion controller (such as a PCIE controller), the mirror address table is set in the expansion controller and indicates the address range where the write copying is allowed in the extended storage (such as a PCIE storage).

[0107] In a case where the write copying is allowed for the write operation of the processor core to the first storage, an embodiment of the present application does not limit the type of storage targeted by the copy write operation. The destination address of the copy write operation is determined according to the mirror address. Therefore, when configuring the mirror address table, the type of storage pointed to by the mirror address is the same as or different from the type of the first storage.

[0108] In some implementations, the mirror address table can include at least one table entry record, where one table entry record indicates an address range where write copying is allowed by the first storage and a corresponding mirror address, the type of storage pointed to by the mirror address is the same as or different from the

type of the first storage. In a possible implementation example, if the mirror address table is set in the memory controller, the table entry record indicates an address range where the write copying is allowed in the memory and the corresponding mirror address. The mirror address can point to the memory or the extended storage. In a possible implementation example, if the mirror address table is set in the expansion controller, one table entry record indicates an address range where the write copying is allowed in the extended storage and the corresponding mirror address. The mirror address can point to the memory or the extended storage.

[0109] In a further optional implementation, the address range indicated by the table entry record can be determined by a source address and a total address length recorded by the table entry record; in the case where the mirror address table is set in the first storage controller, one table entry record records one source address, one total address length, and one mirror address, where the source address belongs to the storage address of the first storage.

[0110] In a case where the mirror address table indicates at least one address range where the write copying is allowed in the first memory and indicates the mirror address corresponding to each address range, the implementation and related content for determining whether existing a target address range that matches the write address can be referred to in the relevant sections of the previous text, and will not be further elaborated here.

[0111] In step S612, determining, according to a target mirror address corresponding to a target address range, a destination address of a copy write operation; where a type of a storage pointed to by the destination address is the same as or different from a type of the first storage.

[0112] In step S613, generating, according to the destination address of the copy write operation, the copy write operation, where the copy write operation is used to write mirror data of the write data at the destination address.

[0113] An embodiment of the present application does not limit the storage type pointed to by the destination address of the copy write operation. For example, the write operation is targeted for the memory, and the copy write operation is targeted for

the memory or the extended storage. In a case where the write copying is allowed for the write operation, the method of determining the destination address of the copy write operation, as well as generating the copy write operation, can be referred to in the relevant sections of the previous text, and will not be further elaborated here.

[0114] In step S614, performing the write operation and processing the copy write operation.

[0115] Since the first storage controller controls the first storage, for the write operation to the first storage, the first storage controller can perform the write operation, so as to write data at the write address of the first storage. Meanwhile, in a case where the write copying is allowed for the write operation, based on the copy write operation generated by the first storage controller, the first storage controller may perform further processing on the copy write operation. For example, if the copy write operation is also targeted for the first storage, the first storage controller can perform the copy write operation to write the mirror data to the destination address of the first storage. For another example, if the type of storage pointed to by the copy write operation is different from the type of the first storage, the first storage controller can transmit the copy write operation to the storage controller corresponding to the copy write operation through the bus, so that the storage controller corresponding to the copy write operation performs the copy write operation.

[0116] In step S615, performing the write operation.

[0117] It can be seen that compared to the write copying method performed by the processor core in the previous text, the main difference in implementation of the write copying method executed by the first storage controller in this embodiment of the present application is that the write operation is targeted for the first storage, the mirror address table is set in the first storage controller, and the address range where the write copying is allowed indicated by the mirror address table belongs to the address range of the first storage (for example, the source address in the table entry record belongs to the storage address of the first storage). Based on the above differences, the implementation of the write copying method performed by the first

storage controller can be adaptively adjusted and changed on the basis of the implementation of the write copying method performed by the processor core. The contents associated with the two methods can be referenced to each other. It should be noted that, through setting up the mirror address table in the first storage controller, and performing the write copying method provided in an embodiment of the present application by the first storage controller, it can eliminate the need to deploy the implementation logic of the write copying in the processor core, reduce the signal processing delay of the common path in the processor core, but the write operation needs to be targeted at the first storage controlled by the first storage controller.

[0118] The solution provided in an embodiment of the present application can support, through configuring the mirror address table in the first storage controller, copying the write operation of the processor core to the first storage into the copy write operation for any type of storage; thus, when the first storage controller obtains the write operation to the first storage initiated by the processor core, if the write copying is allowed for the write operation, an embodiment of the present application can copy the write operation to obtain the copy write operation, and make that the type of storage pointed to by the destination address of the copy write operation is the same as or different from the type of the first storage; thereby reducing the usage limitations of the write copying.

[0119] Based on the write copying method provided in FIG. 6, as an optional implementation example, the first storage controller can be the memory controller, and the first storage can be the memory. Based on the mirror address table set in the memory controller, the memory controller can copy the write operation of the processor core to the memory, and the copy write operation may be targeted for the memory or for the extended storage (the type of storage targeted by the copy write operation depends on the specific configuration purpose of the mirror address table). Taking the first storage controller as the memory controller and the expansion bus standard as the PCIE as an example, a possible implementation example is introduced below.

[0120] On the basic of the computer system architecture shown in FIG. 1, FIG. 7

exemplarily illustrates a still another implementation example of the write copying method provided in an embodiment of the present application. As shown in FIG. 7, in the computer system architecture, when writing data to the memory, the processor core can initiate the write operation to the memory; at this time, the write address of the write operation is the memory address of the memory. For ease of example, the write address of the write operation can be set to a memory address 711. Therefore, the write operation initiated by the processor core can be transmitted to the memory controller via the bus. The memory controller can search for various table entry records in the mirror address table according to the memory address 711 of the write operation. The source address recorded in the table entry record of the mirror address table belongs to the memory address, and the mirror address may belong to the memory address or the storage address of the PCIE storage. It is assumed that the target table entry record hit by the memory address 711 of the write operation in the mirror address table is shown as FIG. 7, and it is further assumed that the source address recorded in the target table entry record is a memory address 712, the total address length is L5, and the mirror address is a storage address 713 of the PCIE storage. Furthermore, the memory controller can add the memory address 711 of the write operation to the mirror address (the storage address 713 of the PCIE storage) of the target table entry record, and subtract the source address (the memory address 712) of the target table entry record, so as to obtain the destination address of the copy write operation. The destination address of the copy write operation points to the PCIE storage and belongs to the storage address of the PCIE storage. For ease of example, the destination address of the copy write operation can be set to a storage address 714 of the PCIE storage.

[0121] After determining the destination address of the copy write operation (the storage address 714 of the PCIE storage), the memory controller can generate the copy write operation, where the copy write operation can be used to write mirror data to the storage address 714 of the PCIE storage.

[0122] Furthermore, the memory controller can perform the write operation to write the write data to the memory address 711; while the memory controller can

transmit the copy write operation targeted for the PCIE storage to the PCIE controller via the bus, so that the PCIE controller can write the mirror data to the storage address 714 of the PCIE storage.

[0123] FIG. 7 takes the copy write operation being targeted for the PCIE storage as an example for illustration, while the copy write operation may also be targeted for the memory (for example, the mirror address of the target table entry record hit in the mirror address table belongs to the memory address); in this case, the implementation content can be obtained based on an adaptive adjustment of the previous description, and will not be expanded here.

[0124] Based on the write copying method provided in FIG. 6, as an optional implementation example, the first storage controller can be the expansion controller, and the first storage can be the extended storage. Based on the mirror address table set in the expansion controller, the expansion controller can copy the write operation of the processor core to the extended storage, and the copy write operation may be targeted for the memory or for the extended storage (the type of storage targeted by the copy write operation depends on the specific configuration purpose of the mirror address table). The following will take an extended bus standard of the PCIE as an example to introduce possible implementation examples.

[0125] On the basic of the computer system architecture shown in FIG. 1, FIG. 8 exemplarily illustrates a still further implementation example of the write copying method provided in an embodiment of the present application. As shown in FIG. 8, in the computer system architecture, when writing data to the PCIE storage, the processor core can initiate the write operation to the PCIE storage; at this time, the write address of the write operation is the storage address of the PCIE storage, and the write data of the write operation is data written to the storage address. For ease of example, the write address of the write operation can be set to a storage address 811 of the PCIE storage. Therefore, the write operation initiated by the processor core can be transmitted to the PCIE controller via the bus. The PCIE controller can search for various table entry records in the mirror address table according to the storage address 811 of the write operation. The source addresses recorded in the table entry records of

the mirror address table belong to the storage addresses of the PCIE storage, and the mirror address may belong to the memory address or the storage address of the PCIE storage. It is assumed that the target table entry record hit by the storage address 811 of the write operation in the mirror address table is shown as FIG. 8, and it is further assumed that the source address recorded in the target table entry record is a storage address 812 of the PCIE storage, the total address length is L6, and the mirror address is a memory address 813. Furthermore, the PCIE controller can add the storage address 811 of the write operation to the mirror address (the memory address 813) of the target table entry record, and subtract the source address (the storage address 812 of the PCIE storage) of the target table entry record, so as to obtain the destination address of the copy write operation. The destination address of the copy write operation points to the memory and belongs to the memory address. For ease of example, the destination address of the copy write operation can be set to a memory address 814.

[0126] After determining the destination address (the memory address 814) of the copy write operation, the PCIE controller can generate the copy write operation, where the copy write operation can be used to write mirror data to the memory address 814.

[0127] Furthermore, the PCIE controller can perform the write operation to write the write data to the storage address 811 of the PCIE storage; while the PCIE controller can transmit the copy write operation targeted for the memory to the memory controller via the bus, so that the memory controller can write the mirror data to the memory address 814.

[0128] FIG. 8 takes the copy write operation being targeted for the memory as an example for illustration, the copy write operation may also be targeted for the extended storage (for example, the mirror address of the target table entry record hit in the mirror address table belongs to the storage address of the PCIE storage); in this case, the implementation content can be obtained based on an adaptive adjustment of the previous description, and will not be expanded here.

[0129] Based on the write copying method performed and implemented by the

first storage controller provided in the embodiment of the present application, an embodiment of the present application may also provide a storage controller for performing and implementing this method.

[0130] In some implementations, the storage controller provided in an embodiment of the present application can control the first storage, and the storage controller can configure the mirror address table, and the mirror address table indicates at least one address range where the write copying is allowed in the first storage and a mirror address corresponding to each address range; where a type of a storage pointed to by the mirror address corresponding to the address range is the same as or different from a type of the first storage. On the basis of configuring the mirror address table, the storage controller provided in an embodiment of the present application can be configured to perform the method flow performed and implemented by the storage controller provided in an embodiment of the present application.

[0131] An embodiment of the present application provides a computer system, where the computer system may include the storage controller provided in the embodiment of the present application. Furthermore, an embodiment of the present application may also provide a computer device, such as a terminal device or a server device, and the computer device may include the computer system provided in the embodiment of the present application.

[0132] In some implementations, the computer system provided in the embodiment of the present application may include: a processor core, a memory controller, a memory controlled by the memory controller, an expansion controller, and an extended storage controlled by the expansion controller. Where the processor core may be the processor core configured with the mirror address table and provided in the embodiment of the present application, or at least one of the memory controller and the expansion controller may be the storage controller configured with the mirror address table and provided in the embodiment of the present application.

[0133] The above text describes multiple embodiment schemes provided by the embodiments of the present application. The various optional manners introduced in

each embodiment scheme can be mutually combined and cross referenced without conflict, thereby extending multiple possible embodiment schemes, which can all be considered as revealed and disclosed embodiment schemes of the present application.

[0134] Although the embodiments disclosed in the present application are described above, the present application is not limited thereto. Any persons of skill in the art may make various changes and modifications without departing from the spirit and scope of the present application, therefore the protection scope of the present application should be subject to the scope defined by the claims.

CLAIMS

1. A write copying method, applied to a processor core, wherein the method comprises:

initiating a write operation, wherein the write operation indicates at least a write address and write data;

determining whether existing a target address range that matches the write address in an address range indicated by a mirror address table; wherein the mirror address table is set in the processor core; the mirror address table indicates at least one address range where write copying is allowed, and indicates a mirror address corresponding to each address range; a type of a storage pointed to by the address range is the same as or different from a type of a storage pointed to by the mirror address corresponding to the address range; the type of the storage is a memory and an extended storage;

in case that the target address range that matches the write address exists, determining, according to a target mirror address corresponding to the target address range, a destination address of a copy write operation; wherein a type of a storage pointed to by the write address is the same as or different from a type of a storage pointed to by the destination address;

generating, according to the destination address, the copy write operation, wherein the copy write operation is used to write mirror data of the write data at the destination address;

issuing the write operation and the copy write operation.

2. The method according to claim 1, wherein the mirror address table comprises at least one table entry record, one table entry record indicates an address range where write copying is allowed and a corresponding mirror address; the determining whether existing the target address range that matches the write address in the address range indicated by the mirror address table comprises:

determining whether existing a target table entry record with an address range

that matches the write address; wherein the address range indicated by the target table entry record is the target address range.

3. The method according to claim 2, wherein the address range indicated by the table entry record is determined by a source address and a total address length recorded by the table entry record, and one table entry record records one source address, one total address length, and one mirror address;

the determining whether existing a target table entry record with the address range that matches the write address comprises:

determining, according to the source address and the total address length recorded in each table entry record, the address range indicated by each table entry record; wherein the source address of the table entry record is a starting address of the address range indicated by the table entry record, an address obtained by combining the source address and the total address length of the table entry record is an ending address of the address range indicated by the table entry record;

determining, according to the address range indicated by each table entry record, whether existing the target table entry record with the address range that matches the write address.

4. The method according to claim 3, wherein the determining, according to the target mirror address corresponding to the target address range, the destination address of the copy write operation comprises:

determining the destination address according to the target mirror address, the write address and the source address recorded in the target table entry record.

5. The method according to any one of claims 1-4, wherein the type of the storage pointed to by the write address is different from the type of the storage pointed to by the destination address; the write address belongs to a memory address of the memory, and the destination address belongs to a storage address of the extended storage; or, the write address belongs to a storage address of the extended storage, and the destination address belongs to a memory address of the memory;

the issuing the write operation and the copy write operation comprises:

in case that the write address belongs to the memory address of the memory, and

the destination address belongs to the storage address of the extended storage, transmitting the write operation to a memory controller, and transmitting the copy write operation to an expansion controller;

or, in case that the write address belongs to the storage address of the extended storage, and the destination address belongs to the memory address of the memory, transmitting the write operation to an expansion controller, and transmitting the copy write operation to a memory controller.

6. The method according to any one of claims 1-4, wherein the type of the storage pointed to by the write address is the same as the type of the storage pointed to by the destination address; both the write address and the destination address belong to a memory address of the memory; or, both the write address and the destination address belong to a storage address of the extended storage;

the issuing the write operation and the copy write operation comprises:

in case that both the write address and the destination address belong to the memory address of the memory, transmitting the write operation and the copy write operation to a memory controller;

or, in case that both the write address and the destination address belong to the storage address of the extended storage, transmitting the write operation and the copy write operation to an expansion controller.

7. A write copying method, applied to a first storage controller, wherein the first storage controller controls a first storage, and the method comprises:

obtaining a write operation of a processor core to the first storage; wherein the write operation indicates at least write data and a write address of the write data in the first storage;

determining whether existing a target address range that matches the write address in an address range indicated by a mirror address table; wherein the mirror address table is set in the first storage controller, the mirror address table indicates at least one address range where write copying is allowed in the first storage, and indicates a mirror address corresponding to each address range; wherein a type of a storage pointed to by the mirror address corresponding to the address range is the

same as or different from a type of the first storage; the type of the storage is a memory and an extended storage;

determining, according to a target mirror address corresponding to a target address range, a destination address of a copy write operation; wherein a type of a storage pointed to by the destination address is the same as or different from a type of the first storage;

generating, according to the destination address of the copy write operation, the copy write operation, wherein the copy write operation is used to write mirror data of the write data at the destination address.

performing the write operation and processing the copy write operation.

8. The method according to claim 7, wherein the mirror address table comprises at least one table entry record, one table entry record indicates an address range where write copying is allowed in the first storage and a corresponding mirror address; the address range indicated by the table entry record is determined by a source address and a total address length recorded by the table entry record, and one table entry record records one source address, one total address length, and one mirror address; and the source address belongs to the storage address of the first storage.

the source address of the table entry record is a starting address of the address range indicated by the table entry record, and an address obtained by combining the source address and the total address length of the table entry record is an ending address of the address range indicated by the table entry record;

wherein the destination address is determined according to the target mirror address, the write address and the source address recorded in the target table entry record, and the target table entry record is a table entry record indicating the target address range.

9. The method according to claim 7 or 8, wherein the first storage controller is a memory controller, and the first storage is a memory; the type of the storage pointed to by the mirror address corresponding to the address range is the same as or different from the type of the first storage comprises:

the mirror address corresponding to the address range points to the extended

storage or the memory;

the type of the storage pointed to by the destination address is the same as or different from the type of the first storage comprises:

the destination address points to the extended storage or the memory;

the processing the copy write operation comprises:

in case that the destination address points to the extended storage, transmitting the copy write operation to the expansion controller, so as to enable the expansion controller to perform the copy write operation;

in case that the destination address points to the memory, performing the copy write operation.

10. The method according to claim 7 or 8, wherein the first storage controller is an expansion controller, and the first storage is an extended storage; the type of the storage pointed to by the mirror address corresponding to the address range is the same as or different from the type of the first storage comprises:

the mirror address corresponding to the address range points to the extended storage or the memory;

the type of the storage pointed to by the destination address is the same as or different from the type of the first storage comprises:

the destination address points to the extended storage or the memory;

the processing the copy write operation comprises:

in case that the destination address points to the extended storage, performing the copy write operation;

in case that the destination address points to the memory, transmitting the copy write operation to the memory controller, so as to enable the memory controller to perform the copy write operation.

11. A processor core, wherein the processor core is configured with a mirror address table, the mirror address table indicates at least one address range where write copying is allowed, and indicates a mirror address corresponding to each address range; a type of a storage pointed to by the address range is the same as or different from a type of a storage pointed to by the mirror address corresponding to the address

range; the type of the storage is a memory and an extended storage; and the processor core is configured to perform the write copying method according to any one of claims 1-6.

12. A storage controller, wherein the storage controller controls a first storage; the storage controller is configured with a mirror address table, the mirror address table indicates at least one address range where write copying is allowed in the first storage, and indicates a mirror address corresponding to each address range; a type of a storage pointed to by the mirror address corresponding to the address range is the same as or different from a type of the first storage; the type of the storage is a memory and an extended storage; and the storage controller is configured to perform the write copying method according to any one of claims 7-10.

13. A computer system, comprising: the processor core according to claim 11, a memory controller, a memory controlled by the memory controller, an expansion controller, and an extended storage controlled by the expansion controller.

14. A computer device, comprising the computer system according to claim 13.