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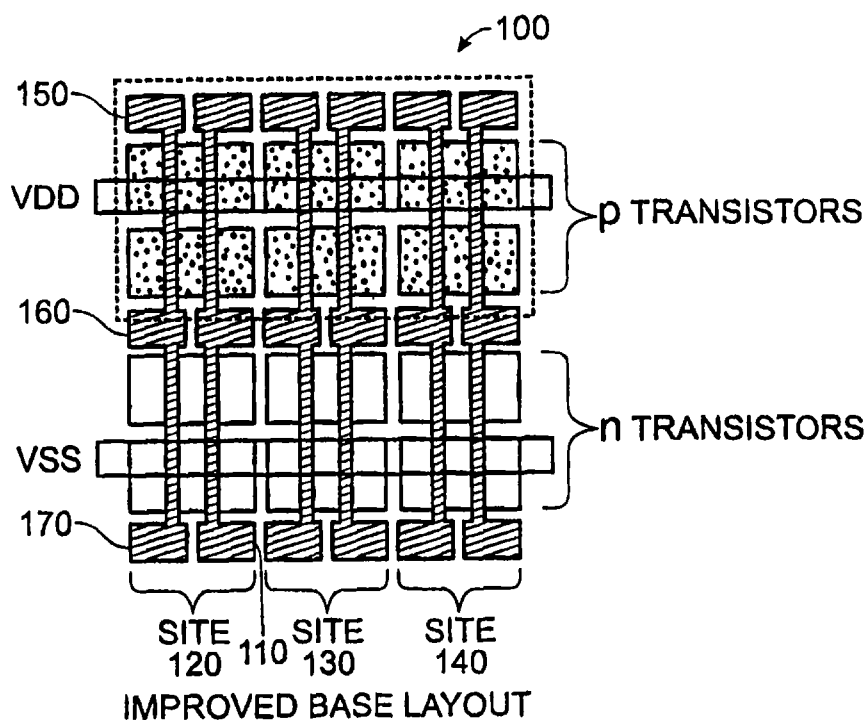
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(54) Title: GATE ARRAY ARCHITECTURE

(57) Abstract

Briefly, in accordance with one embodiment of the invention, an integrated circuit includes: a gate array architecture. The gate array architecture includes at least one base site, the at least one base site being three tracks wide and including four N-type transistors and four P-type transistors. Briefly, in accordance with another embodiment of the invention, a method of fabricating an integrated circuit chip includes: processing a semiconductor substrate to form a gate array architecture of transistors in the substrate. The gate array architecture includes at least one base site being three tracks wide and including four N-type transistors and four P-type transistors. Briefly, in accordance with still another embodiment of the invention, an article includes: a storage medium, the storage medium

having instructions stores thereon, the instructions, when executed, resulting in the capability to design the layout of an integrated circuit chip for fabrication, the integrated circuit chip including a gate array architecture, the gate array architecture including at least one base site being three tracks wide and including four N-type transistors and four P-type transistors.



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