## CLAIMS

WHAT IS CLAIMED:

1. A method, comprising:

forming a masking material 203S above a gate electrode 211 of a P-type transistor 210p;

forming a strained silicon/germanium material 217 in a recess formed adjacent to said masked gate electrode 211 of said P-type transistor 210p;

forming a protection layer 220 on said strained silicon/germanium material 217; and

forming drain and source regions 214 at least partially in said silicon/germanium material 217 in the presence of said protection layer 220.

2. The method of claim 1, wherein said protection layer 220 is formed prior to removing said masking material 203S formed on said masked gate electrode 211.

3. The method of claim 2, wherein said protection layer 220 is formed in an oxidizing ambient.

4. The method of claim 3, wherein said oxidizing ambient is established in a gaseous ambient.

5. The method of claim 1, wherein said protection layer 220 is formed after removing said masking material 203S formed on said masked gate electrode 211.

6. The method of claim 5, wherein forming said protection layer 220 comprises forming an oxide on said P-type transistor 210p and an N-type transistor 210n and removing said oxide from said N-type transistor 210n while maintaining a portion of said oxide on said silicon/germanium material 217.

7. The method of claim 3, wherein said silicon/germanium material 217 is provided with extra height 217T relative to a bottom surface of a gate insulation layer 212 of said P-type transistor 210p so as to compensate for material loss when forming said protection layer 220 in said oxidizing ambient.

8. The method of claim 1, wherein said protection layer 220 is formed on said silicon/germanium material 217 with an initial thickness of approximately 20 Å or more.

9. The method of claim 1, further comprising removing said protection layer 220 prior to forming a metal silicide on said drain and source regions 214 of said P-type transistor 210p.

10. A method, comprising:

selectively forming a protection layer 220 on a silicon/germanium material 217 formed in an active region of a P-type transistor 210p; and

forming drain and source regions 214 in said active region of said P-type transistor 210p and in an active region of an N-type transistor 210n, while said protection layer 220 selectively covers said silicon/germanium material 217.

11. The method of claim 10, wherein said protection layer 220 is formed by an oxidation process.

12. The method of claim 11, wherein selectively forming said protection layer 220 comprises oxidizing said silicon/germanium material 217 while maintaining said N-type transistor 210n and a gate electrode 211 of said P-type transistor 210p masked.

13. The method of claim 11, wherein selectively forming said protection layer 220 comprises removing a masking material 220S from above said N-type transistor 210n and a gate electrode 211 of said P-type transistor 210p after forming said silicon/germanium material 217, exposing said P-type transistor 210p and said N-type transistor 210n to an oxidizing ambient and removing oxide material in said N-type transistor 210n.

14. The method of claim 11, further comprising forming said silicon/germanium material 217 with excess height 217T in said active region of the P-type transistor 210p, said excess height 217T substantially compensating for a material loss of said silicon/germanium material 217 when exposed to said oxidizing ambient.

15. A method, comprising:

depositing a protection layer 320 on a silicon/germanium material 317 formed in an active region of a P-type transistor 310p;

performing at least one manufacturing process in the presence of said protection layer 320; and

removing said protection layer 320 prior to forming a metal silicide at least partially in said silicon/germanium material 317 formed in said P-type transistor 310p.

16. The method of claim 15, wherein said protection layer 320 is formed after removing a masking material provided on a gate electrode 311 of said P-type transistor 310p and used for forming said silicon/germanium material 317.

CLAIMS

1. A method, comprising:

forming a masking material above a gate electrode of a P-type transistor, wherein said masking material covers sidewall and upper surfaces of said gate electrode;

forming a strained silicon/germanium material in a recess formed adjacent to said masked gate electrode of said P-type transistor;

forming a protection layer above said P-type transistor while said masking material covers said sidewall and upper surfaces of said gate electrode, wherein at least a first portion of said protection layer completely covers said strained silicon/germanium material; and

forming drain and source regions at least partially in said silicon/germanium material in the presence of said protection layer, wherein forming said drain and source regions comprises performing an implantation process to implant P-type dopants through said first portion of said protection layer.

2. The method of claim 1, wherein said protection layer is formed in an oxidizing ambient.

3. The method of claim 2, wherein said oxidizing ambient is established in a gaseous ambient.

4. The method of claim 2, wherein additional material is formed adjacent said gate electrode of said P-type transistor, said additional material being provided with extra height relative to a bottom surface of a gate insulation layer of said P-type transistor so as to compensate for material loss when forming said protection layer in said oxidizing ambient.

5. The method of claim 4, wherein said additional material comprises silicon/germanium.

6. The method of claim 4, wherein said additional material is substantially silicon.

7. The method of claim 1, wherein said protection layer is formed on said silicon/germanium layer with an initial thickness of approximately 20 Å or more.

8. The method of claim 1, further comprising removing said protection layer prior to forming a metal silicide on said drain and source regions of said P-type transistor.

9. The method of claim 1, wherein forming said protection layer comprises, after forming said strained silicon/germanium material in said recess, incorporating carbon into a surface area

of said strained silicon/germanium material by performing one of an implantation or plasma treatment process.

10. A method, comprising:

selectively forming a protection layer on a silicon/germanium material formed in an active region of a P-type transistor, wherein selectively forming said protection layer comprises masking upper and sidewall surfaces of a gate electrode of said P-type transistor so as to prevent said protection layer from being formed thereon, said selectively formed protection layer completely covering said silicon/germanium material; and

forming drain and source regions in said active region of said P-type transistor and in an active region of an N-type transistor after selectively forming said protection layer, wherein forming said drain and source regions in said active region of said P-type transistor comprises performing an ion implantation process in the presence of said selectively formed protection layer to implant dopants therethrough.

11. The method of claim 10, wherein said protection layer is formed by an oxidation process.

12. The method of claim 11, wherein selectively forming said protection layer comprises oxidizing said silicon/germanium material while masking said N-type transistor.

13. The method of claim 11, further comprising forming said silicon/germanium material with excess height in said active region of the P-type transistor, said excess height substantially compensating for a material loss of said silicon/germanium material when exposed to said oxidizing ambient.

14. The method of claim 10, wherein selectively forming said protection layer comprises, after selectively forming said silicon/germanium material in said active region of said P-type transistor, incorporating carbon into a surface area of said silicon/germanium material by performing one of an implantation or plasma treatment process.

15. A method, comprising:

forming a protection layer to completely cover a silicon/germanium material formed in an active region of a P-type transistor, wherein forming said protection layer comprises oxidizing an exposed surface of said silicon/germanium material while masking upper and sidewall surfaces of a gate electrode of said P-type transistor;

performing an implantation process in the presence of said protection layer to implant dopants therethrough, wherein process parameters of said implantation process are determined on the basis of a thickness and material composition of said protection layer; and

removing said protection layer prior to forming a metal silicide at least partially in said silicon/germanium material formed in said P-type transistor.

16. The method of claim 15, wherein a thickness of said protection layer is in a range of approximately 20-100 Å.

17. An integrated circuit formed in accordance with a method of any of the preceding claims.