SOI Chip with Mesa Isolation and Recess Resistant Regions

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This application relates to the following co-pending and commonly assigned patent applications: Serial No. 10/379,873, entitled "Method of Forming Strained Silicon on Insulator Substrate," filed March 5, 2003 (Attorney Docket No. TSMC02-1384); and Serial No. 10/384,859, entitled " SOI Chip with Recess-Resistant Buried Insulator and Method of Manufacturing the Same," filed March 10, 2003 (Attorney Docket No. TSMC02-1385), which applications are hereby incorporated herein by reference.

TECHNICAL FIELD

[0002] The present invention relates generally to silicon-on-insulator devices, and more particularly, the preferred embodiment of the present invention relates to silicon-on-insulator devices isolated by mesa isolation where recess-resistant regions are incorporated in the insulator region.

BACKGROUND

[0003] Traditional silicon-on-insulator (SOI) integrated circuits are formed on SOI substrates. A cross-section of a silicon-on-insulator (SOI) substrate 10 is illustrated in Figure 1a. SOI substrates typically have a thin layer of silicon 12, also known as the silicon active layer, disposed on an insulator layer 14 such as the buried oxide (BOX) layer. The insulator layer or the buried oxide layer 14 is provided on a silicon substrate 16. The buried oxide layer 14 is

comprised of an insulator such as silicon oxide. It electrically isolates the silicon active layer 12 from the silicon substrate 16.

[0004] In a conventional SOI chip, as shown in Figure 1b, the SOI substrate 10 is processed to form a plurality of active regions 18 in the active layer 12. Active devices 20 such as transistors and diodes may be formed in the active regions 18. Active regions 18 are electrically isolated from each other by isolation regions 22. The size and placement of the active regions 18 are defined by isolation regions 22. Isolation regions 22 may, for example, be formed of shallow trench isolation (STI). Moreover, the active devices 20 are isolated from the substrate 16 by the buried oxide layer 14.

[0005] State of the art shallow trench isolation structures typically have a groove-like recess 32 at the isolation edge, as shown in Figure 1b. This groove-like recess 32 results from commonly used wet-etch processes and the recess is in the range of tens to a two hundred angstroms below the surface of the active layer. When the thickness of the active layer is about one hundred angstroms, the groove-like recess potentially encroaches into the buried oxide and therefore renders the STI ineffective in protecting the buried oxide from being etched during wet cleaning processes. Moreover, the top surface of the isolation may also be recessed. In cases where the shallow trench isolation is exposed to an excessive amount of wet-etch processes, the STI may be entirely etched, resulting in an exposed buried oxide between active regions.

[0006] Active devices formed on SOI substrates offer many advantages over their bulk counterparts, including absence of reverse body effect, absence of latch-up, soft-error immunity, and elimination of junction capacitance typically encountered in bulk silicon devices. SOI technology therefore enables higher speed performance, higher packing density, and reduced

power consumption. At present, commercial products using SOI technology employ an uniform active layer thickness and shallow trench isolation.

[0007] One type of SOI transistor employs a very thin silicon active layer. For example, the silicon active layer thickness can be as thin as a third of the gate length. If the gate length is 30 nm, the silicon active layer may have a thickness of 10 nm or thinner. This type of SOI transistor is known as ultra-thin body (UTB) transistors or depleted-substrate transistors (DSTs).

[0008] When the thickness of the silicon active layer is as thin as 10 nm, mesa isolation could be a more appropriate isolation scheme for the transistors as compared to shallow trench isolation. In mesa isolation, trenches 24 are formed in the active layer 12, as shown in Figure 2a. The trenches 24 extend from the surface of the active layer 12 to the buried oxide layer 14. These trenches divide the active layer into silicon islands or silicon mesa structures 26. The mesa isolation method thus cuts electrical connection between adjacent active regions by removing portions of the active layer in the SOI substrate.

[0009] One major problem of the mesa isolation is that the exposed buried oxide layer surface 28 will be recessed in subsequent chemical treatments such as wafer cleaning steps. This issue is illustrated in Figure 2b. The recessed buried oxide results in a number of problems. For example, it leads to an increased parasitic capacitance between the substrate and metal lines running over the buried oxide. It also leads to a concentration of electric field lines around the exposed corners 30 of the silicon mesas 26, which potentially impact device reliability.

[0010] In U.S. Patent No. 5,904,539 issued to Hause et al., a trench isolation process is described for improving the overall planarity of filled isolation regions relative to adjacent silicon mesas. This approach is similar to shallow trench isolation.

[0011] In U.S. Patent No. 6,410,938 issued to Xiang, semiconductor-on-insulator devices isolated by a nitrided buried oxide are described for the reduction of dopant penetration from the active layer into the buried oxide. The nitrided buried oxide is formed by an implantation of nitrogen or nitrogen-containing species through the semiconductor active layer to reach the buried silicon oxide

[0012] In U.S. Patent No. 5,468,657 issued to Hsu, a method is provided for improving the electrical isolation in SIMOX buried oxide wafers. In that invention, nitrogen ions are implanted into a wafer to approximately the same depth as oxygen ions are implanted during SIMOX processing. A subsequent heating step causes the nitrogen ions to migrate to the interface region between the buried oxide and the upper and lower semiconductor regions of the substrate. The nitrogen passivates the interface region to reduce the presence of buried free electrons trapped in the substrate.

SUMMARY OF THE INVENTION

[0013] In one aspect, the present invention provides a silicon-on-insulator chip with a recess-resistant insulator in the isolation regions between silicon mesas. In another aspect, this invention provides a buried insulator with a recess-resistant layer that has negligible etch rates in commonly used wet cleaning solutions. In yet another aspect, this invention provides a silicon nitride recess-resistant layer in the buried oxide of a silicon-on-insulator substrate.

[0014] In one embodiment, a recess-resistant semiconductor-on-insulator structure includes a substrate and an insulator layer overlying the substrate. Semiconductor islands overlie portions of the buried insulator layer. Recess-resistant regions are disposed in portions of the insulator layer not covered by the semiconductor islands.

[0015] A method of forming a recess-resistant semiconductor-on-insulator substrate is also described. For example, a semiconductor structure includes semiconductor islands overlying portions of an insulator layer. Recess-resistant regions are formed in portions of the insulator layer not covered by the semiconductor islands. Devices, such as transistors and/or diodes, can then be formed on the semiconductor islands.

[0016] According to embodiments of the present invention, a recess-resistant layer is provided in the buried insulator of a semiconductor-on-insulator wafer for the purpose of restricting the amount of recess in the exposed insulator during wafer processing such as wet cleaning of wafers in dilute hydrofluoric acid. This can be important where the mesa isolation scheme is adopted in the fabrication of a semiconductor-on-insulator integrated circuit chip. Semiconductor-on-insulator integrated circuit chips employing the mesa isolation scheme have exposed buried insulator surfaces. The exposed buried insulator surfaces are susceptible to

chemical attack or etching during wafer processing. This invention teaches a structure and method of forming a recess-resistant region in the insulator in regions that are susceptible to chemical attack or etching.

BRIEF DESCRIPTION OF THE DRAWINGS

[0017] For a more complete understanding of the present invention, and the advantages thereof, reference is now made to the following descriptions taken in conjunction with the accompanying drawing, in which:

[0018] Figure 1a illustrates a convention SOI substrate;

[0019] Figure 1b illustrates a convention SOI device;

[0020] Figure 2a illustrates a convention SOI device with silicon islands in an active layer;

[0021] Figure 2b illustrates recesses in the buried oxide of a convention SOI device;

[0022] Figures 3a and 3b show a first embodiment structure of the present invention;

[0023] Figures 4a and 4b show a second embodiment structure of the present invention;

[0024] Figures 5a-5h show a method to form an SOI device of the present invention; and

[0025] Figures 6a-6d show an alternative method for forming an SOI device of the present invention.

DETAILED DESCRIPTION OF ILLUSTRATIVE EMBODIMENTS

[0026] The making and using of the presently preferred embodiments are discussed in detail below. It should be appreciated, however, that the present invention provides many applicable inventive concepts that can be embodied in a wide variety of specific contexts. The specific embodiments discussed are merely illustrative of specific ways to make and use the invention, and do not limit the scope of the invention.

[0027] The present invention will be described with respect to preferred embodiments in a specific context, namely a silicon-on-insulator (SOI) semiconductor device. Two embodiment structures will first be described with respect to Figures 3a-3b and 4a-4b. Two methods will then be described with respect to Figures 5a-5h and a third method will be described with respect to Figures 6a-6h.

[0028] Figures 3a and 3b will now be used to illustrate a first embodiment of the present invention. As shown in Figure 3a, an SOI chip 110 includes semiconductor mesas or islands 126 that are isolated from the substrate 116 by a buried insulator 114. The substrate 116 is preferably a silicon substrate. For example, an undoped or lightly doped monocrystalline silicon substrate can be utilized.

[0029] According to the present invention, a portion of the buried insulator 114 includes a recess-resistant region 134 that is resistant to commonly used wafer wet cleaning solutions. That is, the etch rate of the recess-resistant region 134 is extremely slow in commonly used wafer wet cleaning solutions so that the total amount etched is negligible. The thickness of the recess-resistant region 134 may range from about 2 angstroms to about 200 angstroms, and is more

preferably less than 100 angstroms (e.g., from about 10 angstroms to about 100 angstroms). The recess-resistant region 134 is formed on the buried insulator layer 114.

[0030] The buried insulator layer 114 can be a dielectric material such as silicon oxide, for example, and may have a thickness ranging from about 100 angstroms to about 5000 angstroms. One commonly used wet cleaning solution is dilute hydrofluoric acid. Dilute hydrofluoric acid may, for example, be formed by a mixture of 1 part of concentrated (49%) hydrofluoric (HF) acid and 25 parts of water (H_2O). This mixture is also commonly known as 25:1 HF. Another commonly used wafer cleaning solution is a mixture of concentrated sulphuric acid and hydrogen peroxide, commonly known as piranha solution.

[0031] The recess-resistant region 134 is preferably comprised of a dielectric material that has very slow or negligible etch rates in commonly used wet cleaning solutions such as the above-mentioned chemicals or solutions. As shown in Figures 3a and 3b, the buried insulator surface 136 is exposed to common wet cleaning etchants in regions not covered by the semiconductor mesas 126 when the mesas are formed. The recess-resistant layer 134 therefore minimizes the reduction in the physical thickness of the buried insulator. It also prevents the formation of a significant recess in the exposed portion of the buried insulator stack.

[0032] In the preferred embodiment, the recess-resistant region 134 is formed from silicon oxynitride (e.g., SiO_xN_y). The etch rate of silicon oxynitride in 25:1 HF is about 1 to 6 angstroms per minute. The etch rate of thermally grown silicon oxide in 25:1 HF is more than ten times higher, about 100 angstroms per minute. By using silicon oxynitride as a recess-resistant region on the exposed surface of the buried insulator, as illustrated in Figures 3a and 3b, the recess in the buried insulator can be reduced by more than ten times. Selection of other materials could lead to different differences in etch rates.

[0033] In another embodiment of the present invention, the recess-resistant region 134 does not need to be the topmost layer of the buried insulator stack 114. Referring now to Figures 4a and 4b, the recess-resistant region 134 may be formed at a depth d beneath the exposed surface 136 of the buried insulator. The buried insulator 114 is preferably comprised of silicon oxide, but may be any other dielectric such as aluminum oxide. The depth d is preferably less than about 200 angstroms. The depth d is preferably kept very thin to limit the amount of recess in the buried insulator. The depth d may be measured from the surface 136 to the peak of the nitrogen content or nitrogen profile in the silicon oxynitride region 134.

[0034] The recess-resistant region 134 in this embodiment is preferably silicon oxynitride. The thickness of the recess-resistant region may range from about 2 angstroms to about 200 angstroms, and is more preferably less than about 100 angstroms (e.g., from about 10 angstroms to about 100 angstroms). The recess-resistant regions 134 are located in regions susceptible to chemical attack or etching, such as the regions shown in Figure 4b. The material comprising the buried insulator 114, e.g., silicon oxide, is in direct contact with the semiconductor islands 126, e.g., silicon, and serves the purpose of providing a high quality interface between the buried insulator 114 and the semiconductor islands 126.

[0035] The interface between silicon oxide and silicon has a much better lower interface state density than the interface between silicon oxynitride and silicon. Good interface properties and low bulk trap density can be important for the achievement of good electrical characteristics in the active devices. This is especially important in active devices with ultra-thin body thicknesses, in which case the mobile carriers flowing between the source and drain (not shown in Figure 4b; see Figure 5h) are in close proximity to the interface between the active layer 126 and the buried insulator 114. For example, trapped charges or charge centers near the top of the

buried insulator may degrade the carrier mobility in the channel region of an ultra-thin body transistor by Coulombic scattering. The low bulk trap density and a low interface trap density ensure that mobility degradation due to Coulombic scattering is kept to a minimum.

[0036] In the following description, methods of forming the above-mentioned structure will be detailed. A first embodiment method will be discussed with respect to Figures 5a-5h. An alternate embodiment method will then be described.

[0037] Referring now to Figures 5a-5h, cross-sections of the wafer during the various steps of the fabrication process flow are shown. In Figure 5a, the starting substrate includes a semiconductor active layer 112 overlying a buried insulator layer 114. The semiconductor layer 112 is preferably a silicon layer and the buried insulator layer 114 is preferably silicon oxide (e.g., SiO_2). The silicon layer may, for example, be a thin layer of epitaxially grown monocrystalline silicon. However, it is understood that the semiconductor layer 114 may be comprised of other materials such as silicon germanium, germanium, or gallium arsenide, as just three examples. It is also understood that the semiconductor layer 114 may be strained, e.g. strained silicon. The strained silicon may be silicon with a tensile strain, and more specifically silicon with a biaxial tensile strain. The strained silicon may alternatively be silicon with a compressive strain, and more specifically silicon with a biaxial compressive strain.

[0038] As shown in Figure 5b, a mask 138 is used to define active regions or islands 126 in the active layer 112. The mask 138 may be any masking material known and used in the art, nitride, or silicon oxynitride. The mask 138 may also be formed of a stack, e.g., including a silicon nitride layer overlying a silicon oxide layer.

[0039] Following active region definition using mask 138, the active layer 110 is etched using techniques known and used in the art. If the active layer is comprised of silicon, a dry

plasma etch using fluorine chemistry may be used. The etching of the active layer 110 forms trenches 124 between silicon islands 126, as shown in Figure 5c.

[0040] The bottom of the trench 124 is the exposed surface of buried oxide 114. At this point, regions of the buried oxide 114 immediately below the exposed buried oxide surface may be converted to recess-resistant regions 134, as shown in Figure 5d. The conversion process may be a nitridation process, such as an exposure to a nitridizing ambient at an elevated temperature. The nitridizing ambient may be a gas ambient containing nitrogen species, e.g. ammonia, NH_3, N_2O, or others. The nitridation process forms a recess-resistant region 134 comprising of silicon oxynitride.

[0041] The conversion process may alternatively, or additionally, be an ion implantation of nitrogen or nitrogen-containing ions into the region to be converted into a recess-resistant region 134. According to this invention, the mask 138 protects the silicon islands 126 from receiving the implanted ions or from being exposed to the nitridizing ambient. An anneal at a selected temperature (e.g., between about 700 and about 1100 degrees Celsius) and a selected time (e.g., from about 1 to about 500 seconds) may additionally be performed. The ion implantation process forms a silicon oxynitride recess-resistant region.

[0042] The ion implantation process may implant nitrogen ions at an implant energy of about 100 electron-volts (eV) to about 10 kilo-electron-volts (keV) to achieve an implant depth of about 10 angstroms to about 350 angstroms. Such ion implantation conditions result in a silicon oxynitride region 134 that is close to the exposed surface of the buried oxide. In general, an ion implantation of nitrogen or nitrogen-containing ions at sufficiently low energy, e.g. less than 10 keV, results in a recess-resistant region that is near the surface of the buried oxide. The dose of the implant may be in the range of 10^{14} cm^{-2} to 10^{16} cm^{-2}.

[0043] By implanting the nitrogen ions at a larger implant energy, e.g., about 10 keV to about 100 keV, implant depths of more than 350 angstroms will be achieved. This results in a buried silicon oxynitride or recess-resistant region that is beneath the surface of the buried oxide.

[0044] Referring next to Figure 5e, trenches 124 are filled with a trench filling material 140, such as silicon oxide (e.g., SiO_2). The trench filling material 140 protects the recess-resistant material 134 while the mask 138 is removed. Since the mask 138 may be formed from a material similar to that of the recess-resistant region 134, the removal of the mask potentially removes the recess-resistant region. Therefore, as shown in Figure 5f, the trench filling material 140 adequately protects the recess-resistant region 134 from being removed during mask removal.

[0045] After the mask 138 is removed, the trench filling material 140 may be removed, as shown in Figure 5g. At this point, the silicon islands or silicon mesas 126 are formed. The regions of the buried oxide 114 not covered by the silicon mesas 126 are protected from being etched by wet cleaning process agents which are typically used before the wafer enters a gate dielectric deposition or growth chamber. The wet cleaning solutions potentially etch into the buried oxide 114 and result in a recessed buried oxide if the recess-resistant layer does not protect it. The recess-resistant layer has a very low etch rate in commonly used wet cleaning solutions such as dilute hydrochloric acid, and minimizes the amount of recess in the exposed surface of the buried oxide.

[0046] Next, active devices 142 are formed. Figure 5h illustrates the formation of a transistor as the active device 142. A gate dielectric 144 may be formed by thermal oxidation, chemical vapor deposition, or sputtering. The gate dielectric may comprise of a conventional material such as silicon dioxide or silicon oxynitride with a thickness ranging from about 3

angstroms to about 100 angstroms, preferably about 10 angstroms or less. The gate dielectric may also comprise of high permittivity (high-k) materials such as lanthalum oxide (e.g., La_2O_3), aluminum oxide (e.g., Al_2O_3), hafnium oxide (e.g., HfO_2), hafnium oxynitride (e.g., HfON), or zirconium oxide (e.g., ZrO_2), with an equivalent oxide thickness of 3 angstroms to 100 angstroms.

[0047] After formation of the gate dielectric 144, the gate electrode material 146 is deposited. The gate material may be polycrystalline-silicon (poly-Si), polycrystalline silicon-germanium (poly-SiGe), a refractory metal such as molybdenum and tungsten, compounds such as titanium nitride, or other conducting materials. Compound layers of more than one of these materials, e.g., polycrystalline silicon and a refractory metal capable of forming a metal silicide, can be used. Examples include polycrystalline silicon with titanium silicide, tantalum silicide, cobalt silicide, or nickel silicide.

[0048] A gate mask (not shown) is defined and the underlying gate material is etched to form the gate electrode 146. The gate etch stops on the gate dielectric, and the gate is electrically isolated from the transistor structure by the gate dielectric. In the preferred embodiment, the gate material is poly-Si and the gate dielectric is silicon oxynitride. A plasma etch using chlorine and bromine chemistry may be used for the gate electrode etching. After gate definition, the gate mask can be removed.

[0049] The source and drain extensions 148 are formed next. This may be achieved by ion implantation, plasma immersion ion implantation (PIII), or other techniques known and used in the art. Next, a spacer 150 is formed on the sidewalls of the gate 146 by deposition and selective etching of the spacer material. The spacer material may comprise of a dielectric material such as

silicon nitride or silicon dioxide. In the preferred embodiment, the spacer comprises of silicon nitride.

[0050] After spacer formation, source and drain regions 152 are doped by ion implantation, PIII, gas or solid source diffusion, or any other techniques known and used in the art. Any implant damage or amorphization can be annealed through subsequent exposure to elevated temperatures. The resistance of the source, drain, and gate can also be reduced by strapping the source, drain, and gate with a conductive material. The conductive material may be a metallic silicide such as titanium silicide, cobalt silicide, or nickel silicide. In the preferred embodiment, the conductive material is nickel silicide, which may be formed by a self-aligned silicide (salicide) process.

[0051] A second method embodiment will now be described. This embodiment can be best understood with reference to Figures 5c, 5d and 5g. As in the first embodiment, a starting substrate comprising of a semiconductor active layer 112 overlying a buried insulator layer 114 is provided. In Figure 5b, a patterned mask 138 is used to define active regions 126 in the active layer 114. According to the second method embodiment, the patterned mask 138 is formed from a mask material with a different etch rate than nitrided oxide or silicon oxynitride. The mask material 138 is preferably photoresist. The mask material may also be a non-silicon material. The mask material may also be a material with less than 30% silicon by atomic concentration. The mask material may also be a stack of mask materials. In addition, the mask material may be a photoresist layer overlying an anti-reflective coating (ARC) layer.

[0052] The etching of the active layer 112 forms trenches 124 between silicon islands, as shown in Figure 5c and the bottom of the trench 124 is converted to recess-resistant regions 134,

as shown in Figure 5d. As discussed above, the conversion process may be a nitridation process and/or an implantation process.

[0053] In this embodiment, the mask material 138 is a photoresist, which can be easily removed, for example, by exposure to an oxygen plasma in a process known as ashing, or by etching in an organic solvent. By selectively removing the mask material, the cross-section according to Figure 5g can be achieved. In this embodiment, the trench filling material 140 is not necessary.

[0054] Active devices 142, such as transistors, can then be formed on the silicon islands 126, as shown in Figure 5h. The formation of transistor devices was discussed above.

[0055] A third method embodiment is now described with respect to Figures 6a-d. The first few steps of the third method embodiment are identical to the first method embodiment. As a result, the discussion related to Figures 5a-5c will not be repeated here.

[0056] Referring to Figure 5c and Figure 6a, a slight recess in the buried oxide 114 may or may not be etched. In the preferred embodiment, the buried oxide 114 is slightly etched, by an amount in the range of about 10 angstroms to about 100 angstroms, or by an amount equal to the thickness of the recess-resistant layer 154 to be subsequently deposited. The mask 138 may or may not be removed at this point. A recess-resistant layer 154 is then deposited, e.g., by chemical vapor deposition, as shown in Figure 6a. In Figure 6a, the mask 138 is not removed prior to the deposition of the recess-resistant layer 154, but it is understood that it may be removed before the deposition of the recess-resistant layer 154. The recess-resistant layer 154 is substantially conformal, and is formed over the silicon island 126 and the buried oxide 114.

[0057] Referring now to Figure 6b, the trenches 124 between the active regions 126 are filled with a dielectric 156, preferably silicon oxide (e.g., SiO_2). A chemical mechanical planarization process may be performed to obtain the cross-section as shown in Figure 6b. The recess-resistant layer 154 above the silicon islands 126 may then be removed using an etch, preferably a wet etch. The mask 138 may be removed in the same process step. The etch may or may not remove the recess-resistant material 154 on the sidewalls of the silicon active regions 126.

[0058] In the case where the recess-resistant layer on the sidewalls of the silicon active region is removed, the resulting structure is depicted in Figure 6c. The dielectric filling the trench may then be removed, as illustrated in Figure 6d. Although not shown, active devices (e.g., 142 from Figure 5h) can be formed in the silicon islands 126 as discussed above.

[0059] While several embodiments of the invention, together with modifications thereof, have been described in detail herein and illustrated in the accompanying drawings, it will be evident that various modifications are possible without departing from the scope of the present invention. The examples given are intended to be illustrative rather than exclusive.

WHAT IS CLAIMED IS:

1. A semiconductor-on-insulator structure comprising:

a substrate;

a buried insulator layer overlying the substrate;

a plurality of semiconductor islands overlying and abutting the buried insulator layer, the semiconductor islands being isolated from one another by trenches; and

a plurality of recess resistant regions overlying the buried insulator layer at a lower surface of the trenches.

2. The structure of claim 1 wherein the buried insulator comprises an oxide layer.

3. The structure of claim 1 wherein the recess resistant regions comprise oxynitride regions.

4. The structure of claim 1 wherein the recess resistant regions comprise nitride regions.

5. The structure of claim 1 wherein the semiconductor islands comprise silicon islands.

6. The structure of claim 5 wherein the semiconductor islands are formed from strained silicon.

7. The structure of claim 1 wherein the buried insulator layer has an upper surface and the recess resistant regions have an upper surface, wherein upper surface of the recess resistant regions is substantially planar to the upper surface of the buried insulator layer beneath the semiconductor islands.

8. The structure of claim 1 and further comprising a thin material layer overlying the recess resistant regions.

9. The structure of claim 8 wherein the thin material layer and the buried insulator layer are formed from the same material.

10. The structure of claim 1 wherein the recess resistant regions are formed from a dielectric characterized by an etch rate of less than 10 angstroms per minute in a wet cleaning solution.

11. The structure of claim 1 wherein the recess-resistant regions are located above an outer surface of the buried insulator layer.

12. The structure of claim 1 wherein the recess resistant regions are located at a depth within the buried insulator layer.

13. The structure of claim 1 wherein the recess-resistant layer has a thickness of between about 10 angstroms and about 200 angstroms.

14. The structure of claim 1 further comprising at least one transistor formed in the plurality of semiconductor islands.

15. A method of forming a semiconductor-on-insulator device, the method comprising:

providing a plurality of semiconductor islands overlying portions of an insulator layer;

forming recess-resistant regions in portions of the insulator layer not covered by the semiconductor islands; and

forming devices on the semiconductor islands.

16. The method of claim 14 wherein providing a plurality of semiconductor islands comprises:

providing a semiconductor structure comprising the semiconductor layer overlying the insulator layer, said insulator layer overlying a substrate;

forming a mask on the semiconductor layer; and

etching the semiconductor layer in a pattern aligned with the mask to form the semiconductor islands.

17. The method of claim 16 and further comprising, after the step of forming recess-resistant regions:

providing trench filling material in regions between the semiconductor islands;

removing the mask; and

removing the trench filling material.

18. The method of claim 17 wherein the trench filling material comprises silicon oxide.

19. The method of claim 17 wherein the mask is formed from a material selected from the group consisting of oxide, nitride, oxynitride, and combinations thereof.

20. The method of claim 19 wherein the mask is formed from silicon nitride.

21. The method of claim 16 wherein the mask is formed from a photoresist.

22. The method of claim 14 wherein forming recess-resistant regions comprises a nitridation process using a nitrogen or nitrogen-containing ambient.

23. The method of claim 14 wherein forming recess-resistant regions comprises an ion implantation process using a nitrogen or nitrogen-containing ions.

24. The method of claim 23 wherein the ion implantation process employs an implant energy in the range of about 10 eV to about 100 keV.

25. The method of claim 23 wherein the ion implantation process employs an implant energy in the range of about 10 eV to about 10 keV.

26. The method of claim 23 and further comprising annealing the device at a temperature between about 700 and about 1100 degrees Celsius after the ion implantation process.

27. The method of claim 14 wherein the semiconductor islands comprise silicon.

28. The method of claim 27 wherein the semiconductor islands comprise strained silicon.

29. The method of claim 14 wherein the semiconductor islands contain silicon and germanium.

30. The method of claim 14 wherein the recess-resistant region comprises a dielectric that has an etch rate of less than 10 angstroms per minute in a wet cleaning solution.

31. The method of claim 14 wherein the recess-resistant region comprises silicon oxynitride.

32. The method of claim 14 wherein the recess-resistant region has a thickness between about 10 angstroms and about 200 angstroms.

33. The method of claim 16 wherein the substrate comprises a silicon substrate.

34. The method of claim 15 wherein forming recess-resistant regions comprises depositing a recess-resistant layer over portions of the insulator layer not covered by the semiconductor islands.

35. The method of claim 34 wherein depositing a recess-resistant layer comprises depositing a silicon nitride layer.

36. The method of claim 34 and further comprising etching a portion of the insulator layer not covered by the semiconductor islands prior to depositing a recess-resistant layer.

37. The method of claim 34 and further comprising removing portions of the recess-resistant layer such that a portion of the recess-resistant layer remains along a sidewall of each of the semiconductor islands.

38. A method of forming a silicon on insulator device, the method comprising:

providing a semiconductor structure comprising a semiconductor layer overlying an insulating layer, said insulating layer overlying a substrate; forming a patterned mask over the semiconductor layer;

removing portions of the semiconductor layer not protected by the mask;

forming recess-resistant regions within the insulating layer in regions where the semiconductor layer was removed;

removing the mask; and

forming at least one transistor in a remaining portion of the semiconductor layer.

39. The method of claim 38 and further comprising, prior to removing the mask, forming trench filling material regions over the insulating layer where the semiconductor layer was removed.

40. The method of claim 39 wherein the mask is formed from a nitrogen-containing material.

41. The method of claim 40 wherein the recess-resistant regions are formed from a nitrogen-containing material.

42. The method of claim 38 wherein the mask comprises a photoresist.

43. The method of claim 38 wherein the insulating layer comprises an oxide layer and wherein forming the recess-resistant regions comprises nitridizing the insulating layer.

44. The method of claim 38 wherein the insulating layer comprises an oxide layer and wherein forming the recess-resistant regions comprises implanting nitrogen ions into the insulating layer.

45. A method of forming a semiconductor-on-insulator structure, the method comprising:

providing a substrate that includes a buried insulator layer overlying the substrate;

forming a plurality of semiconductor islands overlying and abutting the buried insulator layer, the semiconductor islands being isolated from one another by trenches;

depositing a layer of recess resistant material over the structure; and

removing portions of the layer of recess resistant material so as to form a plurality of recess-resistant regions that overlie the buried insulator layer at a lower surface of the trenches.

46. The method of claim 45 wherein depositing a recess-resistant layer comprises depositing a silicon nitride layer by chemical vapor deposition.

47. The method of claim 45 and further comprising etching a portion of the buried insulator layer within the trenches prior to depositing a recess-resistant layer.

48. The method of claim 45 wherein removing portions of the layer of recess resistant material comprises removing portions of the recess-resistant layer such that a portion of the recess-resistant layer remains along a sidewall of each of the semiconductor islands.