

SELF-ALIGNED DIFFUSED SOURCE VERTICAL TRANSISTORS WITH STACK CAPACITORS IN A 4F-SQUARE MEMORY CELL ARRAY

ABSTRACT

A dense array (500) of vertical semiconductor devices, having pillars (230) with stack capacitors, and methods of manufacture are disclosed. The pillars act as transistor channels, formed between upper and lower doped regions. The lower doped regions are self-aligned and are located below the pillars. The array has columns of bitlines (220) and rows of wordlines (225). The lower doped regions of adjacent bitlines may be isolated from each other without increasing the cell size and allowing a minimum area of approximately $4F^2$ to be maintained. The array is suitable for Gbit DRAM applications because the stack capacitors do not increase array area. The array may have an open bitline, a folded, or an open/folded architecture with dual wordlines, where two transistors are formed on top of each other in each trench. The lower regions may be initially implanted. Alternatively, the lower regions may be diffused below the pillars after forming thereof.

Fig. 27