DOUBLE PINNED PHOTODIODE FOR CMOS APS AND METHOD OF FORMATION

FIELD OF THE INVENTION

[0001] The present invention relates to the field of semiconductor devices, particularly to improved photodiodes having greater charge capacity for use in imaging devices.

BACKGROUND OF THE INVENTION

[0002] CMOS imagers are increasingly being used as low cost imaging devices. A CMOS imager circuit includes a focal plane array of pixel cells. Each of the pixel cells includes a photosensitive element, such as a photodiode, photogate, or photoconductor overlying a doped region of a substrate for accumulating photo-generated charge in an underlying portion of the substrate. A readout circuit is connected to each pixel cell and often includes a floating diffusion region for receiving charge from the photosensitive element, and a source follower transistor, which has a gate electrically connected to the floating diffusion region. The imager may also include at least one transistor for transferring charge from the photosensitive element to the floating diffusion region, and a transistor for resetting the floating diffusion region to a predetermined charge level prior to charge transfer. A row select access transistor is also typically used to gate a pixel output signal produced by the source follower transistor. The pixel cell above is often called a CMOS Active Pixel Sensor (APS) cell, which is used to collect light energy and convert it into a readable electrical signal.

[0003] A schematic top view of a portion of a semiconductor wafer fragment containing one exemplary CMOS APS cell is shown in Fig. 1. This CMOS APS cell 10 is a four transistor cell. As it will be described below, the CMOS APS cell 10 shown includes a photodiode 13 formed within a substrate. This photodiode 13 is formed as a pinned photodiode shown in Figure 2. Alternatively, the CMOS APS cell 10 may include a photogate, photoconductor or other photon to charge

converting device, in lieu of a pinned photodiode 13, as the initial accumulating area for photo-generated charge. The photodiode 13 includes a p+ surface layer 5 and an underlying n- region 14.

[0004] The CMOS image sensor 10 of Fig. 1 has a transfer gate 7 for transferring photoelectric charges generated in the n- region 14 to a floating diffusion region (sensing node) 3. The floating diffusion region 3 is further connected to a gate 27 of a source follower transistor. The source follower transistor provides an output signal to a row select access transistor having gate 37 for selectively gating the output signal to terminal 33. A reset transistor having gate 17 resets the floating diffusion region 3 to a specified charge level before each charge transfer from the n- region 14 of the photodiode 13.

[0005] Referring to Fig. 2, pinned photodiode 13 is formed on a p+ substrate base 1, which is beneath a p- epitaxial layer 2 (or p-well surface layer). Typically, the substrate base is p-type and is beneath a p-type epitaxial layer. It is also possible, for example, to have a p-type substrate base beneath p-wells in an n-type epitaxial layer. The n- region 14 underlies the p+ region 5 at a depth in the epitaxial layer 2 above the substrate base 1. The n- region 14 and p+ region 5 of the photodiode 13 are spaced between an isolation region 9 and a charge transfer transistor gate 7. The pinned photodiode 13 has a p+/n-/p- structure.

[0006] The photodiode 13 has two p-type regions 5, 2 having a same potential so that the n- region 14 is fully depleted at a pinning voltage (V_{pin}). The pinned photodiode is termed "pinned" because the potential in the photodiode is pinned to a constant value, V_{pin}, when the photodiode is fully depleted. When the transfer gate 7 is operated, photo-generated charge is transferred from the charge accumulating region 14 to the floating diffusion region 3. A complete transfer of charge takes place when a voltage on the floating diffusion region 3 remains above V_{pin} while the pinned photodiode functions at a voltage below V_{pin}. An incomplete transfer of charge results in image lag.

[0007] The isolation region 9 is typically formed using a conventional shallow trench isolation (STI) process or by using a Local Oxidation of Silicon (LOCOS) process. The floating diffusion region 3 adjacent to the transfer gate 7 is commonly n-type. A translucent or transparent insulating layer (not shown) may also be formed over the CMOS APS cell 10.

[0008] Additionally, impurity doped source/drain regions 32 (Figure 1), having n-type conductivity, are provided on either side of the transistor gates 17, 27, 37. Conventional processing methods are used to form, for example, contacts 32 (Figure 1) in an insulating layer to provide an electrical connection to the source/drain regions 32, the floating diffusion region 3, and other wiring to connect to gates and form other connections in the CMOS APS cell 10.

[0009] Generally, in CMOS pixel cells, such as the CMOS APS cell 10 of Figs. 1 and 2, incident light causes electrons to collect in n- region 14. An output signal produced by the source follower transistor having gate 27 is proportional to the number of electrons to be extracted from the n- region 14. The maximum output signal increases with increased electron capacitance or acceptability of the n-region 14 to acquire electrons. In this example, the p+/n- junction dominates the capacitance of the pinned photodiode 13. The characteristics of a p/n junction are well known.

[0010] At least approximately 30,000 electrons are needed to generate an adequate photosignal. Even as pixel size and, therefore, photodiode size, scale down, the number of electrons needed for an adequate photosignal remains the same. Decreasing the size of a conventional photodiode decreases its electron capacitance, leading to an inadequate photosignal. Accordingly, a pinned photodiode for use in a CMOS APS cell that permits decreased pixel size without decreasing electron capacity or increasing the pinning voltage is desired.

BRIEF SUMMARY OF THE INVENTION

[0011] The invention provides a pinned photodiode that has an increased electron capacitance without an increased pinning voltage, and a method for forming the same.

[0012] The invention provides a pinned photodiode structure comprising a substrate base over which is a first layer of semiconductor material. There is a base layer of a first conductivity type, wherein the base layer of a first conductivity type is the substrate base or is a doped layer over the substrate base. At least one doped region of a second conductivity type is below the surface of said first layer, and extends to form a first junction with the base layer. A doped surface layer of a first conductivity type is over the at least one region of a second conductivity type and forms a second photoconversion junction.

[0013] According to the invention, charge storage capacity for the photodiode is increased by extending the charge collection region thereof to the substrate base. These and other features of the invention will be more apparent from the following detailed description that is provided in connection with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

[0014] Fig. 1 is a top plan view of an exemplary CMOS APS cell.

[0015] Fig. 2 is a cross-sectional view of the CMOS APS cell of Fig. 1 along line AA'.

[0016] Fig. 3 is a cross-sectional view of a CMOS APS cell illustrating a pinned photodiode according to one embodiment of the invention.

[0017] Fig. 4A is a cross-sectional view of a CMOS APS cell of Fig. 3 illustrating the fabrication of a pinned photodiode according to the first embodiment at an initial stage of the process.

[0018] Fig. 4B is a cross-sectional view of a CMOS APS cell of Fig. 3 illustrating the fabrication of a pinned photodiode at a stage of the process subsequent to that shown in Fig. 4A.

[0019] Fig. 4C is a cross-sectional view of a CMOS APS cell of Fig. 3 illustrating the fabrication of a pinned photodiode at a stage of the process subsequent to that shown in Fig. 4B.

[0020] Fig. 4D is a cross-sectional view of a CMOS APS cell of Fig. 3 illustrating the fabrication of a pinned photodiode at a stage of the process subsequent to that shown in Fig. 4C.

[0021] Fig. 5 is a graph representing the pinning voltage versus the capacitance of a conventional pinned photodiode and the capacitance of a photodiode according an embodiment of the invention.

[0022] Fig. 6 is a cross-sectional view of a CMOS APS cell illustrating a pinned photodiode according to another embodiment of the invention.

[0023] Fig. 7A is a cross-sectional view of a CMOS APS cell of Fig. 6 illustrating the fabrication of a pinned photodiode at an initial stage of the process.

[0024] Fig. 7B is a cross-sectional view of a CMOS APS cell of Fig. 6 illustrating the fabrication of a pinned photodiode at a stage of the process subsequent to that shown in Fig. 7A.

[0025] Fig. 7C is a cross-sectional view of a CMOS APS cell of Fig. 6 illustrating the fabrication of a pinned photodiode at a stage of the process subsequent to that shown in Fig. 7B.

[0026] Fig. 7D is a cross-sectional view of a CMOS APS cell of Fig. 6 illustrating the fabrication of a pinned photodiode at a stage of the process subsequent to that shown in Fig. 7C.

[0027] Fig. 7E is a cross-sectional view of a CMOS APS cell of Fig. 6 illustrating the fabrication of a pinned photodiode at a stage of the process subsequent to that shown in Fig. 7D.

[0028] Fig. 8 is a graph representing the pinning voltage versus the capacitance of a conventional pinned photodiode and the capacitance of a photodiode according to another embodiment of the invention.

[0029] Fig. 9 illustrates a schematic diagram of a computer processor system incorporating a CMOS imager device containing one or more pixel cells according to the present invention.

DETAILED DESCRIPTION OF THE INVENTION

[0030] In the following detailed description, reference is made to the accompanying drawings, which form a part hereof, to illustrate specific embodiments of the invention. These embodiments are described in sufficient detail to enable one of ordinary skill in the art to practice the invention. It is to be understood that other embodiments may be utilized, and that structural, logical, and electrical changes may be made without departing from the spirit and scope of the present invention.

[0031] The terms "wafer" and "substrate" denote a semiconductor-based material including silicon, silicon-on-insulator (SOI), silicon-on-sapphire (SOS) technology, doped and undoped semiconductors, epitaxial layers of silicon supported by a base semiconductor foundation, and other semiconductor structures. Also, a "wafer" or "substrate" may have been previously processed to form regions or junctions in or over the base semiconductor structure or foundation. Additionally, the semiconductor need not be silicon based. Instead it may be based on silicon-germanium, silicon-on-insulator, silicon-on-sapphire, germanium, gallium arsenide, or others. The term "substrate base" refers to a base semiconductor structure or foundation an epitaxial layer(s) and/or other semiconductor structures.

[0032] The term "pixel" refers to a picture element unit cell containing a photosensor and transistors for converting electromagnetic radiation into an

electrical signal. Representative pixels and their formation are illustrated in the figures and description herein and the fabrication of all pixels in an imager typically will proceed simultaneously in a similar fashion.

[0033] In the drawings, like elements are designated by like reference numerals. Fig. 3 and Fig. 6 illustrate two exemplary embodiments of CMOS APS cells 330 (Fig. 3) and 660 (Fig. 6) having respective pinned photodiodes 331 and 661 constructed according to the invention.

[0034] The pinned photodiode 331 depicted in Fig. 3 includes an n-region 340 that is laterally displaced from the gate 307 of a transistor and extends from a p+ surface layer 305 to a p+ substrate base 301. The resultant pinned photodiode 331 has a p+ (surface)/n-/p+ (substrate) structure, including two p+/n- junctions.

[0035] The formation of the pinned photodiode 331 (Fig. 3) will be described with reference to Figs. 4A-4D. Fig. 4A illustrates a wafer along a same cross-sectional view as shown in Fig. 2. There is a substrate base 301 of a first conductivity type. The substrate base 301 may be provided with the wafer. Instead of a substrate base 301 of a first conductivity type, there may be a base layer of a first conductivity type that is implanted beneath the photodiode 331 by conventional methods before or after the formation of photodiode 331. For simplicity, in this example, the substrate base 301 is provided with the wafer and is described prior to the formation of the photodiode 331. Preferably, the substrate base 301 is a highly doped p+ substrate base 301 having an active dopant concentration within the range of approximately 1×10^{17} to 1×10^{20} atoms per cm^3, and more specifically within the range of approximately 5×10^{17} to 1×10^{19} atoms per cm^3. Over the substrate base 301 a p-type epitaxial layer 302 is formed.

[0036] Fig. 4A also shows an isolation region 309. An isolation region 309 is formed within the epitaxial layer 302 and is filled with a dielectric material, which may include an oxide, such as SiO or SiO_2; oxynitride; a nitride, such as

silicon nitride; silicon carbide; a high temperature polymer; or other suitable material. Preferably, as in this example, the isolation region is a shallow trench isolation (STI) region 309, formed by known STI processes.

[0037] Further illustrated in Fig. 4A is a gate 307 of a transfer transistor formed over the epitaxial layer 302. As shown in Fig. 4A, the gate 307 may be a multilayer transfer gate stack comprising a first insulating layer 307a of grown or deposited silicon oxide on the epitaxial layer 304, a conductive layer 307b of doped polysilicon or other suitable conductive material, and a second insulating layer 307c, which may be formed of an oxide (SiO_2), a nitride (silicon nitride), an oxynitride (silicon oxynitride), ON (oxide-nitride), NO (nitride-oxide), or ONO (oxide-nitride-oxide). The first and second insulating layers, 307a and 307c, and the conductive layer 307b may be formed by conventional deposition methods, such as chemical vapor deposition (CVD) or plasma chemical vapor deposition (PECVD), among others.

[0038] Also, a silicide layer (not shown) may be formed between the conductive layer 307b and the second insulating layer 307c. The silicide layer may be included in all of the transistor gate structures in an imager circuit and may be titanium silicide, tungsten silicide, cobalt silicide, molybdenum silicide, or tantalum silicide. This additional conductive layer may also be a barrier layer/refractor metal, such as TiN/W or $W/N_x/W$, or it could be formed entirely of WN_x.

[0039] Referring to Fig. 4B, after formation of the STI region 309 and gate 307, an implantation mask 315 is formed in a pattern over the wafer, providing an opening 316 to an area between an edge of the gate 307 and the STI region 309 where a charge accumulation region of a photodiode 331 is to be formed. The implantation mask 315 may be formed of photoresist according to techniques known in the art. As shown in Fig. 4B, on one side, the implantation mask 315 is approximately coincident with an edge of the gate 307. On the other side, the implantation mask 316 overlaps the STI region 309, but does not extend past an

edge of the STI region 309 adjacent to where a charge accumulation region of a photodiode 331 is to be formed.

[0040] Next, a dopant of a second conductivity type is implanted through the opening 316 and into the epitaxial layer 302. Preferably, the dopant is n-type, such as phosphorus, arsenic or antimony. A lightly doped n- region 340 is implanted from a point below the surface of the epitaxial layer 302 continuing to the substrate base 301. Thereby, the n- region 340 and the substrate base 301 form an n-/p+ junction. Preferably, the n-/p+ (substrate base) junction is at a depth that is approximately at or above an absorption depth of red light.

[0041] It should be noted that if the substrate base 301 is instead a p+ base layer implanted before or after photodiode 331 is formed, the n-region 340 would form a junction the p+ base layer.

[0042] The n- region 340 is aligned with an edge of the gate 307 and forms a photosensitive charge storage region for collecting photo-generated electrons. Multiple implants may be used to tailor the profile of the n- region 340. Also, an angled implantation may also be conducted to form the n- region 340, such that implantation is carried out at angles other than 90 degrees relative to the surface of the epitaxial layer 302.

[0043] The active dopant concentration in the n- region 340 may be within the range of approximately 1×10^{15} to 5×10^{18} atoms per cm^3, and more specifically within the range of approximately 5×10^{15} to 1×10^{18} atoms per cm^3. The active dopant concentration in the n- region 340 may also be chosen depending on the dimensions of the n- region 340 to result in a desired pinned potential. If desired, the n- concentration may be dropped or increased to result in a lower or higher pinned potential, respectively.

[0044] Next, a dopant of a first conductivity type is implanted through the opening 316 into the epitaxial layer 302, as shown in Fig. 4C. Preferably, a p-type dopant, such as boron, beryllium, indium or magnesium, is used to form a highly

doped p+ surface layer 305 over the n- region 340 and forming a junction with the n- region 340. Preferably, the active dopant concentration of the p+ surface layer 305 is within the range of approximately 1×10^{17} to 1×10^{20} atoms per cm^3, and more specifically within the range of approximately 5×10^{17} to 1×10^{19} atoms per cm^3. Subsequently, the implantation mask 315 is removed by conventional methods to complete the formation of the pinned photodiode 331.

[0045] The p+ surface layer 305 may also be formed by other known techniques. For example, the p+ surface layer 305 may be formed by a gas source plasma doping process, or by diffusing a p-type dopant into the epitaxial layer 302 from an in-situ doped layer or a doped oxide layer deposited over the area where photodiode 331 is to be formed.

[0046] As shown in Fig. 4D, a floating diffusion region 303 may then be formed by known methods as a doped region of n-type conductivity in the epitaxial layer 302 adjacent to the gate 307 and on an opposite side of the gate 307 from the photodiode 331. Sidewall spacers 308 may also be formed on the sidewall of the gate 307 by conventional methods.

[0047] Devices of a CMOS APS cell, including a reset transistor, a source follower transistor, and a row select transistor are formed by methods known in the art (not shown). Further processing may also be employed to form other conventional features of a CMOS APS cell.

[0048] The resultant pinned photodiode 331 has a p+ (surface)/n-/p+ (substrate base) structure, with two p+/n- junctions because the n- region 340 extends to the substrate base 301. Fig. 5 illustrates the relationship between charge capacitance (C) and pinning voltage (V_{pin}) of the photodiode 331 (Fig. 3), represented by lines 12 and 12b, and a conventional photodiode 13 (Fig. 2), represented by line 11. For a same charge capacity, defined as the area under the C-V curve, the pinned voltage V_{pin2} of photodiode 331, line 12a, is lower than the pinned voltage V_{pin1} of a conventional photodiode 13, line 11. For a same pinned

voltage V_{pin2}, the charge capacity of photodiode 331, line 12b, is higher than the charge capacity of conventional photodiode 13, line 11.

[0049] Additionally, the pinned photodiode 331 has an overall performance advantage over the conventional pinned photodiode 13 (Fig. 2) under certain conditions described below.

[0050] A pinned voltage, or pinned potential, is proportional to both the thickness and doping concentration of the n- region 340. Also, a pinned voltage is limited to a voltage below a CMOS imager operating voltage. Therefore, the n-region 340 doping concentration may be decreased to achieve a lower targeted pinned voltage. If, however, the n- region 340 doping concentration is decreased past an optimal range, the charge capacity advantage of the photodiode 331 is diminished.

[0051] Reducing photodiode dimensions leads to a decreased pinned voltage. Therefore, at a smaller size the pinned photodiode 331 will have higher n-region 340 doping concentration and higher capacitance at a same targeted pinned voltage. Thereby the photodiode 331 has a charge capacity advantage over conventional photodiode 13 is preserved.

[0052] As noted above in connection with Fig. 4B, preferably a depth of the n-/p+ (substrate base) junction of photodiode 331 is approximately at or above the absorption depth of red light. Such a placement of the n-/p+ (substrate base) junction prevents photodiode response and Quantum Efficiency degradation for red light. The absorption depth of red light is chosen because it is higher/deeper than the absorption depths of either green or blue wavelength light. For a smaller/shallower red light absorption depth, the n- region 340 doping concentration can be higher for a same pinned voltage, preserving the charge capacity advantage of photodiode 331 over conventional photodiode 13 is preserved.

[0053] Therefore, the pinned photodiode of embodiment 331 is effective at very small photodiode dimensions, 1 micron x 1 micron and below; for semiconductor materials having a higher absorption coefficient than silicon in the visible wavelength range, such as silicon-germanium alloy or semiconductors of III-V material system; and/or when some quantum efficiency loss is acceptable.

[0054] In addition to increased charge capacity, this embodiment may reduce dark current and cross-talk. Dark current should be reduced because to achieve a same electron storage capacity, photodiode 331 will make better use of the pixel volume it occupies and, therefore, may have a lower n- concentration. In an abrupt p+/n- junction, the lower doped side will determine the junction leakage. Also, cross-talk may be prevented because the n- region 340 extends to the substrate base collecting electrons in an area closer to the substrate base 301, which in a conventional photodiode, may diffuse into another pixel.

[0055] Fig. 6 depicts a more complex second embodiment of a pinned photodiode 661 in accordance with the invention. Photodiode 661 is located between a gate 607 of a transfer transistor and a STI region 609, and includes an intermediate p- region 670 partially separating a surface n- region 651 and a base n- region 652, which remain connected along edges thereof. The surface n- region 651 forms a junction with a p+ surface layer 605, and the base n- region 652 forms a junction with the p+ substrate base 601.

[0056] Formation of the pinned photodiode 661 will be described with reference to Figs. 7A-7E. Referring to Fig. 7A, a substrate base 601 of a first conductivity type is provided. The substrate base 601 may be provided with the wafer. Instead of a substrate base 601 of a first conductivity type, there may be a base layer of a first conductivity type that is implanted beneath the photodiode 661 by conventional methods before or after the formation of photodiode 661. For simplicity, in this example, the substrate base 601 is provided with the wafer and is described prior to the formation of the photodiode 661. Preferably, the substrate

base 601 is a highly doped p+ substrate base 601 having an active dopant concentration within the range of approximately 1 x 10^{17} to 1 x 10^{20} atoms per cm^3, and more specifically within the range of approximately 5 x 10^{17} to 1 x 10^{19} atoms per cm^3.

[0057] A p-type epitaxial layer 602 is grown over the substrate base 601. Fig. 7A also illustrates a STI region 609 and a gate 607, which may be formed as described in connection with Fig 4A above.

[0058] Referring to Fig. 7B, after formation of the STI region 609 and gate 607, a first implantation mask 615 is formed over the wafer according to techniques known in the art. The first implantation mask 615 is patterned to provide an opening 616 to an area between an edge of the gate 607 and the STI region 609 where a charge accumulation region of a pinned photodiode 661 is to be formed. The first implantation mask 615 may be formed of photoresist. As shown in Fig. 7B, on one side, the first implantation mask 615 is approximately coincident with the edge of the gate 607. On the other side, the first implantation mask 615 overlaps the STI region 609, but does not extend past an edge of the STI region 609 adjacent to where a charge accumulation region of a photodiode 661 is to be formed.

[0059] Next, a dopant of a second conductivity type is implanted through the opening 616 into the epitaxial layer 602. Preferably, the dopant is n-type, such as phosphorus, arsenic or antimony. A lightly doped n- region 650 is implanted from a point below the surface of the epitaxial layer 602 continuing to the substrate base 601. Thereby, the n- region 650 and the substrate base 601 form an n-/p+ junction. Preferably, the n-/p+ (substrate base) junction is at a depth that is approximately at or above an absorption depth of red light.

[0060] It should be noted that if the substrate base 601 is instead a p+ base layer implanted before or after photodiode 661 is formed, the n-region 650 would form a junction the p+ base layer.

[0061] The n- region 650 is aligned with an edge of the gate 607 and forms a photosensitive charge storage region for collecting photo-generated electrons. The active dopant concentration in the n- region 650 may be within the range of approximately 1×10^{15} to 5×10^{18} atoms per cm^3, and more specifically within the range of approximately 5×10^{15} to 1×10^{18} atoms per cm^3. Multiple implants may be used to tailor the profile of the n- region 650. Also, an angled implantation may also be conducted to form the n- region 650, such that implantation is carried out at angles other than 90 degrees relative to the surface of the epitaxial layer 602. The first implantation mask 615 is then removed by conventional methods.

[0062] Referring to Fig. 7C, a second implantation mask 625 is formed over the wafer by conventional methods and patterned to have an opening 626 over the n- region 650. The second implantation mask 625 may also be a layer of photoresist. On one side, the second implantation mask 625 overlaps the STI region 609, but does not extend over the photodiode area. On the other side the second implantation mask 625 extends a distance D past an edge of gate 607 over a portion of the n- region 650.

[0063] Thereafter, an intermediate portion of the n- region 650 is counterdoped by implanting a dopant of a first conductivity type. Preferably, the dopant is a p-type dopant, such as boron, beryllium, indium or magnesium. As shown in Fig. 7C, a lightly doped intermediate p- region 670 is formed in the n- region 650 such that it meets a p-type portion of the epitaxial layer 602 on a lateral edge thereof. In this embodiment, the intermediate p- region 670 meets a p-type portion of the epitaxial layer 602 on a lateral edge thereof adjacent to the STI region 609. Multiple implants may be used to tailor the profile of the intermediate p- region 670. Also, an angled implantation may also be conducted to form the intermediate p- region 670, such that implantation is carried out at angles other than 90 degrees relative to the surface of the epitaxial layer 602.

[0064] The active dopant concentration of the intermediate p- region 670 may be within the range of approximately 1 x 10^{15} to 5 x 10^{17} atoms per cm^3, and more specifically within the range of approximately 5 x 10^{15} and 1 x 10^{17} atoms per cm^3. Also, the intermediate p- region may instead be a highly doped intermediate p+ region having an active dopant concentration similar to that of the substrate base 601 and the surface p+ region 605. In such a case, the active dopant concentration of the intermediate p+ region 670 may be within the range of approximately 1 x 10^{17} to 1 x 10^{20} atoms per cm^3, and more specifically within the range of approximately 5 x 10^{17} to 1 x 10^{19} atoms per cm^3.

[0065] The formation of the intermediate p- region 670 also forms two n- regions: a surface n- region 651 and a base n- region 652, which are partially separated by the intermediate p- region 670. The two n-regions 651 and 652 remain connected along at least one edge thereof. Preferably, the n- regions 651 and 652 are connected along at least one edge thereof on a side aligned with the gate 607, causing the n- regions 651 and 652, considered as a whole, to have a reverse C-shape as viewed from the perspective shown in Fig. 6. Subsequently, the second implantation mask 625 is removed using conventional techniques.

[0066] As noted above, the active dopant concentration in the n- region 650 (Fig. 7B) may be within the range of approximately 1 x 10^{15} to 5 x 10^{18} atoms per cm^3, and more specifically within the range of approximately 5 x 10^{15} to 1 x 10^{18} atoms per cm^3. The active dopant concentration in the n- region 650 may also be chosen depending on the dimensions of the n- regions 651 and 652 to result in a desired pinned potential. If desired, the n- concentration may be dropped or increased to result in a lower or higher pinned potential, respectively.

[0067] Referring to Fig. 7D, next, a third implantation mask 635 is formed over the wafer by conventional methods and is patterned to form an opening 636 that is similar to that of the opening 616 of the first implantation mask 615 (Fig. 7B). The third implantation mask 635 may also be a layer of photoresist.

Then, a dopant of a first conductivity type is implanted through the opening 636 into the epitaxial layer 602. Preferably the dopant is a p-type dopant such as boron, beryllium, indium or magnesium, and a highly doped p+ surface layer 605 is formed over the n- region 651, such that the p+ surface layer 605 forms a junction with the surface n- region 651.

[0068] Preferably, the active dopant concentration of the p+ surface layer 605 is within the range of approximately 1×10^{17} to 1×10^{20} atoms per cm^3, and more specifically within the range of approximately 5×10^{17} to 1×10^{19} atoms per cm^3. The p+ surface layer 605 may also be formed by other known techniques. For example, the p+ surface layer 605 may be formed by a gas source plasma doping process, or by diffusing a p-type dopant into the epitaxial layer 302 from an in-situ doped layer or a doped oxide layer deposited over the area where the photodiode 661 is to be formed.

[0069] As shown in Fig. 7E, a floating diffusion region 603 may then be formed by known methods as a doped region of n-type conductivity in the epitaxial layer 602 adjacent to the gate 607 and on an opposite side of the gate 607 from the photodiode 661. Sidewall spacers 608 may also be formed on the sidewall of the gate 607 by conventional methods.

[0070] Devices of a CMOS APS cell, including a reset transistor, a source follower transistor, and a row select transistor are formed by methods known in the art (not shown). Further processing may also be employed to form other conventional features of a CMOS APS cell.

[0071] The resultant pinned photodiode 661 includes two high capacitance p+/n- junctions and has approximately double the capacitance of the conventional pinned photodiode 13 (Fig. 2). Fig. 8 illustrates the relationship between charge capacitance (C) and pinning voltage (V_{pin}) of the photodiode 661 (Fig. 6), represented by line 15, and a conventional photodiode 13 (Fig. 2), represented by line 11. At a same voltage V_1, the capacitance of the photodiode 661

is approximately double that of the photodiode 13 of the prior art below a pinned voltage V_{pin3}. Therefore, the charge capacity, defined as the area under the C-V curve, of photodiode 661 is higher than the charge capacity of conventional photodiode 13. Accordingly, the photodiode 661 can provide an adequate photosignal at a smaller size than a conventional photodiode 13.

[0072] Preferably, the pinned potentials of the two n- regions 651 and 652 will be similar to avoid image lag. Additionally, the surface n- region 651 may have a V_{pin} higher than that of the base n- region 652 to ensure complete charge transfer and avoid image lag. In addition to increased charge capacity, this embodiment may provide reduced cross-talk because the n- region 652 extends to the substrate base, better preventing electrons from diffusing from one pixel to another.

[0073] Although the invention is described as being formed using a p- epitaxial layer over a p+ substrate, it may also be formed using an n- epitaxial layer over a p+ substrate. As known in the art, acceptor regions would be implanted where the potential barrier to electrons would be formed, and n-wells and p-wells would be implanted where MOS transistors would be formed.

[0074] Also, while the above embodiments are described in connection with the formation of pnp-type photodiodes the invention is not limited to these embodiments. The invention also has applicability to photodiodes formed from npn regions in a substrate. The dopant and conductivity types of all structures would change accordingly, with the transfer gate being part of a PMOS transistor, rather than an NMOS transistor as in the embodiments described above.

[0075] In addition, although the invention is described in connection with a four-transistor (4T) pixel cell employing a transfer transistor having a transfer gate 307, 607, the invention may also be incorporated into a three-transistor (3T) cell, or into a five-transistor (5T) cell. A 3T cell differs from the 4T cell by the omission of the charge transfer transistor and associated gate 307, 607, and the coupling of the n

regions of the photodiode and the floating diffusion regions through an overlap of the two or an n region bridging the two, which is well known in the art. A 5T cell differs from the 4T cell by the addition of a shutter transistor or a CMOS photogate transistor.

[0076] A typical processor-based system 988 including a CMOS imager device 981 having an array of pixels, which includes pixels according to the embodiments of the present invention, is illustrated generally in Fig. 9. A processor-based system 988 is exemplary of a system having digital circuits that could include CMOS imager devices. Without being limiting, such a system could include a computer system, camera system, scanner, machine vision, vehicle navigation, video phone, surveillance system, auto focus system, star tracker system, motion detection system, image stabilization system, and data compression system.

[0077] A processor-based system, for example a computer system, generally comprises a central processing unit (CPU) 986, such as a microprocessor, that communicates with an input/output (I/O) device 982 over a bus 989. The CMOS imager 981, which produces an image output from a pixel array, also communicates with the system 988 over bus 989. The processor-based system 988 also includes random access memory (RAM) 983, and may include peripheral devices, such as a floppy disk drive 984 and a compact disk (CD) ROM drive 984, which also communicate with CPU 986 over the bus 989. The CMOS imager 981 may be combined with a processor; such as a CPU, digital signal processor, or microprocessor; with or without memory storage on a single integrated circuit or on a different chip than the processor.

[0078] It is again noted that the above description and drawings are exemplary and illustrate preferred embodiments that achieve the objects, features and advantages of the present invention. It is not intended that the present invention be limited to the illustrated embodiments. Any modification of the present invention which comes within the spirit and scope of the following claims should be considered part of the present invention.

CLAIMS

[0079] What is claimed as new and desired to be protected by Letters Patent of the United States is:

1. A photodiode comprising:

a substrate base;

a first layer of semiconductor material over the substrate base;

a base layer of a first conductivity type, wherein the base layer of a first conductivity type is the substrate base or is a doped layer over the substrate base;

at least one doped region of a second conductivity type below the surface of the first layer, wherein at least one of said regions of a second conductivity type forms a first junction with the base layer;

a doped surface layer of a first conductivity type over the at least one region of a second conductivity type and forming a second junction with at least one of the regions of a second conductivity type.

2. The photodiode of claim 1, wherein the first and second conductivity types are p and n respectively.

3. The photodiode of claim 1, wherein the photodiode is a pinned photodiode.

4. The photodiode of claim 1, wherein the base layer is a p+ base layer, the at least one doped region of a second conductivity type is an n- region, and the doped surface layer is a p+ surface layer.

5. The photodiode of claim 1, wherein the base layer and the doped surface layer have an active dopant concentration within the range of approximately 1 x 10^{17} to approximately 1 x 10^{20} atoms per cm^3.

6. The photodiode of claim 1, wherein the at least one doped region of a second conductivity type has an active dopant concentration within the range of approximately 1 x 10^{15} to approximately 5 x 10^{18} atoms per cm^3.

7. The photodiode of claim 1, wherein the first junction between the at least one of said regions of a second conductivity type and the base layer is at a depth approximately at or above an absorption depth of red light.

8. The photodiode of claim 1, having one doped region of a second conductivity type.

9. The photodiode of claim 1, having at least two doped regions of a second conductivity type, and further comprising at least one doped intermediate region of a first conductivity type partially separating the at least two regions of a second conductivity type.

10. The photodiode of claim 9, wherein the at least two regions of a second conductivity type are vertically spaced below the surface of said first layer, and wherein one of said regions of a second conductivity type forms a junction with the base layer and

another of said regions of a second conductivity type forms a junction with the doped surface layer.

11. The photodiode of claim 9, wherein the at least two regions of a second conductivity type are connected along at least one edge thereof.

12. The photodiode of claim 9, wherein the at least one doped intermediate region has an active dopant concentration with the range of approximately 1 x 10^{15} to approximately 5x 10^{17} atoms per cm^3.

13. A photodiode comprising:

a substrate base;

a first layer of semiconductor material over the substrate base;

a base layer of a first conductivity type, wherein the base layer of a first conductivity type is the substrate base or is a doped layer over the substrate base;

a doped region of a second conductivity type below a surface of said first layer, wherein the region of a second conductivity type extends to the base layer and forms a junction with the base layer;

a doped surface layer of a first conductivity type over the region of a second conductivity type forming a junction with the region of a second conductivity type.

14. A photodiode comprising:

a substrate base;

a first layer of semiconductor material over the substrate base;

a base layer of a first conductivity type, wherein the base layer of a first conductivity type is the substrate base or is a doped layer over the substrate base;

two doped regions of a second conductivity type below a surface of said first layer and vertically spaced over the base layer, wherein the two regions of a second conductivity type are connected along at least one edge thereof, and wherein one of the two regions of a second conductivity type forms a junction with the base layer;

an intermediate doped region of a first conductivity type partially separating the two regions of a second conductivity type; and

a doped surface layer of a first conductivity type over the region of a second conductivity type furthest from the base layer and forming a junction with the region of a second conductivity type furthest from the base layer.

15. A pixel cell, comprising:

a substrate base;

a first layer of semiconductor material over the substrate base;

a base layer of a first conductivity type, wherein the base layer of a first conductivity type is the substrate base or is a doped layer over the substrate base;

a gate of a transistor formed over the first layer;

a field isolation region formed in the first layer; and

a photodiode adjacent to the field isolation region, the photodiode comprising at least one doped region of a second conductivity type below the surface of the first layer, wherein at least one of the regions of a second conductivity type forms a first junction with the base layer, and a doped surface layer of a first conductivity type over the at least one region of a second conductivity type forming a second junction with at least one of the regions of a second conductivity type.

16. The pixel cell of claim 15, wherein the first and second conductivity types are p and n respectively.

17. The pixel cell of claim 15, wherein the photodiode is a pinned photodiode.

18. The pixel cell of claim 15, wherein the base layer is a p+ base layer, the at least one doped region of a second conductivity type is an n- region, and the doped surface layer is a p+ surface layer.

19. The pixel cell of claim 15, having one doped region of a second conductivity type.

20. The pixel cell of claim 15, having at least two doped regions of a second conductivity type vertically spaced below the surface of said first layer, wherein one of said regions of a second conductivity type forms the first junction with the base layer and another of said regions of a second conductivity type forms the second junction with the doped surface layer.

21. The pixel cell of claim 20, further comprising at least one doped intermediate region of a first conductivity type partially separating the at least two regions of a second conductivity type.

22. The pixel cell of claim 20, wherein the at least two regions of a second conductivity type are connected along at least one edge thereof.

23. The pixel cell of claim 20, wherein the region of a second conductivity type forming the second junction with the doped surface layer has a higher pinned potential than does the region of a second conductivity type forming the first junction with the substrate base.

24. The pixel cell of claim 15, wherein said transistor is a transfer transistor which is part of a 4T pixel cell.

25. A CMOS imager system, comprising:

(i) a processor; and

(ii) a CMOS imaging device coupled to the processor, the CMOS imaging device comprising:

a substrate base;

a first layer of semiconductor material over the base layer;

a base layer of a first conductivity type, wherein the base layer of a first conductivity type is the substrate base or is a doped layer over the substrate base;

a field isolation region formed in the first layer; and

a pixel adjacent to the field isolation region, the pixel comprising a gate of a transistor formed over the first layer, and a photodiode, the photodiode comprising at least one doped region of a second conductivity type below the surface of the first layer, wherein at least one of the regions of a second conductivity type forms a first junction with the base layer, and a doped surface layer of a first conductivity type over the at least one region of a second conductivity type and forming a second junction with at least one of the regions of a second conductivity type.

26. The system of claim 25, wherein the first and second conductivity types are p and n respectively.

27. The system of claim 25, wherein the photodiode is a pinned photodiode.

28. The system of claim 25, wherein the base layer is a p+ base layer, the at least one doped region of a second conductivity type is an n- region, and the doped surface layer is a p+ surface layer.

29. The system of claim 25, having one doped region of a second conductivity type.

30. The system of claim 25, having at least two doped regions of a second conductivity type vertically spaced below the surface of said first layer, wherein one of said regions of a second conductivity type forms the first junction with the base layer and

another of said regions of a second conductivity type forms the second junction with the doped surface layer.

31. The system of claim 30, further comprising at least one doped intermediate region of a first conductivity type partially separating the at least two regions of a second conductivity type.

32. The system of claim 30, wherein the at least two regions of a second conductivity type are connected along at least one edge thereof.

33. The system of claim 30, wherein the region of a second conductivity type forming the second junction with the doped surface layer has a higher pinned potential than does the region of a second conductivity type forming the first junction with the substrate base.

34. The system of claim 25, wherein said transistor is a transfer transistor which is part of a 4T pixel cell.

35. A method of forming a photodiode comprising:

providing a substrate base;

forming a first layer of semiconductor material over the base layer;

forming or providing a base layer of a first conductivity type, wherein the base layer of a first conductivity type is either provided with the substrate base or is a doped layer formed over the substrate base;

forming at least one doped region of a second conductivity type below the surface of said first layer, wherein at least one of said regions of a second conductivity type forms a first junction with the base layer;

forming a doped surface layer of a first conductivity type over the at least one region of a second conductivity type, such that the doped surface layer forms a second junction with at least one region of a second conductivity type.

36. The method of claim 35, wherein the first and second conductivity types are p and n respectively.

37. The method of claim 35, wherein the photodiode is formed as a pinned photodiode.

38. The method of claim 35, wherein a p+ base layer is provided or formed, the at least one doped region of a second conductivity type is formed as an n- region, and the doped surface layer is formed as a p+ surface layer.

39. The method of claim 35, wherein the base layer and the doped layer of a first conductivity type have an active dopant concentration within the range of approximately 1×10^{17} to approximately 1×10^{20} atoms per cm^3.

40. The method of claim 35, wherein the at least one doped region of a second conductivity type is formed having an active dopant concentration within the range of approximately 1×10^{15} to approximately 5×10^{18} atoms per cm^3.

41. The method of claim 35, wherein the first junction between the at least one of said regions of a second conductivity type and the base layer is at a depth approximately at or above an absorption depth of red light.

42. The method of claim 35, wherein one doped region of a second conductivity type is formed below a surface of said first layer.

43. The method of claim 35, wherein at least two doped regions of a second conductivity type are formed below a surface of said first layer, and further comprising forming at least one doped intermediate region of a first conductivity type partially separating the at least two regions of a second conductivity type.

44. The method of claim 43, wherein the at least two regions of a second conductivity type are formed vertically spaced below the surface of said first layer, such that one of said regions of a second conductivity type forms the first junction with the base layer and another of said regions of a second conductivity type forms the second junction with the doped surface layer.

45. The method of claim 43, wherein the at least two regions of a second conductivity type are connected along at least one edge thereof.

46. The method of claim 43, wherein the at least one doped intermediate region of a first conductivity type has an active

dopant concentration with the range of approximately 1×10^{15} to approximately 5×10^{17} atoms per cm^3.

47. A method of forming a pixel cell, comprising:

providing a substrate base;

forming a first layer of semiconductor material over the base layer;

providing or forming a base layer of a first conductivity type, wherein the base layer of a first conductivity type is provided with the substrate base or is a doped layer formed over the substrate base;

forming a gate of a transistor over said first layer;

forming a field isolation region in the first layer; and

forming a photodiode adjacent to the field isolation region, the photodiode comprising at least one doped region of a second conductivity type below the surface of the first layer, wherein at least one of said regions of a second conductivity type forms a first junction with the base layer, and a doped surface layer of a first conductivity type over the at least one region of a second conductivity type forming a second junction with at least one of the regions of a second conductivity type.

48. The method of claim 47, wherein the first and second conductivity types are p and n respectively.

49. The method of claim 47, wherein the photodiode is a pinned photodiode.

50. The method of claim 47, wherein a p+ base layer is provided or formed, and wherein the at least one doped region of a second

conductivity type is an n- region, and the doped surface layer is a p+ surface layer.

51. The method of claim 47, wherein the photodiode is formed having one doped region of a second conductivity type below a surface of said first layer.

52. The method of claim 47, wherein the photodiode is formed having at least two doped regions of a second conductivity type vertically spaced below the surface of said first layer, such that one of said regions of a second conductivity type forms the first junction with the base layer and another of said regions of a second conductivity type forms the second junction with the doped surface layer.

53. The method of claim 52, further comprising at least one doped intermediate region of a first conductivity type partially separating the two regions of a second conductivity type.

54. The method of claim 52, wherein the at least two regions of a second conductivity type are connected along at least one edge thereof.

55. The method of claim 57, wherein said transistor is a transfer transistor which is part of a 4T pixel cell.

56. A method of forming a CMOS imager system, comprising:

(i) providing a processor; and

(ii) providing a CMOS imaging device comprising:

a substrate base;

a first layer of semiconductor material over the base layer;

a base layer of a first conductivity type, wherein the base layer of a first conductivity type is the substrate base or is a doped layer over the substrate base;

a field isolation region formed in the first layer; and

a pixel adjacent to the field isolation region, the pixel comprising a gate of a transistor and a photodiode adjacent to the gate, the photodiode comprising at least one doped region of a second conductivity type below the surface of the first layer, wherein at least one of said regions of a second conductivity type forms a first junction with the base layer, and a doped surface layer of a first conductivity type over the at least one region of a second conductivity type forming a second junction with at least one of the regions of a second conductivity type; and

(iii) coupling the processor to said CMOS imaging device.

57. The method of claim 56, wherein the first and second conductivity types are p and n respectively.

58. The method of claim 56, wherein the photodiode is a pinned photodiode.

59. The method of claim 56, wherein a p+ base layer is provided or formed, and wherein the at least one doped region of a second

conductivity type is an n- region, and the doped surface layer is a p+ surface layer.

60. The method of claim 56, wherein the photodiode has one doped region of a second conductivity type.

61. The method of claim 56, wherein the photodiode has at least two doped regions of a second conductivity type vertically spaced below the surface of said first layer, such that one of said regions of a second conductivity type forms the first junction with the base layer and another of said regions of a second conductivity type forms the second junction with the doped surface layer.

62. The method of claim 61, further comprising at least one doped intermediate region of a first conductivity type partially separating the two regions of a second conductivity type.

63. The method of claim 61, wherein the at least two regions of a second conductivity type are connected along at least one edge thereof.

64. The method of claim 56, wherein said transistor is a transfer transistor which is part of a 4T pixel cell.