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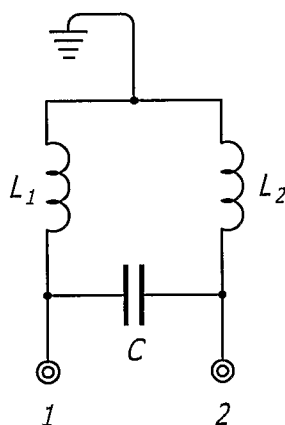
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(54) Title: Q ENHANCEMENT CIRCUIT AND METHOD



(57) Abstract: A Q enhancement circuit and method. In a most general embodiment, the inventive circuit is adapted for use with a component having a parasitic resistance R; a first resistance R1 is disposed in series with the component an arrangement makes the resistance R1 a negative resistance. In the illustrative embodiment, first and second inductors constitute the components for which Q enhancement is effected. A resistance R1 is disposed in series with the first inductor and is equal to the parasitic resistance RL1 thereof. Likewise, a second resistance R2 is disposed in series with the second inductor and is equal to the parasitic resistance RL2 thereof. The Q enhancement circuit further includes a first transistor Q1 and a second transistor Q2.

WO 2006/001878 A1