

SEMICONDUCTOR DEVICE AND METHOD OF MANUFACTURING SEMICONDUCTOR DEVICE

CROSS-REFERENCE TO RELATED APPLICATION

5 [0001] This application claims priority to Korean Patent Application No. 10-2023-0024307 filed on February 23, 2023, which is incorporated herein by reference in its entirety.

BACKGROUND

1. Technical Field

[0002] Embodiments generally relate to an electronic device and a method of manufacturing an electronic device and, more particularly, to a semiconductor device and a method of manufacturing a semiconductor device.

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2. Related Art

[0003] The degree of integration of semiconductor devices is basically determined by the area that is occupied by a unit memory cell. As the improvement of the degree of integration of semiconductor devices in which a memory cell is formed on a substrate as a single layer reaches its limit, a three-dimensional semiconductor device in which memory cells are stacked on a substrate is proposed. Furthermore, to improve operation reliability of such a semiconductor device, various structures and manufacturing methods are developed.

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SUMMARY

[0004] In an embodiment, a semiconductor device may include a gate structure including a cell region and a contact region, a slit structure extending in a first direction through the gate structure, first channel structures disposed in the cell region of the gate structure, and second channel structures disposed in the cell region of the gate structure and disposed to be more adjacent to the contact region of the gate structure than the first channel structures. In a second direction that intersects the first direction, the first channel structures may be spaced apart from the slit structure by a first distance, and the second channel structures may be spaced apart from the slit structure at a second distance, the second distance is greater than the first distance.

[0005] In an embodiment, a semiconductor device may include a first gate structure, first channel structures and second channel structures disposed within the first gate structure, a second gate structure disposed on the first gate structure, third channel structures disposed within the second gate structure and connected to the first channel structures, fourth channel structures disposed within the second gate structure and connected to the second channel structures, and a slit structure disposed within the first gate structure and the second gate structure and extending in a first direction. In a second direction that intersects the first direction, the first channel structures may be

spaced apart from the slit structure by a first distance, and the second channel structures may be spaced apart from the slit structure by a second distance that is greater than the first distance.

[0006] In an embodiment, a method of manufacturing a semiconductor device may include forming a stack, forming first channel structures that extend through the stack, forming second channel structures that extend through the stack, and forming, within the stack, a slit structure that extends in a first direction. In a second direction that intersects the first direction, the first channel structures may be spaced apart from the slit structure by a first distance, and the second channel structures may be spaced apart from the slit structure by a second distance that is greater than the first distance.

[0007] In an embodiment, a method of manufacturing a semiconductor device may include forming a first stack, forming first openings and second openings within the first stack, forming a second stack on the first stack, forming, within the second stack, third openings connected to the first openings, forming, within the second stack, fourth openings connected to the second openings, and forming, within the first stack and the second stack, a slit that extends in a first direction. In a second direction that intersects the first direction, the first openings may be spaced apart from the slit by a first distance, and the second openings may be spaced apart from the slit by a second distance, the second distance is greater than the first distance.

BRIEF DESCRIPTION OF THE DRAWINGS

[0008] FIGS. 1A, 1B, and 1C are diagrams for describing a semiconductor device according to an embodiment of the present disclosure.

[0009] FIGS. 2A and 2B are diagrams for describing a semiconductor device according to an embodiment of the present disclosure.

[0010] FIGS. 3A, 3B, 3C, and 3D are diagrams for describing a semiconductor device according to an embodiment of the present disclosure.

[0011] FIG. 4 is a diagram for describing a semiconductor device according to an embodiment of the present disclosure.

[0012] FIGS. 5A, 5B, 5C, and 5D are diagrams for describing a method of manufacturing a semiconductor device according to an embodiment of the present disclosure.

[0013] FIGS. 6A, 6B, and 6C are diagrams for describing a method of manufacturing a semiconductor device according to an embodiment of the present disclosure.

DETAILED DESCRIPTION

[0014] Hereinafter, embodiments according to the technical spirit of the present disclosure are described with reference to the accompanying drawings.

[0015] Embodiments of the present disclosure may provide a

semiconductor device having a stable structure and improved characteristics and a method of manufacturing a semiconductor device.

5 **[0016]** Various embodiments of the present technology can provide a semiconductor device having a stable structure and improved reliability.

[0017] FIGS. 1A to 1C are diagrams for describing a semiconductor device according to an embodiment of the present disclosure. FIG. 1B may be an enlarged view of A in FIG. 1A. FIG. 1C may be a
10 cross-sectional view of a first channel structure 110R and a second channel structure 110D.

[0018] Referring to FIGS. 1A and 1B, the semiconductor device may include a gate structure 100, the first channel structures 110R, the second channel structures 110D, or slit structures 130 or may include
15 the gate structure 100, the first channel structures 110R, the second channel structures 110D, or the slit structures 130 in combination. The semiconductor device may further include supports 120.

[0019] The gate structure 100 may include a cell region CR and a contact region CTR. The cell region CR may include a first region CR1
20 and a second region CR2. The second region CR2 may be disposed closer to the contact region CTR than the first region CR1. The channel structures 110R and 110D may be disposed in the cell region CR. The supports 120 or contact plugs may be disposed in the contact region CTR. In other words, different structures may be disposed in

the cell region CR and the contact region CTR, respectively, on the basis of a boundary surface between the cell region CR and the contact region CTR, but the present disclosure is not limited thereto. The supports 120 or the contact plugs may be disposed in the cell region CR, and the channel structures 110R and 110D may be disposed in the contact region CTR. The gate structure 100 may include insulating layers 101 and conductive layers 102 that are alternately stacked. In this case, the insulating layers 101 may include an insulating material, such as oxide. The conductive layers 102 may include a conductive material, such as tungsten. The conductive layers 102 may each be a word line or a selection line.

[0020] The slit structures 130 may be disposed within the gate structure 100. The slit structures 130 may extend in a first direction I through the gate structure 100. For example, the slit structures 130 may extend from the cell region CR to the contact region CTR. The slit structures 130 may be disposed in a second direction II that intersects the first direction I by being spaced apart from each other. The slit structures 130 may include an insulating material or a conductive material or may include the insulating material or the conductive material in combination.

[0021] The first channel structures 110R may be disposed in the cell region CR of the gate structure 100. For example, the first channel structures 110R may be disposed in the first region CR1. The second channel structures 110D may be disposed in the cell region CR of the

gate structure 100, and may be disposed to be more adjacent to the contact region CTR of the gate structure 100 than the first channel structures 110R. For example, the second channel structures 110D may be disposed in the second region CR2.

5 **[0022]** The first channel structures 110R may each include a channel layer 110RA. The first channel structures 110R may each further include a memory layer 110RB that surrounds the sidewall of the channel layer 110RA or an insulating core 110RC within the channel layer 110RA or may each further include the memory layer 110RB or
10 the insulating core 110RC in combination. The second channel structures 110D may each include a channel layer 110DA, a memory layer 110DB, or an insulating core 110DC or may each include the channel layer 110DA, the memory layer 110DB, or the insulating core 110DC in combination. Memory cells may be stacked along the
15 channel structures 110R and 110D.

[0023] The second channel structures 110D may be disposed closer to the contact region CTR than the first channel structures 110R. A distance between the first channel structures 110R or the second channel structures 110D and the slit structure 130 may be increased
20 as the first channel structures 110R or the second channel structures 110D become closer to the contact region CTR. For example, in the second direction II, the first channel structures 110R may be spaced apart from the slit structure 130 by a first distance "d1". In the second direction II, the second channel structures 110D may be

spaced apart from the slit structure 130 by a second distance "d2". The first distance "d1" may be substantially the same as or different from the second distance "d2". For example, the second distance "d2" may be greater than the first distance "d1".

5 **[0024]** The form of the slit structure 130 may be influenced by a surrounding environment. If the pattern density of the cell region CR and the pattern density of the contact region CTR are different from each other, the slit structure 130 may be deformed at a boundary between the cell region CR and the contact region CTR at which the
10 pattern density is changed. The term "pattern density" may mean a degree of distribution of structures (patterns) located in region. For example, a first pattern density may mean the degree of distribution of the first channel structures 110R located in the first region CR1, and a second pattern density may mean the degree of distribution of
15 the second channel structures 110D located in the second region CR2. The term "degree of distribution" may mean distance between at least two structures (patterns) or may mean average of distances between two or more structures (patterns). The slit structure 130 may be inclined or some region of the slit structure 130 may protrude.
20 Accordingly, in an embodiment, the distance between the channel structures 110R and 110D and the slit structure 130 may be adjusted so that the deformation of the slit structure 130 attributable to a change in the surrounding pattern is minimized.

[0025] In an embodiment, a change in the form of the slit structure

130 in the boundary surface between the cell region CR and the contact region CTR can be prevented or reduced because the distance between the second channel structures 110D and the slit structure 130 is increased in the second direction II as the second channel structures 110D become closer to the contact region CTR. For example, if the second distance "d2" is substantially the same as the first distance "d1", a form of the slit structure 130 may be changed. However, a change in the form of the slit structure 130 can be reduced because the second channel structures 110D are disposed so that the second distance "d2" is greater than the first distance "d1".

[0026] The first channel structures 110R may be spaced apart from each other at a first interval "r1" in the first direction I, and may be spaced apart from each other at a second interval "r2" in the second direction II. The second channel structures 110D may be spaced apart from each other at a third interval "r3" in the first direction I, and may be spaced apart from each other at a fourth interval "r4" in the second direction II. The first interval "r1" and the third interval "r3" may be substantially the same or different from each other. The second interval "r2" and the fourth interval "r4" may be substantially the same or different from each other.

[0027] The number of channel rows of the first channel structures 110R and the number of channel rows of the second channel structures 110D may be substantially the same or different from each other. In this case, the channel row may include the channel

structures 110R and 110D that are arranged in the first direction I. If the second distance "d2" is greater than the first distance "d1", the interval between the channel rows of the second channel structures 110D may be reduced. Accordingly, the fourth interval "r4" may be smaller than the second interval "r2".

[0028] Furthermore, in order to compensate for a difference between the pattern densities of the first region CR1 and the second region CR2 according to a difference between the second interval "r2" and the fourth interval "r4", the third interval "r3" may be greater than the first interval "r1". Accordingly, a first diagonal line distance S1 between the first channel structures 110R and a second diagonal line distance S2 between the second channel structures 110D may be substantially the same. Furthermore, the pattern density of the first channel structures 110R and the pattern density of the second channel structures 110D may be maintained to be substantially identical to each other.

[0029] The channel structures 110R and 110D may each be a real channel structure or a dummy channel structure. The real channel structure and the dummy channel structure may have similar structures, but electrical connection states of the real channel structure and the dummy channel structure may be different from each other. The real channel structure may be connected between a source line and a bit line. Memory cells that are stacked along the real channel structure may be real memory cells that store data. The

dummy channel structure may have an electrically floated state. Memory cells that are stacked along the dummy channel structure may be dummy memory cells in which data is not stored. In an embodiment, memory cells that are stacked along the dummy channel structure may be dummy memory cells in which data is unable to be stored.

[0030] For example, the first channel structures 110R may each be a real channel structure, and the second channel structures 110D may each be a dummy channel structure. In this case, a distance between the first channel structures 110R and the slit structure 130 may be substantially the same, but the present disclosure is not limited thereto. The distance between the first channel structures 110R and the slit structure 130 may be increased as the first channel structures 110R become closer to the contact region CTR. Furthermore, a distance between the second channel structures 110D and the slit structure 130 may be increased as the second channel structures 110D become closer to the contact region CTR.

[0031] As another example, the first channel structures 110R and the second channel structures 110D may each be a dummy channel structure. In this case, a distance between the first channel structures 110R and the slit structure 130 may be increased as the first channel structures 110R become closer to the contact region CTR. Furthermore, a distance between the second channel structures 110D and the slit structure 130 may be increased as the second

channel structures 110D become closer to the contact region CTR.

[0032] However, the present disclosure is not limited to the examples.

The first channel structures 110R and the second channel structures 110D may each be a real channel structure. A distance between the

5 first channel structures 110R and the slit structure 130 may be substantially the same. A distance between the second channel

structures 110D and the slit structure 130 may be increased as the second channel structures 110D become closer to the contact region

CTR. Alternatively, the distance between the first channel structures

10 110R and the slit structure 130 may be increased as the first channel structures 110R becomes closer to the contact region CTR. The

distance between the second channel structures 110D and the slit structure 130 may be increased as the second channel structures

110D become closer to the contact region CTR.

15 **[0033]** According to an aforementioned structure, the second distance "d2" between the second channel structures 110D and the slit

structure 130 in the second direction II may be increased as the second channel structures 110D become closer to the contact region

CTR. As the second distance "d2" is increased, the fourth interval

20 "r4" between the second channel structures 110D in the second direction II may be reduced. In order to compensate for the

reduction in the distance, the third interval "r3" between the second channel structures 110D in the first direction I may be increased.

Accordingly, in an embodiment, although the second distance "d2" is

increased, the pattern density of the second channel structures 110D can be maintained. Furthermore, in an embodiment, a change in the form of the slit structure 130 at the boundary surface between the cell region CR and the contact region CTR can be prevented or reduced.

5 **[0034]** FIGS. 2A and 2B are diagrams for describing a semiconductor device according to an embodiment of the present disclosure. FIG. 2A may be a plan view of a cell region CR and a contact region CTR. FIG. 2B may be a cross-sectional view of a first channel structure 210R1, a second channel structure 210D1, a third channel structure
10 210R2, and a fourth channel structure 210D2. Hereinafter, a description of contents that are redundant with aforementioned contents will be omitted.

[0035] Referring to FIGS. 2A and 2B, the semiconductor device may include a first gate structure 200A, a second gate structure 200B, the
15 first channel structures 210R1, the second channel structures 210D1, the third channel structures 210R2, the fourth channel structures 210D2, supports 220, or slit structures 230 or may include the first gate structure 200A, the second gate structure 200B, the first channel structures 210R1, the second channel structures 210D1, the third
20 channel structures 210R2, the fourth channel structures 210D2, the supports 220, or the slit structures 230 in combination.

[0036] The first gate structure 200A and the second gate structure 200B may each include the cell region CR and the contact region CTR. The cell region CR may include a first region CR1 and a second region

CR2. The second region CR2 may be disposed closer to the contact region CTR than the first region CR1. The second gate structure 200B may be disposed on the first gate structure 200A. The first gate structure 200A may include first insulating layers 201 and first
5 conductive layers 202 that are alternately stacked. The second gate structure 200B may include second insulating layers 203 and second conductive layers 204 that are alternately stacked.

[0037] The slit structures 230 may be disposed within the first gate structure 200A and the second gate structure 200B, and may extend
10 in a first direction I. For example, the slit structures 230 may extend from the cell region CR to the contact region CTR.

[0038] The first channel structures 210R1 and the second channel structures 210D1 may be disposed within the first gate structure 200A. For example, the first channel structures 210R1 or the second
15 channel structures 210D1 may be disposed in the cell region CR. The first channel structures 210R1 may be disposed in the first region CR1. The second channel structures 210D1 may be disposed in the second region CR2.

[0039] The first channel structures 210R1 may each include a first
20 channel layer 210R1A, a first memory layer 210R1B, or a first insulating core 210R1C or may each include the first channel layer 210R1A, the first memory layer 210R1B or the first insulating core 210R1C in combination. The second channel structures 210D1 may each include a second channel layer 210D1A, a second memory layer

210D1B, or a second insulating core 210D1C or may each include the second channel layer 210D1A, the second memory layer 210D1B, or the second insulating core 210D1C in combination.

[0040] The third channel structures 210R2 and the fourth channel structures 210D2 may be disposed within the second gate structure 200B. For example, the third channel structures 210R2 or the fourth channel structures 210D2 may be disposed in the cell region CR. The third channel structures 210R2 may be connected to the first channel structures 210R1. The fourth channel structures 210D2 may be connected to the second channel structures 210D1. The third channel structures 210R2 may each include the third channel layer 210R2A, the third memory layer 210R2B, or the third insulating core 210R2C or may each include the third channel layer 210R2A, the third memory layer 210R2B, or the third insulating core 210R2C in combination. The fourth channel structures 210D2 may each include the fourth channel layer 210D2A, the fourth memory layer 210D2B, or the fourth insulating core 210D2C or may each include the fourth channel layer 210D2A, the fourth memory layer 210D2B, or the fourth insulating core 210D2C in combination.

[0041] The first channel structure 210R1 and the third channel structure 210R2 may be interconnected and may form one channel structure. For example, a portion that belongs to a channel structure and that is disposed within the first gate structure 200A may be the first channel structure 210R1. A portion that belongs to the channel

structure and that is disposed within the second gate structure 200B may be the third channel structure 210R2. Memory cells that are stacked along the first channel structure 210R1 and memory cells that are stacked along the third channel structure 210R2 may constitute one memory string.

[0042] The second channel structure 210D1 and the fourth channel structure 210D2 may be interconnected, and may form one channel structure. For example, a portion that belongs to a channel structure and that is disposed within the first gate structure 200A may be the second channel structure 210D1. A portion that belongs to the channel structure and that is disposed within the second gate structure 200B may be the fourth channel structure 210D2. Memory cells that are stacked along the second channel structure 210D1 and memory cells that are stacked along the fourth channel structure 210D2 may constitute one memory string.

[0043] The distance between the first channel structures 210R1 and the slit structure 230 may be substantially the same as the distance between the third channel structures 210R2 and the slit structure 230. For example, in the second direction II, the first channel structures 210R1 may be spaced apart from the slit structure 230 by a first distance "d1", and the third channel structures 210R2 may be spaced apart from the slit structure 230 by a third distance "d3". Accordingly, the third channel structures 210R2 and the first channel structures 210R1 may be aligned and disposed, but the present disclosure is not

limited thereto. The distance between the first channel structures 210R1 and the slit structure 230 may be greater than the distance between the third channel structures 210R2 and the slit structure 230. In such a case, the third channel structures 210R2 and the first channel structures 210R1 may be offset and disposed.

[0044] The distance between the second channel structures 210D1 and the slit structure 230 may be substantially the same as the distance between the fourth channel structures 210D2 and the slit structure 230. For example, in the second direction II, the second channel structures 210D1 may be spaced apart from the slit structure 230 by a second distance "d2", and the fourth channel structures 210D2 may be spaced apart from the slit structure 230 by a fourth distance "d4". Accordingly, the second channel structures 210D1 and the fourth channel structures 210D2 may be aligned and disposed, but the present disclosure is not limited thereto. The distance between the second channel structures 210D1 and the slit structure 230 may be greater than the distance between the fourth channel structures 210D2 and the slit structure 230. For example, in the second direction II, the fourth distance "d4" is smaller than the second distance "d2". Therefore, the second channel structures 210D1 and the fourth channel structures 210D2 may be offset and disposed.

[0045] A distance between the first channel structures 210R1 and the slit structure 230 may be increased as the first channel structures 210R1 become closer to the contact region CTR. Furthermore, a

distance between the second channel structures 210D1 and the slit structure 230 may be increased as the second channel structures 210D1 become closer to the contact region CTR. A distance between the third channel structures 210R2 and the slit structure 230 may be increased as the third channel structures 210R2 become closer to the contact region CTR. A distance between the fourth channel structures 210D2 and the slit structure 230 may be increased as the fourth channel structures 210D2 become closer to the contact region CTR. For example, the third distance "d3" may be substantially the same as or different from the fourth distance "d4". The fourth distance "d4" may be greater than the third distance "d3."

[0046] According to an aforementioned structure, the arrangement of the first channel structures 210R1 and the second channel structures 210D1 that are disposed within the first gate structure 200A and the arrangement of the third channel structures 210R2 and the fourth channel structures 210D2 that are disposed within the second gate structure 200B may be substantially the same. For example, the first channel structures 210R1 may be spaced apart from each other at a first interval "r1" in the first direction I, and also the third channel structures 210R2 may be spaced apart from each other at the first interval "r1" in the first direction I. The first channel structures 210R1 may be spaced apart from each other at a second interval "r2" in the second direction II, and also the third channel structures 210R2 may be spaced apart from each other at the second interval "r2" in the

second direction II. And, the second channel structures 210D1 may be spaced apart from each other at a third interval "r3" in the first direction I, and also the fourth channel structures 210D2 may be spaced apart from each other at the third interval "r3" in the first direction I. The second channel structures 210D1 may be spaced apart from each other at a fourth interval "r4" in the second direction II, and also the fourth channel structures 210D2 may be spaced apart from each other at the fourth interval "r4" in the second direction II. Furthermore, pattern density of the third channel structures 210R2 and the pattern density of the fourth channel structures 210D2 may be maintained to be substantially identical to each other.

[0047] The distance between the first channel structures 210R1 and the slit structure 230 and the distance between the second channel structures 210D1 and the slit structure 230 may be increased as the first channel structures 210R1 and the second channel structures 210D1 become closer to the contact region CTR. Similarly, in the second gate structure 200B, the distance between the third channel structures 210R2 and the slit structure 230 and the distance between the fourth channel structures 210D2 and the slit structure 230 may be increased as the third channel structures 210R2 and the fourth channel structures 210D2 become closer to the contact region CTR. Accordingly, in an embodiment, a change in the form of the slit structure 230 at a boundary surface between the cell region CR and the contact region CTR can be prevented or reduced.

[0048] FIGS. 3A to 3D are diagrams for describing a semiconductor device according to an embodiment of the present disclosure.

[0049] FIG. 3A may be a plan view of the semiconductor device. FIG. 3B may be an enlarged view of B in FIG. 3A. FIGS. 3C and 3D may be cross-sectional views of the first channel structure 210R1, the second channel structure 210D1, the third channel structure 210R2, and the fourth channel structure 210D2. Hereinafter, a description of contents that are redundant with aforementioned contents will be omitted.

[0050] Referring to FIGS. 3A to 3D, the semiconductor device may include the first gate structure 200A, the second gate structure 200B, the first channel structures 210R1, the second channel structures 210D1, the third channel structures 210R2, the fourth channel structures 210D2, the supports 220, or the slit structures 230 or may include the first gate structure 200A, the second gate structure 200B, the first channel structures 210R1, the second channel structures 210D1, the third channel structures 210R2, the fourth channel structures 210D2, the supports 220, or the slit structures 230 in combination.

[0051] The third channel structures 210R2 and the fourth channel structures 210D2 may be disposed in the cell region CR of the second gate structure 200B. The distance between the third channel structures 210R2 and the slit structure 230 and the distance between the fourth channel structures 210D2 and the slit structure 230 may be

constant. For example, the distance between the channel structures 210R2 and 210D2 and the slit structure 230 may be constant regardless of the cell region CR or the contact region CTR.

[0052] For reference, locations, arrangements, and forms of the first gate structure 200A that is disposed under the second gate structure 200B and the first channel structures 210R1 and the second channel structures 210D1 that are disposed in the cell region CR of the first gate structure 200A may be similar to those that have been described with reference to FIGS. 2A and 2B. The distance between the first channel structures 210R1 and the slit structure 230 and the distance between the second channel structures 210D1 and the slit structure 230 may be increased as the first channel structures 210R1 and the second channel structures 210D1 become closer to the contact region CTR. Accordingly, the channel structures 210R2 and 210D2 of the second gate structure 200B and the channel structures 210R1 and 210D1 of the first gate structure 200A may be offset and disposed.

[0053] Referring to FIG. 3C, the first channel structures 210R1 and the third channel structures 210R2 may be offset and disposed, and may be interconnected through overlapped portions of the first channel structures 210R1 and the third channel structures 210R2. The second channel structures 210D1 and the fourth channel structures 210D2 may be offset and disposed, and may be interconnected through overlapped portions of the second channel structures 210D1 and the fourth channel structures 210D2.

[0054] Referring to FIG. 3D, a sacrificial layer 210S may be disposed within the first gate structure 200A. The third channel structures 210R2 and the fourth channel structures 210D2 may be disposed within the second gate structure 200B. That is, the sacrificial layers 210S may be disposed within the first gate structure 200A instead of the first channel structures 210R1 and the second channel structures 210D1. The sacrificial layers 210S may be offset and disposed so that the sacrificial layers 210S do not overlap the third channel structure 210R2 and the fourth channel structure 210D2. The sacrificial layers 210S may remain without being replaced with the first channel structure 210R1 or the second channel structure 210D1 in a process of manufacturing the semiconductor device.

[0055] According to an aforementioned structure, the arrangement of the first channel structures 210R1 and the second channel structures 210D1 that are disposed within the first gate structure 200A and the arrangement of the third channel structures 210R2 and the fourth channel structures 210D2 that are disposed within the second gate structure 200B may be different from each other. The distance between the channel structures 210R1 and 210D1 and the slit structure 230 within the first gate structure 200A may be increased as the channel structures 210R1 and 210D1 become closer to the contact region CTR. The distance between the channel structures 210R2 and 210D2 and the slit structure 230 within the second gate structure 200B may be constant.

[0056] FIG. 4 is a diagram for describing a semiconductor device according to an embodiment of the present disclosure. Hereinafter, a description of contents that are redundant with aforementioned contents will be omitted.

5 **[0057]** Referring to FIG. 4, the semiconductor device may include a gate structure 300, first channel structures 310R, second channel structures 310D, or a slit structure 330 or may include the gate structure 300, the first channel structures 310R, the second channel structures 310D, or the slit structure 330 in combination. The
10 semiconductor device may further include supports 320 or bit lines 340 or may further include the supports 320 or the bit lines 340 in combination.

[0058] The gate structure 300, the channel structures 310R and 310D, and the slit structure 330 may be the gate structure 100, the channel
15 structures 110R and 110D, and the slit structure 130, respectively, which have been described with reference to FIGS. 1A to 1C. The channel structures 310R and 310D may be disposed in a cell region CR of the gate structure 300. For example, the first channel structures 310R may be disposed in a first region CR1 of the cell
20 region CR. The second channel structures 310D may be disposed in a second region CR2 of the cell region CR.

[0059] The channel structures 310R and 310D may each be a real channel structure or a dummy channel structure. For example, the first channel structures 310R may each be a real channel structure,

and the second channel structures 310D may each be a dummy channel structure. In this case, a distance between the first channel structures 310R and the slit structure 330 may be increased as the first channel structures 310R become closer to the contact region CTR. A distance between the second channel structures 310D and the slit structure 330 may be increased as the second channel structures 310D become closer to the contact region CTR.

[0060] The bit lines 340 may be disposed in the cell region CR of the gate structure 300. Furthermore, the bit lines 340 may be disposed on a real channel structure, and may be connected to the real channel structures. For example, the bit lines 340 may be connected to the first channel structures 310R. The bit lines 340 may extend in a second direction II that intersects a first direction I, and may be connected to the first channel structures 310R. The bit lines 340 may be disposed in the first direction I in a way to be spaced apart from each other.

[0061] An interval between the bit lines 340 may be increased as the bit lines 340 become closer to a contact region CTR. The bit lines 340 may include first bit lines 340A or second bit lines 340B. The second bit lines 340B may be disposed closer to the contact region CTR than the first bit lines 340A. The first bit lines 340A may be spaced apart from each other at a first interval P1 in the first direction I. The second bit lines 340B may be spaced apart from each other at a second interval P2 in the first direction I. The first interval P1 and

the second interval P2 may be substantially the same or different from each other. For example, the second interval P2 may be greater than the first interval P1.

[0062] For reference, both the first channel structures 310R and the second channel structures 310D may each be a real channel structure. In this case, an interval between the bit lines 340 that are connected to the channel structures 310R and 310D may be increased as the bit lines 340 become closer to the contact region CTR.

[0063] According to an aforementioned structure, the intervals P1 and P2 between the bit lines 340 that are connected to the channel structures 310R and 310D may also be changed depending on distances between the channel structures 310R and 310D and the slit structure 330. The intervals P1 and P2 may be increased as the bit lines 340 become closer to the contact region CTR.

[0064] FIGS. 5A to 5D are diagrams for describing a method of manufacturing a semiconductor device according to an embodiment of the present disclosure. Hereinafter, a description of contents that are redundant with aforementioned contents will be omitted.

[0065] Referring to FIG. 5A, a stack 400 may be formed. The stack 400 may include first material layers and second material layers that are alternately stacked. In this case, the first material layers may include an insulating material, such as oxide. The second material layers may include a sacrificial material, such as nitride. Alternatively, the first material layers may include an insulating

material, such as oxide. The second material layers may include a conductive material, such as tungsten. The stack 400 may include a cell region CR and a contact region CTR. The cell region CR may include a first region CR1 and a second region CR2. The second
5 region CR2 may be disposed closer to the contact region CTR than the first region CR1.

[0066] Referring to FIGS. 5B and 5C, a mask M may be formed on the stack 400. In this case, the mask M may include a hard mask or a photoresist or may include the hard mask or the photoresist in
10 combination. Next, first openings OP1, second openings OP2, or third openings OP3 may be formed within the stack 400 or the first openings OP1, the second openings OP2, or the third openings OP3 may be formed in combination within the stack 400, by using the mask M as an etch barrier.

[0067] The first openings OP1 and the second openings OP2 may be
15 formed in the cell region CR. The third openings OP3 may be formed in the contact region CTR. The first openings OP1 may be formed in the first region CR1. The second openings OP2 may be formed in the second region CR2. The first openings OP1, the second openings OP2,
20 and the third openings OP3 may be simultaneously formed, but the present disclosure is not limited thereto. After the first openings OP1 and the second openings OP2 are formed, the third openings OP3 may be formed. The words "simultaneous" and "simultaneously" as used herein with respect to processes mean that the processes take place

on overlapping intervals of time. For example, if a first process takes place over a first interval of time and a second process takes place simultaneously over a second interval of time, then the first and second intervals at least partially overlap each other such that there exists a time at which the first and second processes are both taking place.

[0068] An interval between the first openings OP1 or an interval between the second openings OP2 may be different depending on a distance from the contact region CTR. For example, an interval between the first openings OP1 in a first direction I and an interval between the second openings OP2 in the first direction I may be increased as the first openings OP1 and the second openings OP2 become closer to the contact region CTR. Furthermore, an interval between the first openings OP1 in a second direction II that intersects the first direction I and an interval between the second openings OP2 in the second direction II may be reduced as the first openings OP1 and the second openings OP2 become closer to the contact region CTR.

[0069] The first openings OP1 or the second openings OP2 may be formed by considering a region OP4A in which a fourth opening will be formed. The second openings OP2 may be disposed closer to the contact region CTR than the first openings OP1. The openings OP1 and OP2 may be formed so that distances between the openings OP1 and OP2 and the region OP4A in which the fourth opening will be

formed are increased as the openings OP1 and OP2 become closer to the contact region CTR. For example, in the second direction II, the first openings OP1 may be formed to be spaced apart from the region OP4A in which the fourth opening will be formed by a first distance "d1". In the second direction II, the second openings OP2 may be formed to be spaced apart from the region OP4A in which the fourth opening will be formed by a second distance "d2". The first distance "d1" may be substantially the same as or different from the second distance "d2". For example, the second distance "d2" may be greater than the first distance "d1".

[0070] The first openings OP1 may be spaced apart from each other at a first interval "r1" in the first direction I, and may be spaced apart from each other at a second interval "r2" in the second direction II. The second openings OP2 may be spaced apart from each other at a third interval "r3" in the first direction I, and may be spaced apart from each other at a fourth interval "r4" in the second direction II. The first interval "r1" and the third interval "r3" may be substantially the same or different from each other. The second interval "r2" and the fourth interval "r4" may be substantially the same or different from each other.

[0071] The number of opening rows of the first openings OP1 and the number of opening rows of the second openings OP2 may be substantially the same or different from each other. In this case, the opening row may include the openings OP1 or OP2 that are arranged

in the first direction I. If the second distance "d2" is greater than the first distance "d1", an interval between the opening rows of the second openings OP2 may be reduced. Accordingly, the fourth interval "r4" may be smaller than the second interval "r2".

5 [0072] Furthermore, in order to compensate for a difference between the pattern density of the first openings OP1 and the pattern density of the second openings OP2 according to a difference between the second interval "r2" and the fourth interval "r4", the third interval "r3" may be greater than the first interval "r1". Accordingly, a first
10 diagonal line distance S1 between the first openings OP1 and a second diagonal line distance S2 between the second openings OP2 may be substantially the same. Furthermore, the pattern densities of the first openings OP1 and the second openings OP2 may be maintained substantially identically.

15 [0073] Referring to FIG. 5D, first channel structures 410R may be formed within the first openings OP1, respectively. Accordingly, the first channel structures 410R that extend through the stack 400 may be formed. Second channel structures 410D may be formed within the second openings OP2, respectively. Accordingly, the second
20 channel structures 410D that extend through the stack 400 may be formed. The second channel structures 410D may be formed simultaneously with the first channel structures 410R, but the present disclosure is not limited thereto. After the first channel structures 410R are formed, the second channel structures 410D may be

formed.

[0074] The channel structures 410R and 410D may be similar to the channel structures 110R and 110D, respectively, which have been described with reference to FIGS. 1A to 1C. The channel structures
5 410R and 410D may each include a channel layer, a memory layer, or an insulating core or may each include the channel layer, the memory layer, or the insulating core in combination.

[0075] The channel structures 410R and 410D may each be a real channel structure or a dummy channel structure. The real channel
10 structure and the dummy channel structure may have similar structures. Electrical connection states of the real channel structure and the dummy channel structure may be different from each other. For example, the first channel structures 410R may each be a real channel structure. The second channel structures 410D may each be
15 a dummy channel structure. As another example, the first channel structures 410R and the second channel structures 410D may each be a dummy channel structure.

[0076] Supports 420 may be formed within the third openings OP3, respectively. The supports 420 may be formed in the contact region
20 CTR. The supports 420 may be simultaneously formed when the channel structures 410R and 410D are formed, but the present disclosure is not limited thereto. After the channel structures 410R and 410D are formed, the supports 420 may be formed.

[0077] Next, a fourth opening OP4 that extends in the first direction I

may be formed within the stack 400. In this case, the fourth opening OP4 may be a slit. The fourth opening OP4 may be formed between the first channel structures 410R, between the second channel structures 410D, or between the supports 420, the first channel structures 410R, the second channel structures 410D, or the supports 420 being spaced apart from each other in the second direction II.

[0078] A form of the fourth opening OP4 may be influenced by a surrounding environment. If the pattern density of the cell region CR and the pattern density of the contact region CTR are different from each other, a form of the fourth opening OP4 may be deformed at a boundary between the cell region CR and the contact region CTR at which the pattern density is changed. For example, the fourth opening OP4 may have an inclined form, or some region of the fourth opening OP4 may protrude. In an embodiment, the fourth opening OP4 can be prevented from being inclined or deformed or the inclination or deformation of the fourth opening OP4 can be reduced because the openings OP1 and OP2 are formed by adjusting the distance between the fourth opening OP4 and the openings OP1 and OP2 so that the deformation of the fourth opening OP4 is minimized.

[0079] Next, a slit structure 430 may be formed within the fourth opening OP4. The relation between the intervals r_1 , r_2 , and S_1 among the first openings OP1, the relation between the intervals r_3 , r_4 , and S_2 among the second openings OP2, and the relation between the distances d_1 and d_2 between the openings OP1 and OP2 and the

fourth opening OP4 may also be identically applied to a relation between the channel structures 410R and 410D and a relation between the channel structures 410R and 410D and the slit structure 430.

5 **[0080]** For reference, the gate structure may be formed within the stack 400 by replacing sacrificial materials with conductive layers. Furthermore, when the stack 400 is formed, if insulating layers and conductive layers are alternately stacked, a process of replacing the sacrificial materials may be omitted. Alternatively, a process for
10 reducing resistance of the conductive layers, such as a silicidation process, may also be performed. In this case, the stack 400 may be a gate structure.

[0081] Furthermore, bit lines that are connected to real channel structures may be formed. For example, if the first channel
15 structures 410R are real channel structures and the second channel structures 410D are dummy channel structures, bit lines that are connected to the first channel structures 410R may be formed. In this case, if a distance between the first channel structures 410R and the slit structure 430 is increased as the first channel structures 410R
20 become closer to the contact region CTR, an interval between the bit lines may be increased.

[0082] According to an aforementioned process, locations of the openings OP1 and OP2 may be determined by considering a location at which the fourth opening OP4 will be formed. For example, the

openings OP1 and OP2 may be formed so that the openings OP1 and OP2 become distant from locations at which the fourth opening OP4 will be formed as the openings OP1 and OP2 become closer to the contact region CTR. Accordingly, in an embodiment, a change in the form of the fourth opening OP4 can be prevented or minimized.

[0083] FIGS. 6A to 6C are diagrams for describing a method of manufacturing a semiconductor device according to an embodiment of the present disclosure. Hereinafter, a description of contents that are redundant with aforementioned contents will be omitted.

[0084] Referring to FIG. 6A, dummy plugs 550 may be formed within a first stack 500A. First, fifth openings OP5 may be formed within the first stack 500A. In this case, the fifth openings OP5 may each be a dummy opening. The fifth openings OP5 may be formed when first openings OP1 and second openings OP2 are formed. The fifth openings OP5 may be formed in a location at which a fourth opening OP4 will be formed. In other words, a dummy opening may be formed at a location at which a slit will be formed.

[0085] The first openings OP1 and the second openings OP2 may be the same as the first openings OP1 and the second openings OP2 that have been described with reference to FIGS. 5B to 5D. The first openings OP1 and the second openings OP2 may be formed by considering the location at which the fourth opening OP4 will be formed. For example, the openings OP1 and OP2 may be formed so that the openings OP1 and OP2 become distant from the location at

which the fourth opening OP4 will be formed as the openings OP1 and OP2 become closer to the contact region CTR.

[0086] Next, the dummy plugs 550 may be formed within the fifth openings OP5, respectively. The dummy plugs 550 may be formed when sacrificial layers 510RS and 510DS are formed within the openings OP1 and OP2, respectively. The sacrificial layers 510RS and 510DS may include a material that has high etch selectivity to the stack. For example, the sacrificial layers 510RS and 510DS may include a conductive material, such as tungsten. The dummy plugs 550 may be formed of the same material as the sacrificial layers 510RS and 510DS. For example, the dummy plugs 550 may include a conductive material, such as tungsten.

[0087] Referring to FIGS. 6B and 6C, a second stack 500B may be formed on the first stack 500A. Next, sixth openings OP6 that are connected to the first openings OP1 may be formed within the second stack 500B. Seventh openings OP7 that are connected to the second openings OP2 may be formed within the second stack 500B. For example, the openings OP6 and OP7 that expose the channel structures 510R1 and 510D1, respectively, may be formed. The openings OP6 and OP7 may be formed by considering the location at which the fourth opening OP4 will be formed. For example, the openings OP6 and OP7 may be formed so that the openings OP6 and OP7 become distant from the location at which the fourth opening OP4 will be formed as the openings OP6 and OP7 become closer to the

contact region CTR. For reference, although not illustrated in these drawings, the second stack 500B may be formed so that a distance between the fourth opening OP4 and the openings OP6 and OP7 is constant.

5 [0088] Next, the first openings OP1 may be re-opened by removing the sacrificial layers 510RS within the first openings OP1 through the sixth openings OP6. The second openings OP2 may be re-opened by removing the sacrificial layers 510DS within the second openings OP2 through the seventh openings OP7. Next, channel structures 510R1,
10 510R2, 510D1, and 510D2 may be formed within the openings OP1, OP6, OP2, and OP7, respectively. For example, the first channel structures 510R1 and the third channel structures 510R2 may be formed within the sixth openings OP6 and the first openings OP1, respectively. The second channel structures 510D1 and the fourth
15 channel structures 510D2 may be formed within the seventh openings OP7 and the second openings OP2. In this case, referring back to FIG. 2B, the first channel structures 510R1 and the third channel structures 510R2 may be aligned and connected, and the second channel structures 510D1 and the fourth channel structures 510D2
20 may be aligned and connected.

[0089] For reference, the channel structures 510R1, 510R2, 510D1, and 510D2 may be offset and disposed. For example, referring back to FIG. 3C, the first channel structures 510R1 and the third channel structures 510R2 may be offset and connected. Referring back to

FIG. 3D, that is, the sacrificial layers 510RS and 510DS may be disposed within the first stack 500A instead of the first channel structures 510R1 and the second channel structures 510D1. The sacrificial layers 510RS and 510DS may be offset and disposed so that the sacrificial layers 510RS and 510DS do not overlap the third channel structure 510R2 and the fourth channel structure 510D2. The sacrificial layers 510RS and 510DS may remain without being replaced with the first channel structure 510R1 or the second channel structure 510D1 in a process of manufacturing the semiconductor device.

[0090] Next, the fourth opening OP4 may be formed. When the fourth opening OP4 is formed, charges may be discharged through the dummy plug 550. For example, charges that have been accumulated within the channel structures 510R1, 510R2, 510D1, and 510D2 may be discharged through the dummy plug 550. The dummy plug 550 may be removed in a process of forming the fourth opening OP4. Next, a slit structure 530 may be formed within the fourth opening OP4.

[0091] According to an aforementioned process, the dummy plug 550 may be formed within the first stack 500A before the second stack 500B is formed. Accordingly, in a process of forming the fourth opening OP4, charges that have been accumulated within the channel structures 510R1, 510R2, 510D1, and 510D2 can be discharged through the dummy plug 550. In an embodiment, the deformation of

the fourth opening OP4 attributable to the charges can be prevented or minimized.

[0092] Although embodiments according to the technical spirit of the present disclosure have been described above with reference to the accompanying drawings, the embodiments have been provided to
5 merely describe embodiments according to the concept of the present disclosure, and the present disclosure is not limited to the embodiments. A person having ordinary knowledge in the art to which the present disclosure pertains may substitute, modify, and
10 change the embodiments in various ways without departing from the technical spirit of the present disclosure written in the claims. Such substitutions, modifications, and changes may be said to belong to the scope of the present disclosure.

WHAT IS CLAIMED IS:

1. A semiconductor device comprising:

a gate structure comprising a cell region and a contact region;

5 a slit structure extending in a first direction through the gate structure;

first channel structures disposed in the cell region of the gate structure; and

second channel structures disposed in the cell region of the gate structure and disposed to be more adjacent to the contact region of the gate structure than the first channel structures,

wherein in a second direction that intersects the first direction, the first channel structures are spaced apart from the slit structure by a first distance, and the second channel structures are spaced apart from the slit structure at a second distance, the second distance is greater than the first distance.

2. The semiconductor device of claim 1, wherein:

the first channel structures are spaced apart from each other at a first interval in the first direction and are spaced apart from each other at a second interval in the second direction,

the second channel structures are spaced apart from each other at a third interval in the first direction and are spaced apart from each other at a fourth interval in the second direction,

the third interval is greater than the first interval, and the fourth interval is less than the second interval.

3. The semiconductor device of claim 1, wherein a pattern
5 density of the first channel structures and a pattern density of the second channel structures are substantially the same as each other.

4. The semiconductor device of claim 1, wherein a first
diagonal line distance between the first channel structures and a
10 second diagonal line distance between the second channel structures are substantially the same as each other.

5. The semiconductor device of claim 1, wherein the first
channel structures and the second channel structures each comprise a
15 dummy channel structure.

6. The semiconductor device of claim 1, wherein:
the first channel structures each comprise a real channel
structure, and
20 the second channel structures each comprise a dummy channel
structure.

7. The semiconductor device of claim 6, wherein:
a distance between the first channel structures and the slit

structure is substantially the same, and

a distance between the second channel structures and the slit structure is increased as the second channel structures become closer to the contact region.

5

8. The semiconductor device of claim 6, wherein a distance between the first channel structures and the slit structure is increased as the first channel structures become closer to the contact region.

10

9. The semiconductor device of claim 1, further comprising bit lines connected to the first channel structures and extending in the second direction,

wherein an interval between the bit lines is increased as the bit lines become closer to the contact region.

15

10. A semiconductor device comprising:

a first gate structure comprising a cell region and a contact region;

first channel structures and second channel structures disposed in the cell region of the first gate structure;

20

a second gate structure disposed on the first gate structure;

third channel structures disposed within the second gate structure and connected to the first channel structures;

fourth channel structures disposed within the second gate

structure and connected to the second channel structures; and

a slit structure disposed within the first gate structure and the second gate structure and extending in a first direction,

wherein in a second direction that intersects the first direction,
5 the first channel structures are spaced apart from the slit structure by a first distance, and the second channel structures are spaced apart from the slit structure by a second distance that is greater than the first distance.

10 11. The semiconductor device of claim 10, wherein in the second direction, the third channel structures are spaced apart from the slit structure by a third distance, and the fourth channel structures are spaced apart from the slit structure by a fourth distance that is greater than the third distance.

15 12. The semiconductor device of claim 10, wherein:
in the second direction, the fourth channel structures are spaced apart from the slit structure by a fourth distance, and
the fourth distance is smaller than the second distance.

20 13. The semiconductor device of claim 10, wherein:
the third channel structures are spaced apart from each other at a first interval in the first direction and are spaced apart from each other at a second interval in the second direction,

the fourth channel structures are spaced apart from each other at a third interval in the first direction and are spaced apart from each other at a fourth interval in the second direction,

the third interval is greater than the first interval, and

5 the fourth interval is less than the second interval.

14. The semiconductor device of claim 10, wherein a pattern density of the third channel structures and a pattern density of the fourth channel structures are substantially the same as each other.

10

15. The semiconductor device of claim 10, wherein:

the fourth channel structures are disposed to be more adjacent to the contact region than the third channel structures,

15 a distance between the third channel structures and the slit structure is substantially identical, and

a distance between the fourth channel structures and the slit structure is increased as the fourth channel structures become closer to the contact region.

20 16. The semiconductor device of claim 15, wherein the distance between the third channel structures and the slit structure is increased as the third channel structures become closer to the contact region.

17. A method of manufacturing a semiconductor device,
comprising:

forming a stack comprising a cell region and a contact region;

forming first channel structures that extend through the cell
5 region of the stack;

forming second channel structures that extend through the cell
region of the stack; and

forming, within the stack, a slit structure that extends in a first
direction,

10 wherein in a second direction that intersects the first direction,
the first channel structures are spaced apart from the slit structure by
a first distance, and the second channel structures are spaced apart
from the slit structure by a second distance, the second distance is
greater than the first distance.

15

18. The method of claim 17, wherein:

the first channel structures are spaced apart from each other at
a first interval in the first direction and are spaced apart from each
other at a second interval in the second direction,

20 the second channel structures are spaced apart from each other
at a third interval in the first direction and are spaced apart from each
other at a fourth interval in the second direction,

the third interval is greater than the first interval, and

the fourth interval is less than the second interval.

19. The method of claim 17, wherein a pattern density of the first channel structures and a pattern density of the second channel structures are substantially with the same as each other.

5

20. The method of claim 17, wherein a first diagonal line distance between the first channel structures and a second diagonal line distance between the second channel structures are substantially the same as each other.

10

21. The method of claim 17, wherein when the first channel structures are formed, the second channel structures are formed.

22. The method of claim 17, wherein the first channel structures and the second channel structures each comprise a dummy channel structure.

15

23. The method of claim 17, wherein:

the first channel structures each comprise a real channel structure, and

20

the second channel structures each comprise a dummy channel structure.

24. The method of claim 23, wherein:

the second channel structures are disposed to be more adjacent to the contact region than the first channel structures,

a distance between the first channel structures and the slit structure is substantially the same, and

5 a distance between the second channel structures and the slit structure is increased as the second channel structures become closer to the contact region.

25. The method of claim 24, wherein:

10 the distance between the first channel structures and the slit structure is increased as the first channel structures become closer to the contact region,

the method further comprises forming bit lines that are connected to the first channel structures and that extend in the
15 second direction, and

an interval between the bit lines is increased as the bit lines become closer to the contact region.

26. A method of manufacturing a semiconductor device,
20 comprising:

forming a first stack;

forming first openings and second openings within the first stack;

forming a second stack on the first stack;

forming, within the second stack, third openings connected to the first openings;

forming, within the second stack, fourth openings connected to the second openings;

5 forming, within the first stack and the second stack, a slit that extends in a first direction,

wherein in a second direction that intersects the first direction, the first openings are spaced apart from the slit by a first distance, and the second openings are spaced apart from the slit by a second
10 distance, the second distance is greater than the first distance.

27. The method of claim 26, further comprising:

forming first channel structures within the first openings and the third openings; and

15 forming second channel structures within the second openings and the fourth openings.

28. The method of claim 26, wherein in the second direction, the third openings are spaced apart from the slit by a third distance, and the fourth openings are spaced apart from the slit by a fourth
20 distance that is greater than the third distance.

29. The method of claim 26, wherein:

in the second direction, the fourth openings are spaced apart

from the slit at a fourth distance, and

the fourth distance is smaller than the second distance.

30. The method of claim 26, further comprising:

5 forming a dummy opening within the first stack; and

forming a dummy plug within the dummy opening.

31. The method of claim 30, wherein when the first openings
and the second openings are formed, the dummy opening is formed.

10

32. The method of claim 30, wherein the dummy opening is
formed in a location at which the slit is to be formed.

33. The method of claim 30, wherein when the slit is formed,

15 charges are discharged through the dummy plug.