voltage and current probe 111 is provided via the communication device 189 and a cable 193 to the host system 130. Examples of a communication device include an Ethernet device that converts data into Ethernet packets and converts Ethernet packets into data, an Ethernet for Control Automation Technology (EtherCAT) device, a serial interface device that transfers data in series, a parallel interface device that transfers data in parallel, a Universal Serial Bus (USB) interface device, etc.

[0062] Examples of the host system 130 include a computer, e.g., a desktop, a laptop, a tablet, etc. As an illustration, the host system 130 includes a processor and the storage HU 162. As used herein, a processor may be a central processing unit (CPU), a microprocessor, an application specific integrated circuit (ASIC), a programmable logic device (PLD), etc. Examples of the storage HU include a read-only memory (ROM), a random access memory (RAM), or a combination thereof. The storage HU may be a flash memory, a redundant array of storage disks (RAID), a hard disk, etc.

[0063] The impedance matching model 104 is stored within the storage HU 162. The impedance matching model 104 has similar characteristics, e.g., capacitances, inductances, complex power, complex voltage and currents, etc., as that of the impedance matching circuit 114. For example, the impedance matching model 104 has the same number of capacitors and/or inductors as that within the impedance matching circuit 114, and the capacitors and/or inductors are connected with each other in the same manner, e.g., serial, parallel, etc. as that within the impedance matching circuit 114. To provide an illustration, when the impedance matching circuit 114 includes a capacitor coupled in series with an inductor, the impedance matching model 104 also includes the capacitor coupled in series with the inductor.

[0064] As an example, the impedance matching circuit 114 includes one or more electrical components and the impedance matching model 104 includes a design, e.g., a computer-generated model, of the impedance matching circuit 114. The computer-generated model may be generated by a processor based upon input signals received from a user via an input hardware unit. The input signals include signals regarding which electrical components, e.g., capacitors, inductors, etc., to include in a model and a manner, e.g., series, parallel, etc., of coupling the electrical components with each other. As another example, the impedance matching circuit 114 includes hardware electrical components and hardware connections between the electrical components and the impedance matching model 104 include software representations of the hardware electrical components and of the hardware connections. As

memory, etc., of the host system 130. The complex V, I, and ϕ includes a voltage magnitude V, a current magnitude I, and a phase ϕ between the voltage and current.

[0069] The output of the impedance matching model 104 is coupled to an input of the RF transmission model 161, which is stored in the storage hardware unit 162. The impedance matching model 104 also has an input, e.g., a node N3m, which is used to receive the complex voltage and current measured at the node N3.

[0070] The RF transmission model 161 includes the portion 173, another portion 197, and an output N2m, which is coupled via the ESC model 125 to the model node N6m. The ESC model 125 is a model of the ESC 177. For example, the ESC model 125 has similar characteristics as that of the ESC 177. For example, the ESC model 125 has the same inductance, capacitance, resistance, or a combination thereof as that of the ESC 177.

[0071] An input of the portion 173 is the input of the RF transmission model 161. An output of the portion 173 is coupled to an input of the portion 197. The portion ~~172~~ 173 has similar characteristics as that of the portion 169 and the portion 197 has similar characteristics as that of the portion 195.

[0072] Based on the complex voltage and current measured at the model node N4m, the processor of the host system 130 calculates a complex voltage and current V, I, and ϕ, e.g., a third complex voltage and current, at the output, e.g., the model node N1m, of the portion 173 of the RF transmission model 161. The complex voltage and current determined at the model node N1m is stored in the storage HU 162 and/or another storage HU, e.g., a compact disc, a flash memory, etc., of the host system 130.

[0073] In several embodiments, instead of or in addition to determining the third complex voltage and current, the processor of the host system 130 computes a complex voltage and current, e.g., an intermediate complex voltage and current V, I, and ϕ, at a point, e.g., a node, etc., within the portion 173 based on the complex voltage and current at the output of the impedance matching model 104 and characteristics of elements between the input of the RF transmission model 161 and the point within the portion 173.

[0074] In various embodiments, instead of or in addition to determining the third complex voltage and current, the processor of the host system 130 computes a complex voltage and current, e.g., an intermediate complex voltage and current V, I, and ϕ, at a point, e.g., a node, etc., within the portion 197 based on the complex voltage and current at the

impedance matching circuit 114 and generates connections between the elements that have the same connections as that between the electrical components.

[0079] The input, e.g., the node N3m, of the impedance matching model ~~163~~ 104 receives the first complex voltage and current. For example, the processor of the host system 130 accesses, e.g., reads, etc., from the storage HU 162 the first complex voltage and current and provides the first complex voltage and current to the input of the impedance matching model 104 to process the first complex voltage and current.

[0080] In an operation 116, the first complex voltage and current is propagated through one or more elements of the impedance matching model 104 (Figure 1) from the input, e.g., the node N3m (Figure 1), of the impedance matching model 104 to the output, e.g., the node N4m (Figure 1), of the impedance matching model 104 to determine the second complex voltage and current, which is at the output of the impedance matching model 104. For example, with reference to Figure 3B, when the 2 MHz RF generator is on, e.g., operational, powered on, coupled to the devices, such as, for example, the impedance matching circuit 104, of the plasma system 126, etc., a complex voltage and current Vx1, Ix1, and ϕx1, e.g., an intermediate complex voltage and current, which includes the voltage magnitude Vx1, the current magnitude Ix1, and the phase ϕx1 between the complex voltage and current, at a node 251, e.g., an intermediate node, is determined based on a capacitance of a capacitor 253, based on a capacitance of a capacitor C5, and based on the first complex voltage and current that is received at an input 255. Moreover, a complex voltage and current Vx2, Ix2, and ϕx2 at a node 257 is determined based on the complex voltage and current Vx1, Ix1, and ϕx1, and based on an inductance of an inductor L3. The complex voltage and current Vx2, Ix2, and ϕx2 includes the voltage magnitude Vx2, the current magnitude Ix2, and the phase ϕx2 between the voltage and current. When the 27 MHz RF generator and the 60 MHz RF generator are off, e.g., nonoperational, powered off, decoupled from the impedance matching circuit 104, etc., a complex voltage and current V2, I2, and ϕ2 is determined to be the second complex voltage and current at an output 259, which is an example of the output, e.g., the model node N4m (Figure 1), of the impedance matching model 104 (Figure 1). The complex voltage and current V2, I2, and ϕ2 is determined based on the complex voltage and current Vx2, Ix2, and ϕx2 and an inductor of an inductor L2. The complex voltage and current V2, I2, and ϕ2 includes the voltage magnitude V2, the current magnitude I2, and the phase ϕ2 between the voltage and current.

[0081] Similarly, when 27 MHz RF generator is on and the 2 MHz and the 60 MHz RF generators are off, a complex voltage and current V27, I27, and ϕ27 at the output 259 is determined based on a complex voltage and current received at a node 261 and characteristics of an inductor LPF2, a capacitor C3, a capacitor C4, and an inductor L2. The complex voltage and current V27, I27, and ϕ27 includes the voltage magnitude V27, the current magnitude I27, and the phase ϕ27 between the voltage and current. The complex voltage and current received at the node 261 is the same as the complex voltage and current measured at the node N5 (Figure 1). When both the 2 MHz and 27 MHz RF generators are on and the 60 MHz RF generator is off, the complex voltages and currents V2, I2, ϕ2, V27, I27, and ϕ27 are an example of the second complex voltage and current. Moreover, similarly, when the 60 MHz RF generator is on and the 2 and 27 MHz RF generators are off, a complex voltage and current V60, I60, and ϕ60 at the output 259 is determined based on a complex voltage and current received at a node 265 and characteristics of an inductor LPF1, a capacitor C1, a capacitor C2, an inductor L4, a capacitor 269, and an inductor L1. The complex voltage and current V60, I60, and ϕ60 includes the voltage magnitude V60, the current magnitude I60, and the phase ϕ60 between the voltage and current. When the 2 MHz, 27 MHz, and the 60 MHz RF generators are on, the complex voltages and currents V2, I2, ϕ2, V27, I27, ϕ27, V60, I60, and ϕ60 are an example of the second complex voltage and current.

[0082] In an operation 117, the RF transmission model 161 (Figure 1) is generated based on the electrical components of the RF transmission line 113 (Figure 1). For example, connections between electrical components of the RF transmission line 113 and characteristics of the electrical components are provided to the processor of the host system 130 by the user via an input device that is coupled with the host system 130. Upon receiving the connections and the characteristics, the processor generates elements that have the same characteristics as that of electrical components of the RF transmission line 113 and generates connections between the elements that are the same as that between the electrical components.

[0083] In an operation 119, the second complex voltage and current is propagated through one or more elements of the RF transmission model portion 173 from the input of the RF transmission model ~~113~~ 161 to the output, e.g., the model node N1m (Figure 1), of the RF transmission model portion 173 to determine the third complex voltage and current at the output of the RF transmission model portion 173. For example, with reference to Figure 5B,

122 includes series connections between electrical components and/or parallel connections between electrical components.

[0087] Figure 3B is a circuit diagram of an embodiment of an impedance matching model 172. The impedance matching model 172 is an example of the impedance matching model 104 (Figure 1). As shown, the impedance matching model 172 includes capacitors having capacitances C1 thru C9, inductors having inductances LPF1, LPF2, and L1 thru L4. It should be noted that the manner in which the inductors and/or capacitors are coupled with each other in Figure 3B is an example. For example, the inductors and/or capacitors shown in Figure 3B can be coupled in a series and/or parallel manner with each other. Also, in some embodiments, the impedance matching model 172 includes a different number of capacitors and/or a different number of inductors than that shown in Figure 3B.

[0088] Figure 4 is a diagram of an embodiment of a system 178 used to illustrate an RF transmission line 181, which is an example of the RF transmission line 113 (Figure 1). The RF transmission line 181 includes a cylinder 148, e.g., a tunnel. Within a hollow of the cylinder 148 lies an insulator ~~189~~ 190 and an RF rod 142. A combination of the cylinder 148 and the RF rod 142 is an example of the portion 169 (Figure 1) of the RF transmission line 113 (Figure 1). The RF transmission line 181 is bolted via bolts B1, B2, B3, and B4 with the impedance matching circuit 114. In one embodiment, the RF transmission line 181 is bolted via any number of bolts with the impedance matching circuit 114. In some embodiments, instead of or in addition to bolts, any other form of attachment, e.g., glue, screws, etc., is used to attach the RF transmission line 181 to the impedance matching circuit 114.

[0089] The RF transmission rod 142 is coupled with the output of the impedance matching circuit 114. Also, an RF strap 144, also known as RF spoon, is coupled with the RF rod 142 and with an RF rod 199, a portion of which is located within a support 146, e.g., a cylinder. The support 146 that includes the RF rod 199 is an example of the portion 195 (Figure 1). In an embodiment, a combination of the cylinder 148, the RF rod 142, the RF strap 144, the support 146 and the RF rod 199 forms the RF transmission line 181, which is an example of the RF transmission line 113 (Figure 1). The support 146 provides support to the plasma chamber. The support 146 is attached to the ESC 177 of the plasma chamber. An RF signal is supplied from the x MHz generator via the cable 150, the impedance matching circuit 114, the RF rod 142, the RF strap 144, and the RF rod 199 to the ESC 177.

coupled via a node 304 to an RF cylinder, which is coupled to the ESC 177 (Figure 1). The RF cylinder is an example of the portion 195 (Figure 1).

[0095] It should be noted that in some embodiments, the inductors and capacitors of the tunnel and strap model 302 have other values. For example, the 20 nH inductors have an inductance ranging between 15 and 20 nH or between 20 and 25 nH. As another example, two or more of the inductors of the tunnel and strap model 302 have difference inductances. As yet another example, the 15 pF capacitor has a capacitance ranging between 8 pF and 25 pF, the 31 pF capacitor has a capacitance ranging between 15 pF and 45 pF, the 15.5 pF capacitor has a capacitance ranging between 9 pF and 20 pF, and the 18.5 pF capacitor has a capacitance ranging between 10 pF and 27 pF.

[0096] In various embodiments, any number of inductors are included in the tunnel and strap model 302 and any number of capacitors are included in the tunnel and strap model 302.

[0097] Figure 6 is a diagram of an embodiment of an electrical circuit 310 used to illustrate a cylinder and ESC model 312, which is a combination of an inductor ~~313~~ 314 and a capacitor 316. The cylinder and ESC model 312 includes a cylinder model and an ESC model, which is an example of the ESC model 125 (Figure 1). The cylinder model is an example of the portion 197 (Figure 1) of the RF transmission model 161 (Figure 1). The cylinder and ESC model 312 has similar characteristics as that of a combination of the portion 195 and the ESC 177 (Figure 1). For example, the cylinder and ESC model 312 has the same resistance as that of a combination of the portion 195 and the ESC 177. As another example, the cylinder and ESC model 312 has the same inductance as that of a combination of the portion 195 and the ESC 177. As yet another example, the cylinder and ESC model 312 has the same capacitance as that of a combination of the portion 195 and the ESC 177. As yet another example, the cylinder and ESC model 312 has the same inductance, resistance, capacitance, or a combination thereof, as that of a combination of the portion 195 and the ESC 177.

[0098] The cylinder and ESC model 312 is coupled via a node 318 to the tunnel and strap model 302. The node 318 is an example of the model node N1m (Figure 1).

[0099] It should be noted that in some embodiments, an inductor having an inductance other than the 44 milliHenry (mH) is used in the cylinder and ESC model 312. For example, an inductor having an inductance ranging from 35 mH to 43.9 mH or from 45.1

mH too 55 mH is used. In various embodiments, a capacitor having a capacitance other than 550 pF is used. For example, instead of the 550 pF capacitor, a capacitor having a capacitance ranging between 250 and 550 pF or between 550 and 600 pF is used.

[00100] The processor of the host system 130 (Figure 1) calculates a combined impedance, e.g., total impedance, etc., of a combination of the model 172, the tunnel and strap model 302, and the cylinder and ESC model 312. The combined impedance and complex voltage and current determined at the model node 318 are used as inputs by the processor of the host system 130 to calculate a complex voltage and impedance at the node N6m. It should be noted that an output of the cylinder and ESC model 312 is the model node N6m.

[00101] Figure 7 is a block diagram of an embodiment of a system 200 that is used to determine a variable. The system 200 includes a plasma chamber 135, which further includes an ESC 201 and has an input 285. The plasma chamber 135 is an example of the plasma chamber 175 (Figure 1) and the ESC 201 is an example of the ESC 177 (Figure 1). The ESC 201 includes a heating element 198. Also, the ESC 201 is surrounded by an edge ring (ER) 194. The ER 194 includes a heating element 196. In an embodiment, the ER 194 facilitates a uniform etch rate and reduced etch rate drift near an edge of the work piece 131 that is supported by the ESC 201.

[00102] A power supply 206 provides power to the heating element 196 via a filter 208 to heat the heating element 196 and a power supply 204 provides power to the heating element 198 via a filter 202 to heat the heating element 198. In an embodiment, a single power supply provides power to both the heating elements 196 and 198. The filter 208 filters out predetermined frequencies of a power signal that is received from the power supply 206 and the filter 202 filters out predetermined frequencies of a power signal that is received from the power supply 204.

[00103] The heating element 198 is heated by the power signal received from the power supply 204 to maintain an electrode of the ESC ~~198~~ 201 at a desirable temperature to further maintain an environment within the plasma chamber 135 at a desirable temperature. Moreover, the heating element 196 is heated by the power signal received from the power supply 206 to maintain the ER 194 at a desirable temperature to further maintain an environment within the plasma chamber 135 at a desirable temperature.

[00104] It should be noted that in an embodiment, the ER 194 and the ESC 201 include any number of heating elements and any type of heating elements. For example, the ESC 201 includes an inductive heating element or a metal plate. In one embodiment, each of the ESC 201 and the ER 194 includes one or more cooling elements, e.g., one or more tubes that allow passage of cold water, etc., to maintain the plasma chamber 135 at a desirable temperature.

[00105] It should further be noted that in one embodiment, the system 200 includes any number of filters. For example, the power supplies 204 and 206 are coupled to the ESC 201 and the ER 194 via a single filter.

[00106] Figure 8A is a diagram of an embodiment of a system 217 used to illustrate a model of the filters 202 and 208 (Figure 7) to improve an accuracy of the variable. The system 217 includes the tunnel and strap model 210 that is coupled via a cylinder model 211 to a model 216, which includes capacitors and/or inductors and connections therebetween of the filters 202 and 208. The model 216 is stored within the storage HU 162 (Figure 1) and/or the other storage HU. The capacitors and/or inductors of the model 216 are coupled with each other in a manner, e.g., a parallel manner, a serial manner, a combination thereof, etc. The model 216 represents capacitances and/or inductances of the filters 202 and 208.

[00107] Moreover, the system 217 includes the cylinder model 211, which is a computer-generated model of the RF rod 199 (Figure 4) and the support 146 (Figure 4). The cylinder model 211 has similar characteristics as that of electrical components of the RF rod 199 and the support 146. The cylinder model 211 includes one or more capacitors, one or more inductors, connections between the inductors, connections between the capacitors, and/or connections between a combination of the capacitors and inductors.

[00108] The processor of the host system 130 (Figure 1) calculates a combined impedance, e.g., total impedance, etc., of the model 216, the tunnel and strap model 210, and the cylinder model 211. The combined impedance provides a complex voltage and impedance at the node N2m. With the inclusion of the model 216 and the tunnel and strap model ~~214~~ 210 in determining the variable at the node N2m, accuracy of the variable is improved. It should be noted that an output of the model 216 is the model node N2m.

[00109] Figure 8B is a diagram of an embodiment of a system 219 used to illustrate a model of the filters 202 and 208 (Figure 7) to improve an accuracy of the variable. The

[00113] When a state is identified as S1, the DSP 226 provides a power value P1 and/or a frequency value F1 to a parameter control 222. Moreover, when the state is identified as S0, the DSP 226 provides a power value P0 and/or a frequency value F0 to a parameter control 224. An example of a parameter control that is used to tune a frequency includes an auto frequency tuner (AFT).

[00114] It should be noted that the parameter control 222, the parameter control 224, and the DSP 226 are portions of a control system 187. For example, the parameter control 222 and the parameter control 224 are logic blocks, e.g., tuning loops, etc., which are portions of a computer program that is executed by the DSP 226. In some embodiments, the computer program is embodied within a non-transitory computer-readable medium, e.g., a storage HU.

[00115] In an embodiment, a controller, e.g., hardware controller, ASIC, PLD, etc., is used instead of a parameter control. For example, a hardware controller is used instead of the parameter control 222 and another hardware controller is used instead of the parameter control 224.

[00116] Upon receiving the power value P1 and/or the frequency value F1, the parameter control 222 provides the power value P1 and/or the frequency value F1 to a driver 228 of a drive and amplifier system (DAS) 232. Examples of a driver includes a power driver, a current driver, a voltage driver, a transistor, etc. The driver 228 generates an RF signal having the power value P1 and/or the frequency value F1 and provides the RF signal to an amplifier 230 of the DAS 232.

[00117] In one embodiment, the driver 228 generates an RF signal having a drive power value that is a function of the power value P1 and/or having a drive frequency value that is a function of the frequency value F1. For example, the drive power value is within a few watts, e.g. 1 thru 5 watts, etc., of the power value P1 and the drive frequency value is within a few Hz, e.g. 1 thru 5 Hz, etc., of the frequency value F1.

[00118] The amplifier 230 amplifies the RF signal having the power value P1 and/or the frequency value F1 and generates an RF signal 215 that corresponds to the RF signal received from the driver 228. For example, the RF signal 215 has a higher amount of power than that of the power value P1. As another example, the RF signal 215 has the same amount of power as that of the power value P1. The RF signal 215 is transferred via a cable ~~217~~ 223 and the impedance matching circuit 114 to the ESC 177 (Figure 1).

[00119] The cable ~~217~~ 223 is an example of the cable 150 or the cable 152 (Figure 1). For example, when the RF generator 220 is an example of the x MHz RF generator (Figure 1), the cable ~~217~~ 223 is an example of the cable 150 and when the RF generator 220 is an example of the y MHz RF generator (Figure 1), the cable ~~217~~ 223 is an example of the cable 152.

[00120] When the power value P1 and/or the frequency value F1 are provided to the DAS 232 by the parameter control 222 and the RF signal 215 is generated, the voltage and current probe 238 measures values of the variable at the output 231 that is coupled to the cable ~~217~~ 223. The voltage and current probe 238 is an example of the voltage and current probe 110 or the voltage and current probe 111 (Figure 1). The voltage and current probe 238 sends the values of the variable via a communication device 233 to the host system 130 for the host system 130 to execute the method 102 (Figure ~~3~~ 2) and methods 340, 351, and 363 (Figures 13, 15, and 17) described herein. The communication device 233 is an example of the communication device 185 or 189 (Figure 1). The communication device 233 applies a protocol, e.g., Ethernet, EtherCAT, USB, serial, parallel, packetization, depacketization, etc., to transfer data from the voltage and current probe 238 to the host system 130. In various embodiments, the host system 130 includes a communication device that applies the protocol applied by the communication device 233. For example, when the communication 233 applies packetization, the communication device of the host system 130 applies depacketization. As another example, when the communication device 233 applies a serial transfer protocol, the communication device of the host system 130 applies a serial transfer protocol.

[00121] Similarly, upon receiving the power value P0 and/or the frequency value F0, the parameter control 224 provides the power value P0 and/or the frequency value F0 to the driver 228. The driver 228 creates an RF signal having the power value P0 and/or the frequency value F0 and provides the RF signal to the amplifier 230.

[00122] In one embodiment, the driver 228 generates an RF signal having a drive power value that is a function of the power value P0 and/or having a drive frequency value that is a function of the frequency value F0. For example, the drive power value is within a few, e.g. 1 thru 5, watts of the power value P0 and the drive frequency value is within a few, e.g. 1 thru 5, Hz of the frequency value F0.

[00123] The amplifier 230 amplifies the RF signal having the power value P0 and/or the frequency value F0 and generates an RF signal 221 that corresponds to the RF

signal received from the driver 228. For example, the RF signal 221 has a higher amount of power than that of the power value P0. As another example, the RF signal 221 has the same amount of power as that of the power value P0. The RF signal 221 is transferred via the cable ~~217~~ 223 and the impedance matching circuit 114 to the ~~known load 112~~ ESC 177 (Figure ~~2~~ 1).

[00124] When the power value P0 and/or the frequency value F0 are provided to the DAS 232 by the parameter control ~~222~~ 224 and the RF signal ~~121~~ 221 is generated, the voltage and current probe 238 measures values of the variable at the output 231. The voltage and current probe 238 sends the values of the variable to the host system 130 for the host system 130 to execute the method 102 (Figure 2), the method 340 (Figure 13), the method 351 (Figure 15), or the method 363 (Figure 17).

[00125] It should be noted that the in one embodiment, the voltage and current probe 238 is decoupled from the DSP 226. In some embodiments, the voltage and current probe 238 is coupled to the DSP 226. It should further be noted that the RF signal 215 generated during the state S1 and the RF signal 221 generated during the state S0 are portions of a combined RF signal. For example, the RF signal 215 is a portion of the combined RF signal that has a higher amount of power than the RF signal 221, which is another portion of the combined RF signal.

[00126] Figure 10 is a block diagram of an embodiment of a system 250 in which the voltage and current probe 238 and the communication device 233 are located outside the RF generator 220. In Figure 1, the voltage and current probe 110 is located within the x MHz RF generator to measure the variable at the output of the x MHz RF generator. The voltage and current probe 238 is located outside the RF generator 220 to measure the variable at the output 231 of the RF generator 220. The voltage and current probe 238 is associated, e.g., coupled, to the output 231 of the RF generator 220.

[00127] Figure 11 is a block diagram of an embodiment of a system 128 in which the values of the variable determined using the system 126 of Figure 1 are used. The system 128 includes an m MHz RF generator, an n MHz RF generator, an impedance matching circuit 115, an RF transmission line 287, and a plasma chamber 134. The plasma chamber 134 may be similar to the plasma chamber 175.

[00128] It should be noted that in an embodiment, the x MHz RF generator of Figure ~~2~~ 1 is similar to the m MHz RF generator and the y MHz RF generator of Figure ~~2~~ 1 is similar to the n MHz RF generator. As an example, x MHz is equal to m MHz and y MHz is

equal to n MHz. As another example, the x MHz generator and the m MHz generators have similar frequencies and the y MHz generator and the n MHz generator have similar frequencies. An example of similar frequencies is when the x MHz is within a window, e.g., within kHz or Hz, of the m MHz frequency. In some embodiments, the x MHz RF generator of Figure ~~2~~ 1 is not similar to the m MHz RF generator and the y MHz RF generator of Figure ~~2~~ 1 is not similar to the n MHz RF generator.

[00129] It is further noted that in various embodiments, a different type of sensor is used in each of the m MHz and n MHz RF generators than that used in each of the x MHz and y MHz RF generators. For example, a sensor that does not comply with the NIST standard is used in the m MHz RF generator. As another example, a voltage sensor that measures only voltage is used in the m MHz RF generator.

[00130] It should further be noted that in an embodiment, the impedance matching circuit 115 is similar to the impedance matching circuit 114 (Figure 1). For example, an impedance of the impedance matching circuit 114 is the same as an impedance of the impedance matching circuit 115. As another example, an impedance of the impedance matching circuit 115 is within a window, e.g., within 10-20%, of the impedance of the impedance matching circuit 114. In some embodiments, the impedance matching circuit 115 is not similar to the impedance matching circuit 114.

[00131] The impedance matching circuit 115 includes electrical components, e.g., inductors, capacitors, etc., to match an impedance of a power source coupled to the impedance matching circuit 115 with an impedance of a load coupled to the circuit 115. For example, the impedance matching circuit ~~114~~ 115 matches an impedance of a source coupled to the impedance matching circuit ~~114~~ 115, e.g., a combination of the m MHz RF generator, the n MHz RF generator, and cables coupling the m and n MHz RF generators to the impedance matching circuit ~~114~~ 115, etc., with an impedance of a load, e.g., a combination of the plasma chamber 134 and the RF transmission line 287, etc.

[00132] It should be noted that in an embodiment, the RF transmission line 287 is similar to the RF transmission line 113 (Figure 1). For example, an impedance of the RF transmission line 287 is the same as an impedance of the RF transmission line 113. As another example, an impedance of the RF transmission line 287 is within a window, e.g., within 10-20%, of the impedance of the RF transmission line 113. In various embodiments, the RF transmission line 287 is not similar to the RF transmission line 113.

matching circuit 114 (Figure 1) within the system 126 (Figure 1) by using a voltage probe and a voltage, e.g., peak voltage, etc., at a corresponding model node output, e.g., the node N4m, determined using the method 102 (Figure 2). Moreover, Figures 12A, 12~~C~~ B, and 12~~B~~ C are diagrams of embodiments of graphs 270, 274, and 277 that illustrate a correlation between current, e.g., root mean square (RMS) current, etc., that is measured the output, e.g., the node N4, of the system 126 (Figure 1) by using a current probe and a current, e.g., RMS current, etc., at a corresponding output, e.g., the node N4m, determined using the method 102 (Figure 2).

[00140] The voltage determined using the method 102 is plotted on an x-axis in each graph 268, 272, and 275 and the voltage measured with the voltage probe is plotted on a y-axis in each graph 268, 272, and 275. Similarly, the current determined using the method 102 is plotted on an x-axis in each graph 270, ~~227~~ 274, and 277 and the current measured with the current probe is plotted on a y-axis in each graph 270, 274, and 277.

[00141] The voltages are plotted in the graph 268 when the x MHz RF generator is on and the y MHz RF generator and a z MHz RF generator, e.g., 60 MHz RF generator, are off. Moreover, the voltages are plotted in the graph 272 when the y MHz RF generator is on and the x and z MHz RF generators are off. Also, the voltages are plotted in the graph 275 when the z MHz RF generator is on and the x and y MHz RF generators are off.

[00142] Similarly, currents are plotted in the graph 270 when the x MHz RF generator is on and the y MHz RF generator and a z MHz RF generator are off. Also, the currents are plotted in the graph 274 when the y MHz RF generator is on and the x and z MHz RF generators are off. Also, the currents are plotted in the graph 277 when the z MHz RF generator is on and the x and y MHz RF generators are off.

[00143] It can be seen in each graph 268, 272, and 275 that an approximately linear correlation exists between the voltage plotted on the y-axis of the graph and the voltage plotted on the x-axis of the graph. Similarly, it can be seen in each graph 270, 274, and 277 that an approximately linear correlation exists between the current plotted on the y-axis and the current plotted on the x-axis.

[00144] Figure 13 is a flowchart of an embodiment of the method 340 for determining wafer bias at a model node, e.g., the model node N4m, the model node N1m, the model node N2m, the model node N6m, etc., of the plasma system 126 (Figure 1). It should be noted that in some embodiments, wafer bias is a direct current (DC) voltage that is created

obtained for the first time and for the one or more additional times to determine the coefficients ax, bx, cx and the constant dx.

[00153] As another example of the operation 342, when the y MHz RF generator is on and the x and z MHz RF generators are off, a wafer bias is determined as ay*Vy + by*Iy + cy*sqrt (Py) + dy, where "ay" is a coefficient, "by" is a coefficient, "dy" is a constant, "Vy" is a voltage magnitude of the second complex voltage and current, "Iy" is a current magnitude of the second complex voltage and current, and "~~Px~~ Py" is a power magnitude of the second complex voltage and current. The power magnitude Py is a product of the current magnitude Iy and the voltage magnitude Vy. As yet another example of the operation 342, when the z MHz RF generator is on and the x and y MHz RF generators are off, a wafer bias is determined as az*Vz + bz*Iz + cz*sqrt (Pz) + dz, where "az" is a coefficient, "bz" is a coefficient, "dz" is a constant, "Vz" is a voltage magnitude of the second complex voltage and current, "Iz" is a current magnitude of the second complex voltage and current, and "Pz" is a power magnitude of the second complex voltage and current. The power magnitude Pz is a product of the current magnitude Iz and the voltage magnitude Vz.

[00154] As another example of the operation 342, when the x and y MHz RF generators are on and the z MHz RF generator is off, the wafer bias is determined as a sum of a first product, a second product, a third product, a fourth product, a fifth product, a sixth product, and a constant. The first product is a product of a first coefficient and the voltage magnitude Vx, the second product is a product of a second coefficient and the current magnitude Ix, the third product is a product of a third coefficient and a square root of the power magnitude Px, the fourth product is a product of a fourth coefficient and the voltage magnitude Vy, the fifth product is a product of a fifth coefficient and the current magnitude Iy, and the sixth product is a product of a sixth coefficient and a square root of the power magnitude Py. When the x and y MHz RF generators are on and the z MHz RF generator is off, the wafer bias is represented as axy*Vx + bxy*Ix + cxy*sqrt (Px) + dxy*Vy + exy*Iy + fxy*sqrt (Py) + gxy, where "axy", "bxy", "cxy", "dxy", "exy", "fxy", "dxy", "exy", and "fxy" are coefficients, and "gxy" is a constant.

[00155] As another example of the operation 342, when the y and z MHz RF generators are on and the x MHz RF generator is off, a wafer bias is determined as ayz*Vy + byz*Iy + cyz*sqrt (Py) + dyz*Vz + eyz*Iz + fyz*sqrt (Pz) + gyz, where "ayz", "byz", "cyz", "dyz", "eyz", and "fyz" are coefficients, and "gyz" is a constant. As yet another example of the operation 342, when the x and z MHz RF generators are on and the y MHz RF generator

[00161] As another example of determination of wafer bias at the output of the one or more models, wafer bias at the model node N6m is determined by the processor of the host system 130 based on voltage and current magnitudes determined at the model node N6m in a manner similar to that of determining wafer bias at the model node N2m based on voltage and current magnitudes determined at the model node N2m. To further illustrate, wafer bias ax*Vx + bx*Ix + cx*sqrt (Px) + dx, ay*Vy + by*Iy + cy*sqrt (Py) + dy, az*Vz + bz*Iz + cz*sqrt (Pz) + dz, axy*Vx + bxy*Ix + cxy*sqrt (Px) + dxy*Vy + exy*Iy + fxy*sqrt (Py) + gxy, axz*Vx + bxz*Ix + cxz*sqrt (Px) + dxz*Vz + exz*Iz + fxz*sqrt (Pz) + gxz, ayz*Vy + byz*Iy + cyz*sqrt (Py) + dyz*Vz + eyz*Iz + fyz*sqrt (Pz) + gyz, and axyz*Vx + bxyz*Ix + cxyz*sqrt (Px) + dxyz*Vy + exyz*Iy + fxyz*sqrt (Py) + gxyz*Vz + hxyz*Iz + ixyz*sqrt (Pz) + jxyz are determined at the model node N6m.

[00162] It should be noted that in some embodiments, wafer bias is stored within the storage HU 162 (Figure 1).

[00163] Figure 14 is a state diagram illustrating an embodiment of a wafer bias generator ~~340~~ 345, which is implemented within the host system 130 (Figure 1). When all of the x, y, and z MHz RF generators are off, wafer bias is zero or minimal at a model node, e.g., the model node N4m, N1m, N2m, N6m (Figure 1), etc. When the x, y, or z MHz RF generator is on and the remaining of the x, y, and z MHz RF generators are off, the wafer bias generator ~~340~~ 345 determines a wafer bias at a model node, e.g., the model node N4m, N1m, N2m, N6m, etc., as a sum of a first product a*V, a second product b*I, a third product c*sqrt(P), and a constant d, where V is a voltage magnitude of a complex voltage and current at the model node, I is a current magnitude of the complex voltage and current, P is a power magnitude of the complex voltage and current, a is a coefficient, b is a coefficient, c is a coefficient, and d is a constant. In various embodiments, a power magnitude at a model node is a product of a current magnitude at the model node and a voltage magnitude at the model node. In some embodiments, the power magnitude is a magnitude of delivered power.

[00164] When two of the x, y, and z MHz RF generators are on and the remaining of the x, y, and z MHz RF generators are off, the wafer bias generator ~~340~~ 345 determines a wafer bias at a model node, e.g., the model node N4m, N1m, N2m, N6m, etc., as a sum of a first product a12*V1, a second product b12*I1, a third product c12*sqrt(P1), a fourth product d12*V2, a fifth product e12*I2, a sixth product f12*sqrt(P2), and a constant g12, where "V1" is a voltage magnitude of a complex voltage and current at the model node determined by propagating a voltage measured at an output of a first one of the RF generators that is on, "I1"

is a current magnitude of the complex voltage and current determined by propagating a current measured at the output of the first RF generator that is on, "P1" is a power magnitude of the complex voltage and current determined as a product of V1 and I1, "V2" is a voltage magnitude of the complex voltage and current at the model node determined by propagating a voltage measured at an output of a second one of the RF generators that is on, "I2" is a current magnitude of the complex voltage and current determined by propagating the current measured at an output of the second RF generator that is on, "P2" is a power magnitude determined as a product of V2 and I2, each of "a12", "b12", "c12", "d12", "e12" and "f12" is a coefficient, and "g12" is a constant.

[00165] When all of the x, y, and z MHz RF generators are on, the wafer bias generator ~~340~~ 345 determines a wafer bias at a model node, e.g., the model node N4m, N1m, N2m, N6m, etc., as a sum of a first product a123*V1, a second product b123*I1, a third product c123*sqrt(P1), a fourth product d123*V2, a fifth product e123*I2, a sixth product f123*sqrt(P2), a seventh product g123*V3, an eighth product h123*I3, a ninth product i123*sqrt(P3), and a constant j123, where "V1" is a voltage magnitude of a complex voltage and current at the model node determined by propagating a voltage measured at an output of a first one of the RF generators, "I1" is a current magnitude of the complex voltage and current determined by propagating a current measured at the output of the first RF generator, "P1" is a power magnitude of the complex voltage and current determined as a product of V1 and I1, "V2" is a voltage magnitude of the complex voltage and current at the model node determined by propagating a voltage measured at an output of a second one of the RF generators, "I2" is a current magnitude of the complex voltage and current determined by propagating a current measured at the output of the second RF generator, "P2" is a power magnitude of the complex voltage and current determined as a product of V2 and I2, "V3" is a voltage magnitude of the complex voltage and current at the model node determined by propagating a voltage measured at an output of a third one of the RF generators, "I3" is a current magnitude of the complex voltage and current determined by propagating a current at the output of the third RF generator, "P3" is a power magnitude of the complex voltage and current determined as a product of V3 and I3, each of "a123", "b123", "c123", "d123", "e123", "f123", "g123", "h123", and "i123" is a coefficient, and "j123" is a constant.

[00166] Figure 15 is a flowchart of an embodiment of the method 351 for determining a wafer bias at a point along a path 353 (Figure 16) between the model node N4m (Figure 16) and the ESC model 125 (Figure 16). Figure 15 is described with reference

to Figure 16, which is a block diagram of an embodiment of a system 355 for determining a wafer bias at an output of a model.

[00167] In an operation 357, output of the x, y, or z MHz RF generator is detected to identify a generator output complex voltage and current. For example, the voltage and current probe 110 (Figure 1) measures complex voltage and current at the node N3 (Figure 1). In this example, the complex voltage and current is received from the voltage and current probe 110 via the communication device 185 (Figure 1) by the host system 130 (Figure 1) for storage within the storage HU 162 (Figure 1). Also, in the example, the processor of the host system 130 identifies the complex voltage and current from the storage HU 162.

[00168] In an operation 359, the processor of the host system 130 uses the generator output complex voltage and current to determine a projected complex voltage and current at a point along the path 353 between the model node N4m and the model node N6m. The path ~~161~~ 353 extends from the model node N4m to the model node N6m. For example, the fifth complex voltage and current is determined from the complex voltage and current measured at the output of the x MHz RF generator, the y MHz RF generator, or the z MHz RF generator. As another example, the complex voltage and current measured at the node N3 or the node N5 is propagated via the impedance matching model 104 to determine a complex voltage and current at the model node N4m (Figure 1). In the example, the complex voltage and current at the model node N4m is propagated via one or more elements of the RF transmission model 161 (Figure 16) and/or via one or more elements of the ESC model 125 (Figure 16) to determine complex voltage and current at a point on the path 353.

[00169] In an operation 361, the processor of the host system 130 applies the projected complex voltage and current determined at the point on the path 353 as an input to a function to map the projected complex voltage and current to a wafer bias value at the node N6m of the ESC model 125 (Figure 15). For example, when the x, y, or z MHz RF generator is on, a wafer bias at the model node N6m is determined as a sum of a first product a*V, a second product b*I, a third product c*sqrt(P), and a constant d, where, V is a voltage magnitude of the projected complex voltage and current at the model node N6m, I is a current magnitude of the projected complex voltage and current at the model node N6m, P is a power magnitude of the projected complex voltage and current at the model node N6m, a, b, and c are coefficients, and d is a constant.

voltage magnitude measured by the voltage probe 332 is a signal, the host system 334 determines wafer bias.

[00185] The system 126 (Figure 1) is cost effective compared to the system 330 and saves time and effort compared to the system 330. The system 330 includes the voltage probe 332, which does not need to be included in the system 126. There is no need to couple a voltage probe at the node N4, N1, or N2 of the system 126 to determine wafer bias. In the system 126, wafer bias is determined based on the impedance matching model 104, RF transmission model 161, and/or the ESC model 125 (Figure 1). Moreover, the system 330 includes the module 336, which also does not need to be included in the system 126. There is no need to spend time and effort to determine whether a complex voltage and current is a signal or noise. No such determination needs to be made by the host system 130 (Figure 1).

[00186] Figures 19A, 19B, and 19C show embodiments of graphs 328, ~~332~~ 333, and ~~336~~ 337to illustrate a correlation, e.g., a linear correlation, etc., between voltage, e.g., peak voltage, etc., that is measured at the output, e.g., the node N1, of the portion 195 (Figure 1) by using a voltage probe and a voltage, e.g., peak voltage, etc., at a corresponding model node output, e.g., the node N1m, determined using the method 102 (Figure 2). In each graph 328, ~~332~~ 333, and ~~336~~ 337, the measured voltage is plotted on a y-axis and the voltage determined using the method 102 is plotted on an x-axis.

[00187] Moreover, Figures 19A, 19B, and 19C show embodiments of graphs ~~330~~ 331, ~~334~~ 335, and 338 to illustrate a correlation, e.g., a linear correlation, etc., between wafer bias that is measured at the output N6 (Figure 1) by using a wafer bias probe and wafer bias at a corresponding model node output, e.g., the node N6m, determined using the method 340 (Figure 13), the method 351 (Figure 15), or the method 363 (Figure 17). In each graph ~~330~~ 331, ~~334~~ 335, and 338, the wafer bias determined using the wafer bias probe is plotted on a y-axis and the wafer bias determined using the method 340, the method 351, or the method 363 is plotted on an x-axis.

[00188] The voltages and wafer bias are plotted in the graphs 328 and ~~330~~ 331 when the y MHz and z MHz RF generators are on and the x MHz RF generator is off. Moreover, the voltages and wafer bias are plotted in the graphs ~~332~~ 333 and ~~334~~ 335 when the x MHz and z MHz RF generators are on and the y MHz RF generator is off. Also, the voltages are plotted in the graphs ~~336~~ 337 and 338 when the x MHz and y MHz RF generators are on and the z MHz RF generator is off.

[00189] Figure 20A is a diagram of an embodiment of graphs 276 and 278 to illustrate that there is a correlation between a wired wafer bias measured using a sensor tool, e.g., a metrology tool, a probe, a sensor, a wafer bias probe, etc., a model wafer bias that is determined using the method 340 (Figure 13), the method 351 (Figure 15), or the method 363 (Figure 17), and an error in the model bias. The wired wafer bias that is plotted in the graph 276 is measured at a point, e.g., a node on the RF transmission line 113, a node on the upper surface 183 (Figure 1) of the ESC 177, etc. and the model bias that is plotted in the graph 276 is determined at the corresponding model point, e.g., the model node N4m, the model node N1m, the model node N2m, the model node N6m, etc. (Figure 1), on the path 353 (Figure 16). The wired wafer bias is plotted along a y-axis in the graph 276 and the model bias is plotted along an x-axis in the graph 276.

[00190] The wired wafer bias and the model bias are plotted in the graph 276 when the x MHz RF generator is on, and the y and z MHz RF generators are off. Moreover, the model bias of graph 276 is determined using an equation a2*V2 + b2*I2 + c2*sqrt (P2) + d2, where "*" represents multiplication, "sqrt" represents a square root, "V2" represents voltage at the point along the path 353 (Figure 16), I2 represents current at the point, P2 represents power at the point, "a2" is a coefficient, "b2" is a coefficient, "c2" is a coefficient, and "d2" is a constant value.

[00191] The graph 278 plots an error, which is an error in the model bias at the point, on a y-axis and plots the model bias at the point on an x-axis. The model error is an error, e.g., a variance, a standard deviation, etc., in the model bias. The model error and the model bias are plotted in the graph 278 when the x MHz RF generator is on and the y and z MHz RF generators are off.

[00192] Figure 20B is a diagram of an embodiment of graphs 280 and 282 to illustrate that there is a correlation between a wired wafer bias, a model bias that is determined using the method 340 (Figure 13), the method 351 (Figure 15) or method 363 (Figure 17), and an error in the model bias. The graphs 280 and 282 are plotted in a manner similar to the graphs 276 and 278 (Figure ~~17A~~ 20A) except that the graphs 280 and 282 are plotted when the y MHz RF generator is on and the x and z MHz RF generators are off. Moreover, the model bias of the graphs 280 and 282 is determined using an equation a27*V27 + b27*I27 + c27*sqrt (P27) + d27, where "V27" represents a voltage magnitude at the point along the path 353 (Figure 16), "I27" represents a current magnitude at the point, "P27"

represents a power magnitude at the point, "a27" is a coefficient, "b27" is a coefficient, "c27" is a coefficient, and "d27" is a constant value.

[00193] Figure 20C is a diagram of an embodiment of graphs 284 and 286 to illustrate that there is a correlation between a wired wafer bias, a model bias that is determined using the method 340 (Figure 13), the method 351 (Figure 15) or method 363 (Figure 17), and an error in the model bias. The graphs 284 and 286 are plotted in a manner similar to the graphs 276 and 278 (Figure ~~17A~~ 20A) except that the graphs 284 and 286 are plotted when the z MHz RF generator is on and the x and y MHz RF generators are off. Moreover, the model bias of the graphs 284 and 286 is determined using an equation a60*V60 + b60*I60 + c60*sqrt (P60) + d60, where "V60" represents a voltage magnitude at the point along the path 353 (Figure 16), "I60" represents a current magnitude at the point, "P60" represents a power magnitude at the point, "a60" is a coefficient, "b60" is a coefficient, "c60" is a coefficient, and "d60" is a constant value.

[00194] Figure 20D is a diagram of an embodiment of graphs 288 and 290 to illustrate that there is a correlation between a wired wafer bias, a model bias that is determined using the method 340 (Figure 13), the method 351 (Figure 15) or method 363 (Figure 17), and an error in the model bias. The graphs 288 and 290 are plotted in a manner similar to the graphs 276 and 278 (Figure 20A) except that the graphs 288 and 290 are plotted when the x and y MHz RF generators are on, and the z MHz RF generator is off. Moreover, the model bias of the graphs 288 and 290 is determined using an equation a227*V2 + b227*I2 + c227*sqrt (P2) + d227*V27 + e227*I27 + f227*sqrt (P27) + g227, where "a227", "b227" and "c227", "d227", "e227" and "f227" are coefficients, and "g227" is a constant value.

[00195] Figure 20E is a diagram of an embodiment of graphs 292 and 294 to illustrate that there is a correlation between a wired wafer bias, a model bias that is determined using the method 340 (Figure 13), the method 351 (Figure 15) or method 363 (Figure 17), and an error in the model bias. The graphs 292 and 294 are plotted in a manner similar to the graphs 276 and 278 (Figure 20A) except that the graphs 292 and 294 are plotted when the x and z MHz RF generators are on, and the y MHz RF generator is off. Moreover, the model bias of the graphs 292 and 294 is determined using an equation a260*V2 + b260*I2 + c260*sqrt (P2) + ~~d20~~ 260*V60 + e260*I60 + f260*sqrt (P60) + g260, where "a260", "b260" "c260", "d260", "e260" and "f260" are coefficients, and "g260" is a constant value.

[00196] Figure 20F is a diagram of an embodiment of graphs 296 and 298 to illustrate that there is a correlation between a wired wafer bias, a model bias that is determined using the method 340 (Figure 13), the method 351 (Figure 15) or method 363 (Figure 17), and an error in the model bias. The graphs 296 and 298 are plotted in a manner similar to the graphs 276 and 278 (Figure 20A) except that the graphs 296 and 298 are plotted when the y and z MHz RF generators are on, and the x MHz RF generator is off. Moreover, the model bias of the graphs 296 and 298 is determined using an equation a2760*V27 + b2760*I27 + c2760*sqrt (P27) + d2760*V60 + e2760*I60 + f2760*sqrt (P60) + g2760, where "a2760", "b2760" "c2760", "d2760", "e2760" and "f2760" are coefficients, and "g2760" is a constant value.

[00197] Figure 20G is a diagram of an embodiment of graphs ~~302~~ 303 and ~~304~~ 305 to illustrate that there is a correlation between a wired wafer bias, a model bias that is determined using the method 340 (Figure 13), the method 351 (Figure 15) or method 363 (Figure 17), and an error in the model bias. The graphs ~~302~~ 303 and ~~304~~ 305 are plotted in a manner similar to the graphs 276 and 278 (Figure 20A) except that the graphs ~~302~~ 303 and ~~304~~ 305 are plotted when the x, y and z MHz RF generators are on. Moreover, the model bias of the graphs ~~302~~ 303 and ~~304~~ 305 is determined using an equation a22760*V2 + b22760*I2 + c22760*sqrt (P2) + d22760*V60 + e22760*I60 + f22760*sqrt (P60) + g22760*V27 + h22760*I27 + i22760*sqrt (P27) + j22760, where "a22760", "b22760", "c22760", "d22760", "e22760", "f22760" "g22760", "h22760", and "i22760" are coefficients and " j22760" is a constant value.

[00198] Figure 21 is a block diagram of an embodiment of the host system 130. The host system 130 includes a processor 168, the storage HU 162, an input HU 380, an output HU 382, an input/output (I/O) interface 384, an I/O interface 386, a network interface controller (NIC) 388, and a bus ~~390~~ 392. The processor 168, the storage HU 162, the input HU 380, the output HU 382, the I/O interface 384, the I/O interface 386, and the NIC 388 are coupled with each other via a bus 392. Examples of the input HU 380 include a mouse, a keyboard, a stylus, etc. Examples of the output HU 382 include a display, a speaker, or a combination thereof. The display may be a liquid crystal display, a light emitting diode display, a cathode ray tube, a plasma display, etc. Examples of the NIC 388 include a network interface card, a network adapter, etc.

[00199] Examples of an I/O interface include an interface that provides compatibility between pieces of hardware coupled to the interface. For example, the I/O interface 384 converts a signal received from the input HU 380 into a form, amplitude, and/or

6. The method of claim 4, wherein the empirical modeling data includes data obtained based on measurements of wafer bias at the ESC, based on determinations of magnitudes of complex voltages and currents, and based on an application of estimation statistical method to the measurements of the wafer bias at the ESC and the magnitudes of complex voltage and current, the determination of the magnitudes of complex voltages and currents made based on the model of the impedance matching ~~model~~ circuit and the model for at least part of the path.

7. The method of claim 1, wherein the function includes a sum of a first product, a second product, a third product, and a constant, wherein the first product is a product of a coefficient and a voltage magnitude, the second product is a product of a coefficient and a current magnitude, the third product is a product of a coefficient and a square root of power magnitude, the voltage magnitude extracted from the projected complex voltage and current, the current magnitude extracted from the projected complex voltage and current, the power magnitude calculated from the current magnitude and the voltage magnitude.

8. A method for determining wafer bias, the method comprising:

receiving one or more generator output complex voltages and currents measured at one or more outputs of one or more generators, the one or more generators coupled to an impedance matching circuit, the impedance matching circuit coupled via a radio frequency (RF) transmission line to an electrostatic chuck (ESC) of a plasma chamber;

determining from the one or more generator output complex voltages and currents projected complex voltage and current at a point along a path between a model of the impedance matching circuit and a model of the ESC, the models characterizing physical components along the path; and

calculating a wafer bias at the point by using the projected complex voltage and current as an input to a function.

9. The method of claim 8, wherein the function is characterized by a summation of values that represent physical attributes of the path, wherein the projected complex voltage and current is used in the summation of the values.

10. The method of claim 9, wherein the physical attributes of the path are derived values from test data.

11. The method of claim 8, wherein the function is a sum of characterized values and a constant, the characterized values including magnitudes and coefficients, the magnitudes derived from the projected complex voltage and current, the coefficients and the constant incorporating empirical modeling data.

12. The method of claim 11, wherein the coefficients are coefficients of the magnitudes.

13. The method of claim 11, wherein the empirical modeling data includes data obtained based on measurements of wafer bias at the ESC, based on determinations of magnitudes of complex voltages and currents, and based on an application of estimation statistical method to the measurements of the wafer bias at the ESC and the magnitudes of complex voltage and current, the determination of the magnitudes of complex voltages and currents made based on the model of the impedance matching ~~model~~ circuit and ~~the~~ a model for at least part of the path.

14. The method of claim 8, wherein the function includes a sum of a first product, a second product, a third product, and a constant, wherein the first product is a product of a coefficient and a voltage magnitude, the second product is a product of a coefficient and a current magnitude, the third product is a product of a coefficient and a square root of power magnitude, the voltage magnitude identified from the projected complex voltage and current, the current magnitude identified from the projected complex voltage and current, the power magnitude determined from the current magnitude and the voltage magnitude.

15. A method for determining wafer bias, the method comprising:

identifying a first complex voltage and current measured at an output of a radio frequency (RF) generator when the RF generator is coupled to a plasma chamber via an impedance matching circuit, the impedance matching circuit having an input coupled to the output of the RF generator and an output coupled to an RF transmission line;

one or more radio frequency (RF) generators for generating one or more RF signals, the one or more RF generators associated with one or more voltage and current probes, wherein the one or more voltage and current probes are configured to measure one or more complex voltages and currents at corresponding one or more outputs of the one or more RF generators;

an impedance matching circuit coupled to the one or more RF generators;

a plasma chamber coupled to the impedance matching circuit via an RF transmission line, the plasma chamber including an electrostatic chuck (ESC), the ESC coupled to the RF transmission line; and

a processor coupled to the one or more RF generators, the processor configured to:

receive the one or more complex voltages and currents;

determine from the one or more complex voltages and currents projected complex voltage and current at a point along a path between a model of the impedance matching circuit and a model of the ESC, the models characterizing physical components along the path; and

calculate a wafer bias at the point by using the projected complex voltage and current as an input to a function.

31. The ~~method of claim~~ plasma system of claim 30, wherein the function is characterized by a summation of values that represent physical attributes of the path, wherein the projected complex voltage and current is used in the summation of the values.

32. The ~~method of claim~~ plasma system of claim 31, wherein the physical attributes of the path are derived values from test data.

33. The ~~method of claim~~ plasma system of claim 30, wherein the function is a sum of characterized values and a constant, the characterized values including magnitudes and coefficients, the magnitudes derived from the projected complex voltage and current, the coefficients and the constant incorporating empirical modeling data.

34. The ~~method of claim~~ plasma system of claim 33, wherein the coefficients are coefficients of the magnitudes.

35. The ~~method of claim~~ plasma system of claim 33, wherein the empirical modeling data includes data obtained based on measurements of wafer bias at the ESC, based on determinations of magnitudes of complex voltages and currents, and based on an application of estimation statistical method to the measurements of the wafer bias at the ESC and the magnitudes of complex voltage and current, the determination of the magnitudes of complex voltages and currents made based on the impedance matching model and ~~the~~ a model for at least part of the path.

36. The plasma system of claim 30, wherein the function includes a sum of a first product, a second product, a third product, and a constant, wherein the first product is a product of a coefficient and a voltage magnitude, the second product is a product of a coefficient and a current magnitude, the third product is a product of a coefficient and a square root of power magnitude, the voltage magnitude extracted from the projected complex voltage and current, the current magnitude extracted from the projected complex voltage and current, the power magnitude calculated from the current magnitude and the voltage magnitude.