

A MODULATION TECHNIQUE FOR TRANSMITTING MULTIPLE HIGH DATA RATE SIGNALS THROUGH A BAND LIMITED CHANNEL

The present invention relates to a modulation technique which transmits multiple a high data rate signals through a band limited channel.

5 It is always desirable to provide data at higher data rates through channels which have limited bandwidth. Many modulation techniques have been developed for increasing the data rate through a channel. For example, M-ary phase shift keyed (PSK) and Quadrature Amplitude Modulation (QAM) techniques permit compression by encoding a plurality of data bits in each transmitted
10 symbol. Such systems have constraints associated with them. First, the hardware associated with such systems is expensive. This is because these techniques require a high level of channel linearity in order to operate properly. Consequently, extensive signal processing must be performed for carrier tracking, symbol recovery, interpolation and signal shaping. Second, such techniques
15 are sensitive to multipath effects. These effects need to be compensated for in the receiver. Third, these systems often require bandwidths beyond those available in some applications (for example in-band on-channel broadcast FM subcarrier service) for the desired data rates.

It is also desirable to provide for several data signals through a channel.
20 Some modulation techniques utilize the channel completely, while others leave some aspect of the channel unused. Frequency domain multiplexing and time domain multiplexing are two techniques for sharing a channel among a plurality of signals. By sharing the channel in this manner, the overall throughput through the channel is increased.

25 In accordance with principles of the present invention, a digital data modulator includes a source of a plurality of digital data signals having a common data bit period. A plurality of encoders each encode a corresponding one of the plurality of digital data signals using a variable pulse width code

having edges occurring in respective non-overlapping intervals within the data bit period. A plurality of pulse signal generators each generate respective pulses representing the edges of the corresponding one of the encoded plurality of digital data signals. A carrier signal generator generates a carrier signal having
5 carrier pulses corresponding to the respective pulses.

In accordance with another aspect of the present invention, a digital data demodulator includes a source of a modulated signal including successive bit periods, each bit period having a plurality of non-overlapping intervals respectively associated with corresponding intervals in successive bit periods, each
10 interval containing a carrier pulse, spaced relative to carrier pulses in other associated intervals, representing a corresponding variable pulse width encoded digital data signal. A detector demodulates the modulated signal to generate pulses corresponding to received carrier pulses. A plurality of decoders each decode pulses received in a respective one of the plurality of associated intervals
15 in the bit period to generate the corresponding digital data signal.

The technique according to the principles of the present invention provides for simultaneous transmission of a plurality of independent high data rate signal through a single channel. A system according to the present invention may be implemented using relatively inexpensive circuitry, is insensitive to multipath
20 interference, and provides substantial bandwidth compression.

Brief Description of the Drawing

In the drawing:

Fig. 1 is a block diagram of a modulator for generating a relatively high data rate signal in a relatively narrow bandwidth;

25 Fig. 2 is a waveform diagram useful in understanding the operation of the modulator illustrated in Fig. 1;

Fig. 3 is a block diagram of a receiver which can receive a signal modulated as illustrated in Fig. 1;

Fig. 4 is a spectrum diagram useful in understanding an application of the modulation technique illustrated in Figs. 1 and 2;

Fig. 5 is a block diagram of an FM broadcast transmitter incorporating an in-band-on-channel digital transmission channel implemented using the

5 modulation technique illustrated in Figs. 1 and 2;

Fig. 6 is a block diagram of an FM broadcast receiver which can receive a signal modulated by an FM broadcast transmitter illustrated in Fig. 5;

Fig. 7 is a waveform diagram useful in understanding the operation of a modulator in accordance with principles of the present invention;

10 Fig. 8 is a block diagram of another embodiment of the modulator of Figs. 1 and 2 for also transmitting an auxiliary data signal along with the high data rate data signal;

Fig. 9 is a block diagram of a receiver which can receive the signal produced by the modulator illustrated in Fig. 8;

15 Fig. 10 is a waveform diagram useful in understanding the operation of a modulator in accordance with principles of the present invention;

Fig. 11 is a block diagram of a modulator according to principles of the present invention;

20 Fig. 12 is a block diagram of a receiver which can receive the signal produced by the modulator illustrated in Fig. 11, according to the present invention.

Fig. 1 is a block diagram of a modulator for generating a high data rate, narrow band signal. In Fig. 1, an input terminal IN receives a high data rate digital signal. The input terminal IN is coupled to an input terminal of an encoder 10. An output terminal of the encoder 10 is coupled to an input terminal of a differentiator 20. An output terminal of the differentiator 20 is coupled to an input terminal of a level detector 25. An output terminal of the level detector 25 is coupled to a first input terminal of a mixer 30. A local oscillator 40 is coupled to a second input terminal of the mixer 30. An output terminal of the mixer 30

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is coupled to an input terminal of a bandpass filter (BPF) 50. An output terminal of the BPF 50 is coupled to an output terminal OUT, which generates a modulated signal representing the digital signal at the input terminal IN.

Fig. 2 is a waveform diagram useful in understanding the operation of the modulator illustrated in Fig. 1. Fig. 2 is not drawn to scale in order to more clearly illustrate the waveforms. In the illustrated embodiment, the high data rate digital signal at the input terminal IN is a bilevel signal in non-return-to-zero (NRZ) format. This signal is illustrated as the top waveform in Fig. 2. The NRZ signal carries successive bits, each lasting for a predetermined period called the bit period, shown by dashed lines in the NRZ signal, and having a corresponding frequency called the bit rate. The level of the NRZ signal represents the value of that bit, all in a known manner. The encoder 10 operates to encode the NRZ signal using a variable pulse width code. In the illustrated embodiment, the variable pulse width code is a variable aperture code. Variable aperture coding is described in detail in International Patent Application PCT/US99/05301 of Chandra Mohan, filed March 11, 1999. In this patent application, an NRZ signal is phase encoded in the following manner.

Each bit period in the NRZ signal is coded as a transition in the encoded signal. An encoding clock at a multiple M of the bit rate is used to phase encode the NRZ signal. In the above mentioned patent application, the encoding clock runs at a rate M which is nine times the bit rate. When the NRZ signal transitions from a logic '1' level to a logic '0' level, a transition is made in the encoded signal eight encoding clock cycles ($M-1$) from the previous transition. When the NRZ signal transitions from a logic '0' level to a logic '1' level, a transition is made in the encoded signal 10 encoding clock cycles ($M+1$) from the previous transition. When the NRZ signal does not transition, that is if successive bits have the same value, then a transition is made in the encoded signal nine encoding clock cycles (M) from the last transition. The variable aperture coded signal (VAC) is illustrated as the second waveform in Fig. 2.

The variable aperture coded signal (VAC) is differentiated by the differentiator 20 to produce a series of pulses time aligned with transitions in the VAC signal. The differentiator also gives a 90 degree phase shift to the VAC modulating signal. Leading edge transitions produce positive-going pulses and trailing edge transitions produce negative-going pulses, all in a known manner.

The differentiated VAC signal $\frac{\partial VAC}{\partial t}$ is illustrated as the third signal in Figure 2.

The $\frac{\partial VAC}{\partial t}$ signal is level detected by the level detector 25 to generate a series

of trilevel pulses having constant amplitudes. When the differentiated VAC

signal $\frac{\partial VAC}{\partial t}$ has a value greater than a positive threshold value, a level signal is

generated having a high value; when it has a value less than a negative threshold value, a level signal is generated having a low value, otherwise it has a center value, all in a known manner. The level signal is shown as the fourth signal (LEVEL) in Fig. 2.

The LEVEL signal modulates a carrier signal from the local oscillator 40 in the mixer 30. A positive pulse produces a pulse of carrier signal having a first phase, and a negative pulse produces a pulse of carrier signal having a second phase. The first and second phases are preferably substantially 180 degrees out of phase. This carrier signal pulse is preferably substantially one coding clock period long, and in the illustrated embodiment, has a duration of substantially 1/9 of the NRZ bit period. The frequency of the local oscillator 40 signal is selected so that preferably at least 10 cycles of the local oscillator signal can occur during the carrier signal pulse time period. In Fig. 2, the carrier signal CARR is illustrated as the bottom waveform in which the carrier signal is represented by vertical hatching within respective rectangular envelopes. In the CARR signal illustrated in Fig. 2, the phase of carrier pulses generated in response to positive-going LEVEL pulses is represented by a "+", and the phase of carrier pulses generated in response to negative-going LEVEL pulses is represented by a "-". The "+" and "-" represent only substantially 180 degree phase differences and are not intended to represent any absolute phase.

The BPF 50 filters out all "out-of-band" Fourier components in the CARR signal, as well as the carrier component itself and one of the sidebands, leaving only a single sideband. The output signal OUT from the BPF 50, thus, is a single-side-band (SSB) phase or frequency modulated signal representing the NRZ data signal at the input terminal IN. This signal may be transmitted to a receiver by any of the many known transmission techniques.

Fig. 3 is a block diagram of a receiver which can receive a signal modulated by the modulator illustrated in Figs. 1 and 2. In Fig. 3, an input terminal IN is coupled to a source of a signal modulated as described above with reference to Figs. 1 and 2. The input terminal IN is coupled to an input terminal of a BPF 110. An output terminal of the BPF 110 is coupled to an input terminal of an integrator 120. An output terminal of the integrator 120 is coupled to an input terminal of a limiting amplifier 130. An output terminal of the limiting amplifier 130 is coupled to an input terminal of a detector 140. An output terminal of the detector 140 is coupled to an input terminal of a decoder 150. An output terminal of the decoder 150 reproduces the NRZ signal represented by the modulated signal at the input terminal IN and is coupled to an output terminal OUT.

In operation, the BPF 110 filters out out-of-band signals, passing only the modulated SSB signal, described above. The integrator 120 reverses the 90 degree phase shift which is introduced by the differentiator 20 (of Fig. 1). The limiting amplifier 130 restricts the amplitude of the signal from the integrator 120 to a constant amplitude. The signal from the limiting amplifier 130 corresponds to the carrier pulse signal CARR illustrated in Fig. 2. The detector 140 is either an FM discriminator, or a phase-locked loop (PLL) used to demodulate the FM or PM modulated, respectively, carrier pulse signals. The detector 140 detects the carrier pulses and generates a bilevel signal having transitions represented by the phase and timings of those pulses. The output of the detector 140 is the variable bit width signal corresponding to the VAC signal in Fig. 2. The decoder 150 performs the inverse operation of the encoder 10 (of Fig. 1), and generates the NRZ signal, corresponding to the NRZ signal in Fig. 2,

at the output terminal OUT. The above mentioned U.S. Patent application (RCA 88,945) describes a decoder 150 which may be used in Fig. 3. The NRZ signal at the output terminal OUT is then processed by utilization circuitry (not shown).

Because the carrier pulses (signal CARR in Fig. 2) occur at well defined
5 times with respect to each other, and because those pulses are limited in duration, it is possible to enable the detector 140 only at times when pulses are expected. For example, in the illustrated embodiment, as described in detail above, each pulse has a duration substantially $1/9$ of the time between NRZ signal transition times. After a carrier pulse is received $8/9$ of the time between
10 NRZ signal transitions since the preceding carrier pulse (representing a trailing edge), succeeding pulses are expected only at $9/9$ (no transition) or $10/9$ (leading edge) of the time between NRZ signal transitions from that pulse. Similarly, after a carrier pulse is received $10/9$ of the time between NRZ signal transitions since the preceding carrier pulse (representing a leading edge), succeeding pulses are
15 expected only at $8/9$ (trailing edge) or $9/9$ (no transition) of the time between NRZ signal transitions from that pulse. The detector 140 only need be enabled when a carrier pulse is expected, and only in the temporal neighborhood of the duration of the expected pulse.

A windowing timer, illustrated as 160 in phantom in Fig. 3, has an input
20 terminal coupled to a status output terminal of the detector 140 and an output terminal coupled to an enable input terminal of the detector 140. The windowing timer 160 monitors signals from the detector 140 and enables the detector only when a carrier pulse is expected and only in the temporal neighborhood of the duration of that pulse, as described above.

25 In the illustrated embodiment, the energy in the modulated signal lies primarily between 0.44 ($8/18$) and 0.55 ($10/18$) times the bit rate, and consequently has a bandwidth of 0.11 times the bit rate. This results in increasing the data rate through the bandwidth by nine times. Other compression ratios are easily achieved by changing the ratio of the encoding

clock to the bit rate, with trade-offs and constraints one skilled in the art would readily appreciate.

The system described above may be implemented with less sophisticated circuitry than either M-ary PSK or QAM modulation techniques in both the transmitter and receiver. More specifically, in the receiver, after the modulated signal is extracted, limiting amplifiers (e.g. 130) may be used, which is both less expensive and saves power. Also both the encoding and decoding of the NRZ signal may be performed with nominally fast programmable logic devices (PLDs). Such devices are relatively inexpensive (currently \$1 to \$2). In addition, there is no intersymbol interference in this system, so waveform shaping is not required. Further, there are no tracking loops required, except for the clock recovery loop.

Because, as described above, carrier transmission occurs only at bit boundaries and does not continue for the entire bit period, temporal windowing may be used in the receiver to detect received carrier pulses only at times when pulses are expected. Consequently, there are no multi-path problems with the present system.

One application for the modulation technique described above is to transmit CD quality digital music simultaneously with FM monophonic and stereophonic broadcast audio signals. Fig. 4 is a spectrum diagram useful in understanding this application of the modulation technique illustrated in Figs. 1 and 2. Fig. 4a illustrates the power envelope for FM broadcast signals in the United States. In Fig. 4a, the horizontal line represents frequency, and represents a portion of the VHF band somewhere between approximately 88 MHz and approximately 107 MHz. Signal strength is represented in the vertical direction. The permitted envelopes of spectra of two adjacent broadcast signals are illustrated. Each carrier is illustrated as a vertical arrow. Around each carrier are sidebands which carry the broadcast signal FM modulated on the carrier.

In the United States, FM radio stations may broadcast monophonic and stereophonic audio at full power in sidebands within 100 kHz of the carrier. In Fig. 4a these sidebands are illustrated unhatched. The broadcaster may

broadcast other information in the sidebands from 100 kHz to 200 kHz, but power transmitted in this band must be 30 dB down from full power. These sidebands are illustrated hatched. Adjacent stations (in the same geographical area) must be separated by at least 400 kHz.

5 The upper sideband above the carrier of the lower frequency broadcast signal in Fig. 4a is illustrated in the spectrum diagram of Fig. 4b. In Fig. 4b, the vertical direction represents modulation percentage. In Fig. 4b, the monophonic audio signal $L + R$ is transmitted in the 0 to 15 kHz sideband at 90% modulation level. The $L - R$ audio signal is transmitted as a double-sideband-suppressed-
10 carrier signal around a suppressed subcarrier frequency of 38 kHz at 45% modulation level. A lower sideband (lsb) runs from 23 kHz to 38 kHz, and an upper sideband (usb) runs from 38 kHz to 53 kHz. A 19 kHz pilot tone (one-half the frequency of the suppressed carrier) is also included in the sidebands around the main carrier. Thus, 47 kHz in both the upper sideband (Fig. 4b) and the
15 lower sideband (not shown) around the main carrier (i.e. from 53 kHz to 100 kHz) remains available to the broadcaster to broadcast additional information at full power. As described above, from 100 kHz to 200 kHz transmitted power must be 30 dB down from full power.

 Using the modulation technique illustrated in Figs. 1 and 2, described
20 above, a 128 kilobit-per-second (kbps) signal, containing an MP3 CD quality audio signal, may be encoded and transmitted in a bandwidth less than 20 kHz. This digital audio signal may be placed in the space between 53 kHz and 100 kHz in the upper sideband (for example) and transmitted as a subcarrier signal along with the regular broadcast stereo audio signal, as illustrated in Fig. 4b. In
25 Fig. 4b, the digital audio signal is the SSB signal described above centered at 70 kHz, and runs from approximately 60 kHz to 80 kHz. This signal is within 100 kHz of the main carrier and, thus, may be transmitted at full power.

 Fig. 5 is a block diagram of an FM broadcast transmitter incorporating an in-band-on-channel digital transmission channel implemented according to the
30 modulation technique described above with reference to Figs. 1 through 3. In

Fig. 5, those elements which are the same as those illustrated in Fig. 1 are enclosed in a dashed rectangle labeled "Fig. 1", are designated with the same reference numbers and are not described in detail below. The combination of the encoder 10, differentiator 20, level detector 25, mixer 30, oscillator 40 and BPF 50 generates an SSB phase or frequency modulated signal (CARR of Fig. 2) representing a digital input signal (NRZ of Fig. 2), all as described above with reference to Figs. 1 and 2. An output terminal of the BPF 50 is coupled to an input terminal of an amplifier 60. An output terminal of the amplifier 60 is coupled to a first input terminal of a second mixer 70. A second oscillator 80 is coupled to a second input terminal of the second mixer 70. An output terminal of the second mixer 70 is coupled to an input terminal of a first filter/amplifier 260. An output terminal of the first filter/amplifier 260 is coupled to a first input terminal of a signal combiner 250.

An output terminal of a broadcast baseband signal processor 210 is coupled to a first input terminal of a third mixer 220. A third oscillator 230 is coupled to a second input terminal of the third mixer 220. An output terminal of the third mixer 220 is coupled to an input terminal of a second filter/amplifier 240. An output terminal of the second filter/amplifier 240 is coupled to a second input terminal of the signal combiner 250. An output terminal of the signal combiner 250 is coupled to an input terminal of a power amplifier 270, which is coupled to a transmitting antenna 280.

In operation, the encoder 10 receives a digital signal representing the digital audio signal. In a preferred embodiment, this signal is an MP3 compliant digital audio signal. More specifically, the digital audio data stream is forward-error-correction (FEC) encoded using a Reed-Solomon (RS) code. Then the FEC encoded data stream is packetized. This packetized data is then compressed by the circuitry illustrated in Fig. 1, into an SSB signal, as described in detail above.

The frequency of the signal produced by the oscillator 40 is selected to be 10.7 MHz, so the digital information from the encoder 10 is modulated around a center frequency of 10.7 MHz. The modulation frequency may be any

frequency, but is more practically selected so that it corresponds to the frequencies of existing low cost BPF filters. For example, typical BPF filters have center frequencies of 6 MHz, 10.7 MHz, 21.4 MHz, 70 MHz, 140 MHz, etc. In the illustrated embodiment, 10.7 MHz is selected for the modulating frequency, and the BPF 50 is implemented as one of the existing 10.7 MHz filters. The filtered SSB signal from the BPF 50 is amplified by amplifier 60 and up-converted by the combination of the second mixer 70 and second oscillator 80. In the illustrated embodiment, the second oscillator 80 generates a signal at 77.57 MHz and the SSB is up-converted to 88.27 MHz. This signal is filtered and further amplified by the first filter/amplifier 260.

The broadcast baseband signal processor 210 receives a stereo audio signal (not shown) and performs the signal processing necessary to form the baseband composite stereo signal, including the L + R signal at baseband, the double-sideband-suppressed-carrier L - R signal at a (suppressed) carrier frequency of 38 kHz and a 19 kHz pilot tone, all in a known manner. This signal is then modulated onto a carrier signal at the assigned frequency of the FM station. The third oscillator 230 produces a carrier signal at the assigned broadcast frequency which, in the illustrated embodiment, is 88.2 MHz. The third mixer 220 generates a modulated signal modulated with the baseband composite monophonic and stereophonic audio signals as illustrated in Fig. 4b. The modulated signal, at a carrier frequency of 88.2 MHz and with the standard broadcast audio sidebands illustrated in Fig. 4b, is then filtered and amplified by the second filter/amplifier 240. This signal is combined with the SSB modulated digital signal at a center frequency of 88.27 MHz from the first filter/amplifier 260 to form a composite signal. This composite signal, thus, includes both the standard broadcast stereophonic audio sidebands modulated on the carrier at 88.2 MHz, and the SSB modulated signal carrying the digital audio signal centered at 70 kHz above the carrier (88.27 MHz), as illustrated in Fig. 4b. This composite signal is then power amplified by the power amplifier 270 and supplied to the transmitting antenna 280 for transmission to FM radio receivers.

Fig. 6 is a block diagram of an FM broadcast receiver which can receive a signal modulated by an FM broadcast transmitter illustrated in Fig. 5. In Fig. 6, those elements which are the same as those illustrated in Fig. 3 are outlined with a dashed rectangle labeled "Fig. 3", are designated with the same reference numbers and are not described in detail below. In Fig. 6, a receiving antenna 302 is coupled to an RF amplifier 304. An output terminal of the RF amplifier 304 is coupled to a first input terminal of a first mixer 306. An output terminal of a first oscillator 308 is coupled to a second input terminal of the first mixer 306. An output terminal of the first mixer 306 is coupled to respective input terminals of a BPF 310 and a tunable BPF 110. An output terminal of the BPF 310 is coupled to an input terminal of an intermediate frequency (IF) amplifier 312 which may be a limiting amplifier. An output terminal of the IF amplifier 312 is coupled to an input terminal of an FM detector 314. An output terminal of the FM detector 314 is coupled to an input terminal of an FM stereo decoder 316.

In operation, the RF amplifier 304 receives and amplifies RF signals from the receiving antenna 304. The first oscillator 308 generates a signal at 98.9 MHz. The combination of the first oscillator 308 and the first mixer 306 down-converts the 88.2 MHz main carrier signal to 10.7 MHz, and the SSB digital audio signal from 88.27 MHz to 10.63 MHz. The BPF 310 passes only the 53 kHz of FM stereo signal sidebands (L+R and L-R) around 10.7 MHz in a known manner. The IF amplifier 312 amplifies this signal and provides it to an FM detector 314 which generates the baseband composite stereo signal. The FM stereo decoder 316 decodes the baseband composite stereo signal to generate monophonic and/or stereophonic audio signals (not shown) representing the transmitted audio signals, all in a known manner.

In the illustrated embodiment, the tunable BPF 110 is tuned to a center frequency of 10.63 MHz, and passes only the 20 kHz digital audio signal around that frequency. In the illustrated embodiment, the passband of the BPF 110 runs from 10.53 MHz to 10.73 MHz. The combination of the BPF 110, integrator 120, limiting amplifier 130, detector 140, decoder 150 and windowing timer

160 operates to extract the modulated digital audio signal, and demodulate and decode that signal to reproduce the digital audio signal, in the manner described above with reference to Fig. 3. The digital audio signals from the decoder 150 are processed in an appropriate manner by further circuitry (not shown) to
5 generate audio signals corresponding to the transmitted digital audio signal. More specifically, the signal is depacketized, and any errors introduced during transmission are detected and corrected. The corrected bit stream is then converted to a stereo audio signal, all in a known manner.

The embodiment described above provides the equivalent compression
10 performance of a 1024 QAM system. However, in practice QAM systems are limited to around 256 QAM due to the difficulty of correcting noise and multipath intersymbol interference resulting from the tight constellation spacing. The above system has no ISI problem because of the narrow and widely spaced carrier pulses. In short, higher data rates may be transmitted in narrower
15 bandwidth channels with none of the problems associated with other techniques, such as QAM.

Referring back to Fig. 2, in the CARR signal, it may be seen that there are relatively wide gaps between carrier pulses during which no carrier signal is transmitted. These gaps may be further utilized. Fig. 7 is a more detailed
20 waveform diagram of the CARR signal useful in understanding the operation of a modulator which can utilize these gaps. As described above, in the encoder 10 illustrated in Fig. 1 an encoding clock signal has a period one-ninth of the bit period of the NRZ signal. Dashed vertical lines in Fig. 7 represent encoding clock signal periods. In Fig. 7, a bit period is illustrated from time t1 to time t10 to
25 illustrate that there are nine clock periods in one bit period. However, this bit period is not necessarily time aligned with the NRZ input signal, and will most likely be delayed with respect to the NRZ signal.

Permitted time locations of carrier pulses are represented by dashed rectangles. A carrier pulse may occur either 8, 9 or 10 clock pulses after a
30 preceding one. Thus, carrier pulses may occur in any one of three adjacent clock

periods. Carrier pulse A is assumed to be 8 clock pulses from the previous one, carrier pulse B is assumed to be 9 clock pulses from the preceding one, and carrier pulse C is assumed to be 10 clock pulses from the preceding one.

As described above, when a carrier pulse is 8 clock pulses from the preceding one (A), this indicates a trailing edge in the NRZ signal, and can only be immediately followed by either a 9 clock pulse interval (D), representing no change in the NRZ signal, or a 10 clock pulse interval (E), representing a leading edge in the NRZ signal. Similarly when a carrier pulse is 10 clock pulses from the preceding one (C), this indicates a trailing edge in the NRZ signal, and can only be immediately followed by either an 8 clock pulse interval (E), representing a leading edge in the NRZ signal, or 9 clock pulse interval (F), representing no change in the NRZ signal. When a carrier pulse is 9 clock pulses from the preceding one (B), this indicates no change in the NRZ signal, and can be immediately followed by either an 8 clock pulse (D), representing a trailing edge in the NRZ signal, a 9 clock pulse (E), representing no change in the NRZ signal, or a 10 clock pulse (F) interval, representing a leading edge in the NRZ signal. This is all illustrated on Fig. 7. It is apparent that of the nine encoding clock periods in an NRZ bit period, a first interval of the bit period, consisting of one of three adjacent clock periods (t_1 - t_4), can potentially contain a carrier pulse, while a second interval, consisting of the other six clock periods (t_4 - t_{10}), cannot have a carrier pulse.

During the interval when no carrier pulses may be produced in the CARR signal (t_4 - t_{10}), other auxiliary data may be modulated on the carrier signal. This is illustrated in Fig. 7 as a rounded rectangle (AUX DATA) with vertical hatching. Respective guard periods of Δt each, a first after the last potential carrier pulse (C) in a bit period and a second before the next succeeding potential carrier pulse (D) in the next bit period surrounding this gap, are maintained to minimize potential interference between the carrier pulses (A) - (F) carrying the digital audio signal and the carrier modulation (AUX DATA) carrying the auxiliary data.

Fig. 8 is a block diagram of an embodiment of a modulating system which can implement the inclusion of auxiliary data in the modulated encoded data stream. In Fig. 8, those elements which are the same as those illustrated in Fig. 1 are designated by the same reference number and are not described in detail below. In Fig. 8, a source (not shown) of auxiliary data (AUX) is coupled to an input terminal of a first-in-first-out (FIFO) buffer 402. An output terminal of the FIFO buffer 402 is coupled to a first data input terminal of a multiplexer 404. An output terminal of the multiplexer 404 is coupled to an input terminal of the mixer 30. The output terminal of the level detector 25 is coupled to a second data input terminal of the multiplexer 404. A timing output terminal of the encoder 10 is coupled to a control input terminal of the multiplexer 404.

In the illustrated embodiment, the auxiliary data signal is assumed to be in condition to directly modulate the carrier signal. One skilled in the art will understand how to encode and/or otherwise prepare a signal to modulate a carrier in a manner most appropriate to the characteristics of that signal. In addition, in the illustrated embodiment, the auxiliary data signal is assumed to be in digital form. This is not necessary, however. The auxiliary data signal may also be an analog signal.

In operation, the encoder 10 includes internal timing circuitry (not shown) which controls the relative timing of the pulses. This timing circuitry may be modified in a manner understood by one skilled in the art to generate a signal having a first state during the three adjacent encoding clock periods, t_1 - t_4 , when pulses may potentially occur in the CARR signal, and a second state during the remaining encoding clock periods, t_4 - t_{10} . This signal may be used to control the multiplexer 404 to couple the output terminal of the level detector 25 to the input terminal of the mixer 30 during the periods, t_1 - t_4 , when pulses may occur and to couple the output terminal of the FIFO buffer 402 to the mixer 30 otherwise, t_4 - t_{10} . During the periods, t_1 - t_4 , when the output terminal of the level detector 25 is coupled to the mixer 30, the circuit of Fig. 8 is in the configuration illustrated in Fig. 1, and operates as described above in detail.

During the periods ($t_4 + \Delta t$ to $t_{10} - \Delta t$) when the FIFO buffer 402 is coupled to the mixer 30 (taking into account the guard bands Δt), the data from the FIFO buffer 402 modulates the carrier signal from the oscillator 40. The FIFO buffer 402 operates to receive the digital auxiliary data signal at a constant
5 bit rate, and buffer the signal during the time periods ($t_1 - t_4$) when carrier pulses (A) - (C) may be produced. The FIFO buffer 402 then provides the stored auxiliary data to the mixer 30 as a burst at a higher bit rate during the time period ($t_4 + \Delta t$ to $t_{10} - \Delta t$) when the auxiliary data is to be transmitted. The net throughput of the bursts of auxiliary data through the CARR signal must match
10 the constant net throughput of auxiliary data from the auxiliary data signal source (not shown). One skilled in the art will understand how to match the throughputs, and also how to provide for overruns and underruns, all in a known manner.

Fig. 9 is a block diagram of a receiver which can receive the signal
15 produced by the system illustrated in Fig. 8. In Fig. 9, those elements which are the same as those illustrated in Fig. 3 are designated with the same reference number and are not described in detail below. In Fig. 9, the output terminal of the detector 140 is coupled to an input terminal of a controllable switch 406. A first output terminal of the controllable switch 406 is coupled to the input
20 terminal of the decoder 150. A second output terminal of the controllable switch 406 is coupled to an input terminal of a FIFO 408. An output terminal of the FIFO 408 produces the auxiliary data (AUX). The output terminal of the windowing timer 160 is coupled, not to an enable input terminal of the detector 140, as in Fig. 3, but instead to a control input terminal of the controllable
25 switch 406.

In operation, the detector 140 in Fig. 9 is always enabled. The windowing signal from the windowing timer 160 corresponds to the timing signal generated by the encoder 10 in Fig. 8. The windowing signal has a first state during the period (t_1 - t_4) when carrier pulses (A)-(C) could potentially occur, and a second
30 state otherwise (t_4 - t_{10}). During the period (t_1 - t_4) when carrier pulses (A)-(C) could potentially occur the windowing timer 160 conditions the controllable

switch 406 to couple the detector 140 to the decoder 150. This configuration is identical to that illustrated in Fig. 3, and operates as described above in detail.

During the remainder of the bit period (t_4 - t_{10}), the detector 140 is coupled to the FIFO 408. During this period, the modulated auxiliary data is demodulated and supplied to the FIFO 408. In a corresponding manner to the FIFO 402 (of Fig. 8), the FIFO 408 receives the auxiliary data bursts from the detector 140, and generates an auxiliary data output signal AUX at a constant bit rate. The auxiliary data signal represents the auxiliary data as encoded for modulating the carrier. Further processing (not shown) may be necessary to decode the received auxiliary data signal to the desired format.

In accordance with principles of the present invention, the auxiliary data inserted into the carrier signal is another set of carrier pulses representing a second, independent, high data rate signal. In some implementations, it may be possible to include more than one set of carrier pulses, representing more than one corresponding high data rate signals, as the auxiliary data. In the illustrated embodiment, two additional high data rate signals are included in the channel, for a total of three data signals.

In Fig. 10, each horizontal line illustrates the timing of carrier pulses representing a high data rate signal. The top line, labeled DATA 1 illustrates the timing of carrier pulses representing a first high data rate signal DATA 1, similar to Fig. 7. The second line in Fig. 10 illustrates the timing of the carrier pulses representing a second high data rate signal DATA 2, and the third line in Fig. 10 illustrates the timing of the carrier pulses representing a third high data rate signal DATA 3. As can be seen, the carrier pulse representing the first data signal DATA 1 is located in one of clock periods in the interval from time t_1 to t_4 , the carrier pulse representing the second data signal DATA 2 is located in one of the clock periods in the interval from time t_4 to t_7 , and the carrier pulse representing the third data signal DATA 3 is located in one of the clock periods in the interval from time t_7 to t_{10} . The carrier pulses from all the data signals DATA 1, DATA 2 and DATA 3 are combined into a single carrier signal CARR,

illustrated at the bottom of Fig. 10. This single carrier signal, thus, can transmit three independent high data rate signals through a single channel.

One skilled in the art will understand that each data signal represented as carrier pulses, as described in detail above, requires a time interval within the bit period containing three adjacent encoding clock periods. In the illustrated embodiment, there are nine encoding clock periods in each bit period, so up to three data signals may be carried simultaneously. More generally, $3 \times S$ encoding clock periods within a bit period are required to simultaneously encode S data signals. One skilled in the art will further understand that not every encoding clock period within a bit period need be utilized to encode data signals. For example, in the illustrated embodiment, two data signals could be simultaneously encoded. A first interval of three adjacent encoding clock periods is allocated to the first signal, and a second interval of three adjacent encoding clock periods, not overlapping those allocated to the first signal, is allocated to the second signal. The remaining three of the encoding clock periods remain unused, or are allocated to auxiliary data as illustrated in Fig. 7. One skilled in the art will further understand that the encoding clocks used to encode the respective data signals need not be the same, have the same period or be time aligned, so long as the time intervals when carrier pulses may occur representing the separate signals do not overlap.

Fig. 11, is a block diagram of a transmitter according to the present invention which can transmit three high data rate signals simultaneously over a single channel. Fig. 11 corresponds to Fig. 8. Elements which are similar to those illustrated in Fig. 8 are designated by corresponding reference numbers and are not described in detail below. In Fig. 11, respective input terminals, DATA 1, DATA 2, and DATA 3 are coupled to sources (not shown) of corresponding high data rate signals. The first input terminal DATA 1 is coupled to a first input terminal of a multiplexer 404' through the series connection of an encoder 10(1), a differentiator 20(1) and level detector 25(1). The second input terminal DATA 2 is coupled to a second input terminal of the multiplexer 404' through the series connection of an encoder 10(2), a differentiator 20(2) and level detector 25(2),

and the third input terminal DATA 3 is coupled to a third input terminal of the multiplexer 404' through the series connection of an encoder 10(3), a differentiator 20(3) and level detector 25(3). An output terminal of the multiplexer 404' is coupled to the input terminal of the mixer 30.

5 In operation, the encoder 10(1), a differentiator 20(1) and level detector 25(1) generate a tri-level signal, corresponding to signal LEVEL in Fig. 2 and described in detail above, representing the first high data rate signal DATA 1. Similarly, encoder 10(2), a differentiator 20(2) and level detector 25(2) generate a tri-level signal representing the second high data rate signal DATA 2, and
10 encoder 10(3), a differentiator 20(3) and level detector 25(3) generate a tri-level signal representing the third high data rate signal DATA 3. The timing of the pulses of the respective tri-level signals is controlled by a system timing circuit (not shown) to occur as illustrated in Fig. 10. One skilled in the art will understand how to design and implement such timing circuitry. The multiplexer
15 404' combines the tri-level pulses into a single tri-level signal having the timing illustrated in the bottom signal CARR of Fig. 10. This combined signal is then used to modulate the carrier signal from the oscillator 40 in the mixer 30. The resulting carrier signal is filtered in the BPF 50 to form the SSB signal, all as described above.

20 It is possible that the timing of the high data rate signals DATA 1, DATA 2 and DATA 3 are not synchronized, and/or including timing jitter with respect to each other. To compensate for these conditions, respective FIFO buffers, 27(1), 27(2), and 27(3), indicated in phantom in Fig. 11, are coupled between
25 respective level detectors (25(1), 25(2), 25(3)) and corresponding input terminals of the multiplexer 404'. The FIFO buffers, 27(1), 27(2), 27(3), operate to compensate for differences in data rate between the input signals DATA 1, DATA 2 and DATA 3 and the timing of the carrier signal CARR generated by the mixer 30, all in a known manner.

Fig. 12 is a block diagram of a receiver according to the present invention
30 capable of receiving the modulated signal produced by the transmitter of Fig. 11

and reproducing the three high data rate signals DATA 1, DATA 2 and DATA 3. Fig. 12 corresponds to Fig. 9. In Fig. 12, those elements similar to those illustrated in Fig. 9 are designated with the same reference number and are not described in more detail below. In Fig. 12, the output terminal of detector 140 is
5 coupled to an input terminal of a controllable switch 406'. A first output terminal of the controllable switch 406' is coupled to an input terminal of a first decoder 150(1). An output terminal of the first decoder 150(1) is coupled to an output terminal DATA 1. A second output terminal of the controllable switch 406' is coupled to an input terminal of a second decoder 150(2). An output
10 terminal of the second decoder 150(1) is coupled to an output terminal DATA 2, and a third output terminal of the controllable switch 406' is coupled to an input terminal of a third decoder 150(3). An output terminal of the third decoder 150(3) is coupled to an output terminal DATA 3.

In operation, the detector 140 generates a signal corresponding to the
15 composite tri-level signal (CARR of Fig. 10) generated by the multiplexer 404' (of Fig. 11). During the interval from time t1 to t4, the controllable switch 406' is conditioned to couple the detector 140 to the first decoder 150(1). During the interval from time t4 to t7, the controllable switch 406' is conditioned to couple the detector 140 to the second decoder 150(2), and during the interval from
20 time t7 to t10, the controllable switch 406' is conditioned to couple the detector 140 to the third decoder 150(3). A control circuit (not shown) generates a control signal for controlling the controllable switch 406' to operate as described above. One skilled in the art will understand how to design and implement such a control circuit.

25 The first decoder 150(1) receives the tri-level signal during the interval from time t1 to t4, corresponding to the DATA 1 signal in Fig. 10. The first decoder 150(1) processes this signal to regenerate the first NRZ signal DATA 1, in a known manner. Similarly, the second decoder 150(2) regenerates the second NRZ signal DATA 2 from the tri-level signal DATA 2 of Fig. 10, and the
30 third decoder 150(2) regenerates the third NRZ signal DATA 3 from the tri-level signal DATA 3 of Fig. 10.

21
CLAIMS

1. A digital data modulation method characterized by the steps of:
providing a plurality of digital data signals having a common data bit

5 period;

encoding respective ones of the plurality of digital data signals using a
variable pulse width code having edges occurring in respective non-overlapping
intervals within the data bit period;

generating respective pulses representing the edges of the corresponding
10 one of the encoded plurality of digital data signals; and

generating a carrier signal having carrier pulses corresponding to the
respective pulses.

2. A digital data modulator, characterized by:

15 a source of a plurality of digital data signals (Data 1, Data 2, Data 3)
having a common data bit period;

a plurality of encoders (10(1), 10(2), 10(3)), each encoding a
corresponding one of the plurality of digital data signals using a variable pulse
width code having edges occurring in respective non-overlapping intervals within
20 the data bit period;

a plurality of pulse signal generators (20(1), 25(1), 20(2), 25(2), 20(3),
25(3)), each generating respective pulses representing the edges of the
corresponding one of the encoded plurality of digital data signals;

a carrier signal generator (30, 40) for generating a carrier signal having
25 carrier pulses corresponding to the respective pulses.

3. The modulator of claim 2 characterized in that the variable pulse
width code is a variable aperture code.

30 4. The modulator of claim 3 characterized in that edges for each of the
digital data signals occur in one of three adjacent periods within the respective
interval.

5. The modulator of claim 3 characterized in that:

the data signal source (Data 1, Data 2, Data 3) produces a plurality of S digital data signals; and

5 the data bit period is divided into a plurality of at least $3 \cdot S$ encoding clock periods including S non-overlapping intervals of three adjacent encoding clock periods each; wherein

edges for each of the S digital data signals occur in a respective one of the S non-overlapping intervals.

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6. The modulator of claim 2 further characterized by a multiplexer (404') coupled between the plurality of pulse signal generators (20(1), 20(3), 25(1), 25(3)) and the carrier signal generator (30, 40) and conditioned to couple a selected one of the plurality of pulse signal generators to the carrier signal generator during the interval when the pluses from the selected pulse signal generator occur.

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7. The modulator of claim 6 further characterized by a plurality of first-in-first-out (FIFO) buffers (27(1), 27(3)) respectively coupled between the plurality of pulse signal generators and the multiplexer (404').

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8. The modulator of claim 2 characterized in that:

each one of the plurality of encoders (10(1), 10(2), 10(3)) generates an encoded digital data signal having leading edges and trailing edges;

25

each one of the plurality of pulse signal generators (20(1), 20(3), 25(1), 25(3)) generates positive pulses in response to leading edges in the corresponding digital data signal and negative pulses in response to trailing edges in the corresponding digital data signal; and

30

the carrier signal generator (30, 40) generates a carrier pulse having a first phase in response to a positive pulse and having a second phase in response to a negative pulse.

9. The modulator of claim 8 characterized in that the first phase is substantially 180 degrees out of phase with the second phase.

5 10. The modulator of claim 2 characterized in that each one of the plurality of pulse signal generators comprises:

a differentiator (20(1), 20(3)), coupled to the corresponding one of the plurality of encoders; and

a level detector (25(1), 25(2), 25(3)), coupled to the differentiator.

10 11. The modulator of claim 2 characterized in that the carrier signal generator comprises:

a carrier oscillator (40); and

15 a mixer (30), having a first input terminal coupled to the pulse signal generator and a second input terminal coupled to the carrier oscillator.

12. The modulator of claim 11 further characterized by a bandpass filter (50) coupled to an output terminal of the mixer (30).

20 13. A digital data demodulator, characterized by:

a source (IN) of a modulated signal including successive bit periods, each bit period having a plurality of non-overlapping intervals respectively associated with corresponding intervals in successive bit periods, each interval containing a carrier pulse, spaced relative to carrier pulses in other associated intervals,

25 representing a corresponding variable pulse width encoded digital data signal;

a detector (140) for demodulating the modulated signal to generate pulses corresponding to received carrier pulses; and

30 a plurality of decoders (150(1), 150(2), 150(3)), each decoding pulses received in a respective one of the plurality of associated intervals in the bit period to generate the corresponding digital data signal.

14. The demodulator of claim 13 further characterized by a controllable switch (406') having an input terminal coupled to the detector (140), and a plurality of output terminals coupled to corresponding ones of the plurality of decoders (150(1), 150(3)), and conditioned to couple the decoder (140) to a corresponding output terminal during a respective one of the plurality of associated intervals in the bit period.

15. The demodulator of claim 13 wherein the variable pulse width code is a variable aperture code.

16. The demodulator of claim 13 characterized in that the carrier pulses have one of a first phase and a second phase.

17. The demodulator of claim 13 characterized in that the first phase is substantially 180 degrees out of phase with the second phase.

18. The demodulator of claim 13 further characterized in that, coupled between the modulated signal source and the detector:

a bandpass filter (110);

an integrator (120); and

a limiting amplifier (130).

19. A digital data modulator, characterized by:

a source (Data 1) of a first digital data signal having a data bit period;

a first encoder (10(1)), for encoding the first digital data signal using a variable pulse width code having edges occurring in a first interval within the data bit period;

a first pulse signal generator (20(1), 25(1)), generating respective pulses representing the edges of the encoded first digital data signal;

a source of a second digital data signal (Data 2) having the data bit period;

a second encoder 10(2), for encoding the second digital data signal using a variable pulse width code having edges occurring in a second interval within the data bit period not overlapping the first interval;

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a second pulse signal generator (20(2), 25(2)), generating respective pulses representing the edges of the encoded second digital data signal;

a carrier signal generator(30, 40) for generating a carrier signal having carrier pulses corresponding to the respective first pulses during the first interval,
5 and having carrier pulses corresponding to the respective second pulses during the second interval.