A METHOD TO FORM LOW-OVERLAP-CAPACITANCE TRANSISTORS BY FORMING MICROTRENCH AT THE GATE EDGE

BACKGROUND OF THE INVENTION

(1) Field of the Invention

The invention relates to the fabrication of integrated circuit devices, and more particularly, to a method of spacing the source drain extensions from the gate edge to lower the gate to source drain extensions capacitance in the fabrication of integrated circuits.

(2) Description of the Prior Art

As the physical geometry of semiconductor devices shrinks, the channel length of the transistor is reduced as well. This leads to serious short channel effects. Lateral dopant diffusion from the source/drain extensions into the channel underlying the gate electrode will affect the threshold voltage and transistor current drive, thus affecting the device performance. Current practice involves spacing the source/drain extensions (SDE) from the gate edge using an offset spacer to lower the overlap capacitance between the gate and the SDE. However, it is desired to find a method to further lower the gate to SDE capacitance in situations where the offset spacer alone





is insufficient.

U.S. Patent 6,117,712 to Wu discloses a disposable spacer process for making raised source/drain devices. U.S. Patent 6,127,234 to Gardner et al shows a shallow extension process using disposable spacers. U.S. Patent 6,010,929 to Chapman teaches forming a nitride cap over the gate with extensions over the SDE region to space the source/drain regions from the gate.

SUMMARY OF THE INVENTION

A principal object of the present invention is to provide an effective and very manufacturable method of forming an integrated circuit device having low overlap capacitance transistors.

A further object of the invention is to provide a method of forming a transistor having low overlap capacitance by reducing effective dielectric constant value of the dielectric at the overlap between the gate and the source/drain extensions.

Yet another object is to provide a method of forming a transistor having low overlap capacitance by

forming a microtrench at the gate edge to reduce effective dielectric constant value of the dielectric at the overlap between the gate and the source/drain extensions.

In accordance with the objects of this invention a method for forming a transistor having low overlap capacitance by forming a microtrench at the gate edge to minimize lateral dopant diffusion is achieved. A gate electrode is provided overlying a gate dielectric layer on a semiconductor substrate wherein a hard mask layer overlies a top surface of the gate electrode layer. An oxide layer is formed overlying the semiconductor substrate. First spacers are formed on sidewalls of the gate electrode and overlying the oxide layer. Source/drain extensions are formed in the substrate using the first spacers as a mask. Second spacers are formed on the first spacers being comprised of a material different from the first spacers. Source/drain regions are formed in the substrate using the first and second spacers as a mask. A dielectric layer is deposited overlying the gate electrode and the oxide layer and planarized to the hard mask layer whereby the first and second spacers are exposed. The exposed second spacers are removed whereby the oxide layer underlying the second spacers is exposed. The exposed oxide layer is removed whereby the semiconductor substrate underlying the second spacers is

exposed. The exposed semiconductor substrate is etched into to form a microtrench wherein the microtrench undercuts the gate oxide layer at an edge of the gate electrode. The microtrench is filled with an epitaxial oxide layer and planarized to the hard mask layer. The dielectric layer is patterned to form third spacers on the epitaxial oxide layer. The effective dielectric constant at the overlap between the gate and the source/drain extensions is reduced by the microtrench thereby completing formation of a transistor having low overlap capacitance in the fabrication of an integrated circuit device.

BRIEF DESCRIPTION OF THE DRAWINGS

In the accompanying drawings forming a material part of this description, there is shown:

Figs. 1 through 11 schematically illustrate in cross-sectional representation a preferred embodiment of the present invention.

Fig. 12 schematically illustrates in cross-sectional representation a completed integrated circuit device fabricated according to the process of the present invention.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

It will be understood by those skilled in the art that while Figs. 1 through 11 illustrate an N channel MOSFET integrated circuit device, a P channel FET integrated circuit device could be formed simply by substituting opposite polarities to those given for the P channel embodiment. Also, in a similar way, a CMOSFET could be formed by making both N channel and P channel devices upon the same substrate. The process of the present invention will increase the effective thickness of the gate dielectric at the edge of the gate, both by thickening the dielectric and by using a lower dielectric constant material at the gate edge.

Referring now more particularly to Fig. 1, there is shown an illustration of a portion of a partially completed metal oxide field effect transistor (MOSFET). The semiconductor substrate 10 is preferably composed of silicon having a (100) crystallographic orientation.

In an effort to simplify the description and the drawings the dielectric isolation between devices has been only partially shown and will not be described in detail, because they are conventional. For example, Field

OXide regions FOX 11 can be formed in and on the semiconductor substrate.

A gate dielectric layer 14 is grown or deposited to a thickness of between about 12 and 65 Angstroms on the semiconductor substrate. This is an equivalent silicon dioxide thickness. The physical thickness will depend upon the dielectric constant (k) value of the gate dielectric material used. Preferably, the gate dielectric material will be a high dielectric constant material that will not be removed by a standard silicon dioxide etch process. The gate dielectric may be silicon nitride, for example.

A conductive layer 16, such as polysilicon, is deposited over the gate dielectric. A hard mask 18, such as silicon dioxide, is deposited to a thickness of between about 300 and 600 Angstroms. The hard mask, polysilicon, and gate oxide layers 18, 16, and 14 are patterned to form a gate electrode 20, as shown.

Now, referring to Fig. 2, the exposed substrate and polysilicon sidewalls are re-oxidized to form a very thin oxide layer 22, having a thickness of between about 10 and 20 Angstroms. For example, this is a dry rapid rapid

thermal oxidation (RTO).

First spacers 24 are formed on the sidewalls of gate electrode 20. The spacers may comprise silicon oxide or tetraethoxysilane (TEOS) oxide. The spacers are formed by depositing the dielectric layer overlying the substrate and the gate electrode and anisotropically etching back the dielectric layer to leave the spacers 24 on the sidewalls of the gate electrode. The spacers may have a width of between about 30 and 50 Angstroms. The re-oxidation oxide layer 22 is thinner than these spacers 24. Ions are implanted into the substrate to form source/drain extensions 28, as shown in Fig. 2. The gate electrode and the first spacers act as a mask for this implantation.

Referring now to Fig. 3, second spacers 26 are formed on the first spacers 24. The spacers 26 may comprise silicon nitride. The spacers are formed by depositing the dielectric layer overlying the substrate, the gate electrode, and the first spacers and anisotropically etching back the dielectric layer to leave the second spacers 26 on the first spacers 24 on the sidewalls of the gate electrode. The second spacers 26 may have a width of between about 60 and 100 Angstroms. Now, second ions are implanted into the substrate to form source and drain regions 30. The gate

electrode and the first and second spacers act as a mask for this implantation.

A thick oxide layer 32 is deposited over the substrate to a thickness of between about 1000 and 2000 Angstroms. This thick oxide layer may comprise plasma-enhanced TEOS oxide (PETEOS). The thick oxide layer is planarized such as by chemical mechanical polishing (CMP) down to the hard mask layer, thereby exposing the first and second spacers 24 and 26, as illustrated in Fig. 4.

The exposed second spacers 26 are removed using a wet etch, such as hot phosphoric acid, as shown in Fig. 5.

Next, referring to Fig. 6, the thin oxide layer 22 under the area previously occupied by the second spacers is removed by a short dip in hydrofluoric acid (HF).

Referring now to Fig. 7, a portion of the silicon substrate is removed by a dry etch underlying the openings left by the removal of the second spacers. A downstream plasma etcher or decoupled plasma system with no ion bombardment should be used. This is a timed etch using fluorine chemistry; for example, $SF_6 + O_2$, $CF_4 + O_2$, $NF_3 +$

O_2, $F_2 + O_2$, and so on, alone or in combination. The dry etching undercuts the gate dielectric at the gate edge by between about 50 and 100 Angstroms. The HF dip also undercuts the first spacers 24 by removing a portion of the thin oxide layer 22 underlying the first spacers, as shown. This undercutting forms a microtrench 34 at the gate edge. The microtrench has a depth into the semiconductor substrate of between about 50 and 80 Angstroms.

Referring now to Fig. 8, the microtrenches 34 and the openings formerly occupied by the second spacers are filled with liquid phase epitaxy oxide 36. For example, the wafers are immersed in a hydrofluorosilicic acid (H_2SiF_6) solution supersaturated with silicic acid at room temperature. The supersaturation is achieved by adding boric acid. The oxide layer 36 is planarized to the hard mask layer, such as by CMP.

A photoresist mask 40, for example, is formed over the gate electrode and thick oxide layer 30, as shown in Fig. 9. The thick oxide layer 30 is patterned to form third spacers 42 on the oxide spacers 36. This is illustrated in Fig. 10.

Now, the gate and source/drain regions are to be silicided. The hard mask 18 is removed over the gate electrode 20. Referring now to Fig. 11, the gate 20 and source/drain regions 30 are silicided 54 by any of the conventional methods. For example, a metal layer such as titanium or cobalt may be deposited over the substrate and the gate electrode. The wafer is subjected to an annealing process. The metal layer overlying the polysilicon gate electrode and overlying the silicon substrate in the source and drain regions 30 is transformed to a metal silicide 54. The metal overlying the spacers 41 and 36 and FOX regions 11 is unreacted. The unreacted metal is removed to complete the silicidation process.

This completes the formation of the transistor with associated source/drain regions and source/drain extensions. The integrated circuit device is completed as is conventional in the art. For example, as illustrated in Fig. 12, insulating layer 60 is deposited over the surface of the substrate. Contact openings are made through the insulating layer to the underlying semiconductor devices, such as to silicided source region 30. A metal layer 62 is deposited and patterned to form electrical connections between the elements of the integrated circuit. A passivation layer 64 completes the fabrication of the integrated circuit.

The process of the invention provides a low overlap capacitance transistor. Because of the microtrench formed at the gate edge, the effective k-value of the dielectric at the overlap between the SDE and the gate is reduced. The dielectric thickness at the overlap also is increased physically. The minimal overlap between the SDE and the gate is between about 100 and 150 Angstroms.

While the invention has been particularly shown and described with reference to the preferred embodiments thereof, it will be understood by those skilled in the art that various changes in form and details may be made without departing from the spirit and scope of the invention.

What is claimed is:

1. A method of forming a transistor with associated source and drain regions in the fabrication of an integrated circuit device comprising:

providing a gate electrode overlying a gate dielectric layer on a substrate wherein a hard mask layer overlies a top surface of said gate dielectric layer;

forming an oxide layer overlying said substrate and sidewalls of said gate;

forming first spacers on sidewalls of said gate electrode and overlying said oxide layer;

forming source/drain extensions in said substrate using said first spacers as a mask;

forming second spacers on said first spacers;

forming source and drain regions in said substrate using said first and second spacers as a mask;

depositing a dielectric layer overlying said gate electrode and said oxide layer and planarizing said dielectric layer to said hard mask layer whereby said first spacers and said second spacers are exposed;

removing exposed said second spacers whereby said oxide layer underlying said second spacers is exposed;

removing exposed said oxide layer whereby said semiconductor substrate underlying said second spacers is exposed;

etching into exposed said semiconductor substrate to form a microtrench wherein said microtrench undercuts said gate oxide layer at an edge of said gate electrode;

filling said microtrench with an epitaxial oxide layer and planarizing said epitaxial oxide layer to said hard mask layer; and

thereafter patterning said dielectric layer to form third spacers on said epitaxial oxide layer to complete formation of said transistor and associated source and drain regions in said fabrication of said integrated circuit device.

2. The method according to Claim 1 wherein said gate dielectric layer comprises a material not removed by a silicon dioxide etch process.

3. The method according to Claim 1 wherein said oxide layer is formed by re-oxidizing said substrate and said gate to form said oxide layer having a thickness of between about 10 and 20 Angstroms.

4. The method according to Claim 1 wherein said first oxide spacers comprise silicon dioxide or tetraethoxysilane (TEOS) oxide, and have a width of between about 30 and 50 Angstroms.

5. The method according to Claim 1 wherein said oxide layer has a thickness smaller than a width of said first spacers.

6. The method according to Claim 1 wherein said second spacers comprise silicon nitride and have a width of between about 60 and 100 Angstroms.

7. The method according to Claim 1 wherein said dielectric layer comprises TEOS oxide deposited by plasma-enhanced chemical vapor deposition (PETEOS).

8. The method according to Claim 1 wherein said step of removing said second spacers uses a wet etch.

9. The method according to Claim 1 wherein said step of etching into exposed said semiconductor substrate to form a microtrench comprises a dry etch with no ion bombardment and wherein said microtrench has a depth into said semiconductor substrate of between about 50 and 80 Angstroms and wherein said microtrench undercuts said gate oxide layer at said gate edge by between about 50 and 100 Angstroms.

10. The method according to Claim 1 wherein said step of filling said microtrench with an epitaxial oxide layer is a liquid phase epitaxy process comprising immersing said substrate in a hydrofluorosilicic acid solution supersaturated with silicic acid at room temperature.

11. The method according to Claim 1 further comprising siliciding said gate electrode and said source and drain regions.

12. A method of forming a transistor with associated source and drain regions in the fabrication of an integrated circuit device comprising:

providing a gate electrode overlying a gate dielectric layer on a substrate wherein a hard mask layer overlies a top surface of said gate dielectric layer;

forming a first oxide layer overlying said substrate and sidewalls of said gate;

forming oxide spacers on sidewalls of said gate electrode and overlying said first oxide layer;

forming source/drain extensions in said substrate using said oxide spacers as a mask;

forming nitride spacers on said oxide spacers;

forming source and drain regions in said substrate

using said oxide and said nitride spacers as a mask;

depositing a second oxide layer overlying said gate electrode and said first oxide layer and planarizing said second oxide layer to said hard mask layer whereby said oxide spacers and said nitride spacers are exposed;

removing exposed said nitride spacers whereby said first oxide layer underlying said nitride spacers is exposed;

removing exposed said first oxide layer whereby said substrate underlying said nitride spacers is exposed;

etching into exposed said substrate to form a microtrench wherein said microtrench undercuts said gate oxide layer at an edge of said gate electrode;

filling said microtrench with an epitaxial oxide layer and planarizing said epitaxial oxide layer to said hard mask layer; and

thereafter patterning said second oxide layer to form third spacers on said epitaxial oxide layer to complete formation of said transistor and associated source and drain regions in said fabrication of said integrated circuit device.

13. The method according to Claim 12 wherein said first oxide layer is formed by re-oxidizing said substrate

and said gate to form said first oxide layer having a thickness of between about 10 and 20 Angstroms.

14. The method according to Claim 12 wherein said oxide spacers comprise silicon oxide or TEOS oxide and have a width of between about 30 and 50 Angstroms.

15. The method according to Claim 12 wherein said first oxide layer has a thickness smaller than a width of said oxide spacers.

16. The method according to Claim 12 wherein said nitride spacers comprise silicon nitride and have a width of between about 60 and 100 Angstroms.

17. The method according to Claim 12 wherein said second oxide layer comprises PETEOS oxide.

18. The method according to Claim 12 wherein said step of removing said nitride spacers uses a wet etch in hot phosphoric acid.

19. The method according to Claim 12 wherein said step of etching into exposed said semiconductor substrate to form a microtrench comprises a dry etch with no ion

bombardment and wherein said microtrench has a depth into said substrate of between about 50 and 80 Angstroms and wherein said microtrench undercuts said gate oxide layer at said gate edge by between about 50 and 100 Angstroms.

20. The method according to Claim 12 wherein said step of filling said microtrench with an epitaxial oxide layer is a liquid phase epitaxy process comprising immersing said substrate in a hydrofluorosilicic acid solution supersaturated with silicic acid at room temperature.

21. The method according to Claim 12 further comprising siliciding said gate electrode and said source and drain regions.

22. A method of forming a transistor with associated source and drain regions in the fabrication of an integrated circuit device comprising:

providing a gate electrode overlying a gate dielectric layer on a substrate wherein a hard mask layer overlies a top surface of said gate dielectric layer;

re-oxidizing said substrate and said gate to

form a first oxide layer overlying said substrate and sidewalls of said gate;

forming oxide spacers on sidewalls of said gate electrode and overlying said first oxide layer;

forming source/drain extensions in said substrate using said oxide spacers as a mask;

forming nitride spacers on said oxide spacers;

forming source and drain regions in said substrate using said oxide and said nitride spacers as a mask;

depositing a second oxide layer overlying said gate electrode and said first oxide layer and planarizing said second oxide layer to said hard mask layer whereby said oxide spacers and said nitride spacers are exposed;

removing exposed said nitride spacers whereby said first oxide layer underlying said nitride spacers is exposed;

removing exposed said first oxide layer whereby said substrate underlying said nitride spacers is exposed;

etching into exposed said substrate to form a microtrench wherein said microtrench undercuts said gate oxide layer at an edge of said gate electrode;

immersing said substrate in a hydrofluorosilicic acid solution supersaturated with silicic acid at room temperature whereby said microtrench is filled with an

epitaxial oxide layer and planarizing said epitaxial oxide layer to said hard mask layer; and

thereafter patterning said second oxide layer to form third spacers on said epitaxial oxide layer to complete formation of said transistor and associated source and drain regions in said fabrication of said integrated circuit device.

23. The method according to Claim 22 wherein said oxide spacers comprise silicon oxide or TEOS oxide and have a width of between about 30 and 50 Angstroms.

24. The method according to Claim 22 wherein said nitride spacers comprise silicon nitride and have a width of between about 60 and 100 Angstroms.

25. The method according to Claim 22 wherein said step of removing said nitride spacers uses a wet etch in hot phosphoric acid.

26. The method according to Claim 22 wherein said step of etching into exposed said semiconductor substrate to form a microtrench comprises a dry etch with no ion bombardment and wherein said microtrench has a depth into said substrate of between about 50 and 80 Angstroms

and wherein said microtrench undercuts said gate oxide layer at said gate edge by between about 50 and 100 Angstroms.

27. The method according to Claim 22 further comprising siliciding said gate electrode and said source and drain regions.