(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
28 June 2012 (28.06.2012)

WIPO | PCT

(10) International Publication Number
WO 2012/088097 A2

(51) International Patent Classification:
H01L 29/78 (2006.01) *H01L 21/336* (2006.01)

(21) International Application Number:
PCT/US2011/066129

(22) International Filing Date:
20 December 2011 (20.12.2011)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
12/975,278 21 December 2010 (21.12.2010) US

(71) Applicant *(for all designated States except US)*: **INTEL CORPORATION** [US/US]; 2200 Mission College Boulevard, MS: RNB-4-150, Santa Clara, California 95052 (US).

(72) Inventors; and

(75) Inventors/Applicants *(for US only)*: **GLASS, Glenn A.** [US/US]; 6220 SW Madhatter Ln., Beaverton, Oregon 97008 (US). **MURTHY, Anand S.** [US/US]; 10934 NW Lucerne Ct., Portland, Oregon 97229 (US).

(74) Agent: **MALONEY, Neil F.**; Finch & Maloney PLLC, c/o CPA Global, P.O. Box 52050, Minneapolis, Minnesota 55402 (US).

(81) Designated States *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IS, JP, KE, KG, KM, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LT, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) Designated States *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, GH,

[Continued on next page]

(54) Title: COLUMN IV TRANSISTORS FOR PMOS INTEGRATION

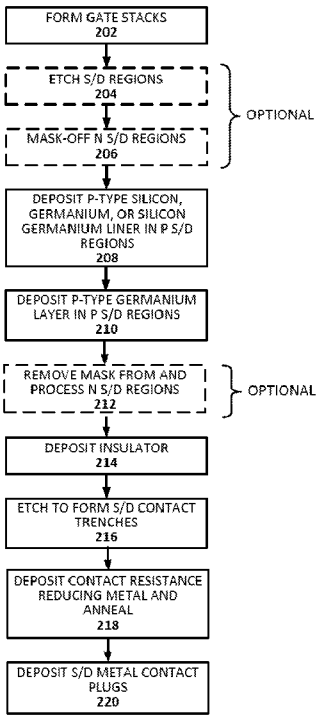


FIG. 2

(57) Abstract: Techniques are disclosed for forming column IV transistor devices having source/drain regions with high concentrations of germanium, and exhibit reduced parasitic resistance relative to conventional devices. In some example embodiments, the source/drain regions each includes a thin p-type silicon or germanium or SiGe deposition with the remainder of the source/drain material deposition being p-type germanium or a germanium alloy (e.g., germanium:tin or other suitable strain inducer, and having a germanium content of at least 80 atomic % and 20 atomic % or less other components). In some cases, evidence of strain relaxation may be observed in the germanium rich cap layer, including misfit dislocations and/or threading dislocations and/or twins. Numerous transistor configurations can be used, including both planar and non-planar transistor structures (e.g., FinFETs and nanowire transistors), as well as strained and unstrained channel structures.

WO 2012/088097 A2

GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Published:

— *without international search report and to be republished upon receipt of that report (Rule 48.2(g))*