

TRANSMISSION CIRCUIT, INTERFACE CIRCUIT AND MEMORY

ABSTRACT

Provided are a transmission circuit, an interface circuit and a memory. The transmission circuit comprises: an upper-layer clock pad (101), which is used for transmitting a clock signal; M upper-layer data pads (102), which are used for transmitting data signals; a lower-layer clock pad (111), which is electrically connected to the upper-layer clock pad (101), wherein the area of the lower-layer clock pad (111) is less than that of the upper-layer clock pad (101); and M lower-layer data pads (112), which are electrically connected in one-to-one correspondence to the M upper-layer data pads (102), wherein the area of each lower-layer data pad (112) is less than that of each upper-layer data pad (102); the upper-layer clock pad (101) and the upper-layer data pads (102) are located in a first layer, the lower-layer clock pad (111) and the lower-layer data pads (112) are located in a second layer; a dielectric layer is arranged between the first layer and the second layer; and the first layer, the dielectric layer and the second layer are all located on the same substrate.

[Fig. 6]