CLAIMS

1. A layout method of an integrated circuit, wherein the integrated circuit comprises multiple standard cells (10), each of the standard cells (10) comprises a polysilicon gate (11) and virtual polysilicon gates (12), at least two of the multiple standard cells (10) have different gate lengths (X), the gate length (X) of the standard cell (10) is a width of the polysilicon gate (11) of the standard cell (10), and the method comprises:

determining (S301) the standard cell (10) having a maximum gate length (X) in the multiple standard cells (10) as a first standard cell;

determining (S302) a first pitch (P) of the first standard cell, wherein the first pitch (P) is a distance between a central axis of the polysilicon gate (21) in the first standard cell and central axes of the virtual polysilicon gates (22) in the first standard cell; and

adjusting (S303) distances between the polysilicon gate (11) and the virtual polysilicon gates (12) in each of the standard cells (10) based on the first pitch (P) and the gate length (X) of each of the standard cells (10), wherein after the adjustment, distances between a central axis of the polysilicon gate (11) and central axes of the virtual polysilicon gates (12) in each of the standard cells (10) are the same as the first pitch (P);

wherein each of the standard cells (10) further comprises contact structures (13) and active regions (14), the contact structures (13) are located between the polysilicon gate (11) and each of the virtual polysilicon gates (12) in each of the standard cells (10) and located in the active regions (14), and the active regions (14) are located between two virtual polysilicon gates (12) in each of the standard cells (10); and

the determining (S302) a first pitch (P) of the first standard cell comprises:

determining the first pitch (P) based on the gate length (K1) of the first standard cell, a spacing distance (K2) between the contact structures (23) and the polysilicon gate (21) in the first standard cell, a width (K3) of the contact structures (23) in the first standard cell, a distance (K4) from one of the contact structures (23) to a boundary of one of the active regions (24) in the first standard cell, a spacing distance (K5) between the virtual polysilicon gates (22) and the active regions (24) in the first standard cell, and a width (K6) of the virtual polysilicon gates (22) in the first

standard cell;

wherein the determining the first pitch (P) based on the gate length (K_1) of the first standard cell, a spacing (K_2) distance between the contact structures (23) and the polysilicon gate (21) in the first standard cell, a width (K_3) of the contact structures (23) in the first standard cell, a distance (K_4) from one of the contact structures (23) to a boundary of one of the active regions (24) in the first standard cell, a spacing (K_5) distance between the virtual polysilicon gates (22) and the active regions (24) in the first standard cell, and a width (K_6) of the virtual polysilicon gates (22) in the first standard cell comprises:

determining the first pitch (P) in the following manner:

$$P = \frac{1}{2}K_1 + K_2 + K_3 + K_4 + K_5 + \frac{1}{2}K_6;$$

wherein the P represents the first pitch, the K_1 represents the gate length of the first standard cell, the K_2 represents the spacing distance between the contact structures (23) and the polysilicon gate (21) in the first standard cell, the K_3 represents the width of the contact structures (23) in the first standard cell, the K_4 represents the distance from one of the contact structures (23) to the boundary of one of the active regions (24) in the first standard cell, the K_5 represents the spacing distance between the virtual polysilicon gates (22) and the active regions (24) in the first standard cell, and the K_6 represents the width of the virtual polysilicon gates (22) in the first standard cell.

2. The method according to claim 1, wherein each of the standard cells (10) further comprises contact structures and active regions (14), the contact structures (13) are located between the polysilicon gate (11) and each of the virtual polysilicon gates (12) in each of the standard cells (10) and located in the active regions (14), and the active regions (14) are located between two virtual polysilicon gates (12) in each of the standard cells (10); and

the adjusting (S303) distances between the polysilicon gate (11) and the virtual polysilicon gates (12) in each of the standard cells (10) based on the first pitch (P) and the gate length (X) of each of the standard cells (10) comprises:

determining a first spacing distance (Y) between the contact structures (13) and the polysilicon gate (11) in each of the standard cells (10) and a second spacing distance (Z) between the virtual polysilicon gates (12) and the active regions (14) in

each of the standard cells (10) based on the first pitch (P) and the gate length (X) of each of the standard cells (10); and

adjusting a spacing distance between the contact structures (13) and the polysilicon gate (11) in each of the standard cells (10) to be the first spacing distance (Y) corresponding to each of the standard cells (10); and adjusting a spacing distance between the virtual polysilicon gates (12) and the active regions (14) in each of the standard cells (10) to be the second spacing distance (Z) corresponding to each of the standard cells (10).

3. The method according to claim 2, wherein the determining a first spacing distance (Y) between the contact structures (13) and the polysilicon gate (11) in each of the standard cells (10) and a second spacing distance (Z) between the virtual polysilicon gates (12) and the active regions (14) in each of the standard cells (10) based on the first pitch (P) and the gate length (X) of each of the standard cells (10) comprises:

determining the first spacing distance (Y) between the contact structures (13) and the polysilicon gate (11) in each of the standard cells (10) based on the first pitch (P), the gate length (X) of each of the standard cells (10), and a width (B) of the contact structures (13); and

determining the second spacing distance (Z) between the virtual polysilicon gates (12) and the active regions (14) in each of the standard cells (10) based on the first pitch (P), the gate length (X), the width (B) of the contact structures (13), and a distance (C) from one of the contact structures (13) to a boundary of one of the active regions (14) in each of the standard cells (10).

4. The method according to claim 3, wherein the determining the first spacing distance (Y) between the contact structures (13) and the polysilicon gate (11) in each of the standard cells (10) based on the first pitch (P), the gate length (X) of each of the standard cells (10), and a width (B) of the contact structures (13) comprises:

calculating a first spacing distance Y_i between the contact structures (13) and the polysilicon gate (11) in an i^{th} standard cell (10) in the following manner:

$$Y_i = \frac{1}{2}P - \frac{1}{2}X_i - \frac{1}{2}B_i$$

wherein the P represents the first pitch, the X_i represents the gate length (X) of the i^{th} standard cell (10), and the B_i represents the width (B) of the contact structures (13) of the i^{th} standard cell (10).

5. The method according to claim 3, wherein the determining the second spacing distance (Z) between the virtual polysilicon gates (12) and the active regions (14) in each of the standard cells (10) based on the first pitch (P), the gate length (X), the width (B) of the contact structures (13), and a distance (C) from one of the contact structures to a boundary of one of the active regions (14) in each of the standard cells (10) comprises:

calculating a second spacing distance Z_i between the virtual polysilicon gates (12) and the active regions (14) in an i^{th} standard cell (10) in the following manner:

$$Z_i = \frac{1}{2}P - \frac{1}{2}X_i - \frac{1}{2}B_i - C_i$$

wherein the P represents the first pitch, the X_i represents the gate length (X) of the i^{th} standard cell (10), the B_i represents the width (B) of the contact structures (13) in the i^{th} standard cell (10), and the C_i represents the distance (C) from one of the contact structures (13) to the boundary of one of the active regions (14) in the i^{th} standard cell (10).

6. The method according to claim 1, wherein after the adjusting (S303) distances between the polysilicon gate (11) and the virtual polysilicon gates (12) in each of the standard cells (10) based on the first pitch (P) and the gate length (X) of each of the standard cells (10), the method further comprises:

when the gate length (X) of a target standard cell in the standard cells (10) changes, updating the first spacing distance (Y) between the contact structures (13) and the polysilicon gate (11) in the target standard cell and updating the second spacing distance (Z) between the virtual polysilicon gates (12) and the active regions (14) in the target standard cell based on the changed gate length; and

adjusting a spacing distance between the contact structures (13) and the polysilicon gate (11) in the target standard cell to be the updated first spacing distance in the target standard cell, and adjusting a spacing distance between the virtual polysilicon gates (12) and the active regions (14) in the target standard cell to be the updated second spacing distance in the target standard cell.

7. An integrated circuit, comprising multiple standard cells (10), wherein each of the standard cells (10) comprises a polysilicon gate (11) and virtual polysilicon gates (12), at least two of the multiple standard cells (10) have different gate lengths (X), and the gate length (X) of the standard cell (10) is a width of the polysilicon gate (11) of the standard cell (10); and

each of the standard cells (10) has a same target pitch and the target pitch is a first pitch (P), the target pitch is a distance between a central axis of the polysilicon gate (11) in each of the standard cells (10) and central axes of the virtual polysilicon gates (12) in each of the standard cells (10), the first pitch (P) is determined based on the distance between the central axis of the polysilicon gate (21) in a first standard cell and the central axes of the virtual polysilicon gates (22) in the first standard cell, and the first standard cell is the standard cell (10) having a maximum gate length (X) in the multiple standard cells (10);

wherein each of the standard cells (10) further comprises contact structures (13) and active regions (14), the contact structures (13) are located between the polysilicon gate (11) and each of the virtual polysilicon gates (12) in each of the standard cells (10) and located in the active regions (14), and the active regions (14) are located between two virtual polysilicon gates (12) in each of the standard cells (10); and

the first pitch (P) is determined based on the gate length (K_1) of the first standard cell, a spacing distance (K_2) between the contact structures (23) and the polysilicon gate (21) in the first standard cell, a width (K_3) of the contact structures (23) in the first standard cell, a distance (K_4) from one of the contact structures (23) to a boundary of one of the active regions (24) in the first standard cell, a spacing distance (K_5) between the virtual polysilicon gates (22) and the active regions (24) in the first standard cell, and a width (K_6) of the virtual polysilicon gates (22) in the first standard cell;

wherein the first pitch (P) is determined in the following manner:

$$P = \frac{1}{2}K_1 + K_2 + K_3 + K_4 + K_5 + \frac{1}{2}K_6;$$

wherein the P represents the first pitch, the K_1 represents the gate length of the first standard cell, the K_2 represents the spacing distance between the contact structures (23) and the polysilicon gate (21) in the first standard cell, the K_3 represents the width of the contact structures (23) in the first standard cell, the K_4 represents the distance from one of the contact structures (23) to the boundary of one of the active regions (24) in the first standard cell, the K_5 represents the spacing distance between the virtual polysilicon gates (22) and the active regions (24) in the first standard cell, and the K_6 represents the width of the virtual polysilicon gates (22) in the first standard cell.

8. The integrated circuit according to claim7, wherein each of the standard cells (10) further comprises contact structures (13) and active regions (14), the contact structures (13) are located between the polysilicon gate (11) and each of the virtual polysilicon gates (12) in each of the standard cells (10) and located in the active regions (14), and the active regions (14) are located between two virtual polysilicon gates (12) in each of the standard cells (10); and

a first spacing distance (Y) between the contact structures (13) and the polysilicon gate (11) in each of the standard cells (10) and a second spacing distance (Z) between the virtual polysilicon gates (12) and the active regions (14) in each of the standard cells (10) are both determined based on the first pitch (P) and the gate length (X) of each of the standard cells (10).

9. The integrated circuit according to claim 8, wherein the first spacing distance (Y) between the contact structures (13) and the polysilicon gate (11) in each of the standard cells (10) is determined based on the first pitch (P), the gate length (X) of each of the standard cells (10), and a width(B) of the contact structures (13); and

the second spacing distance (Z) between the virtual polysilicon gates (12) and the active regions (14) in each of the standard cells (10) is determined based on the first pitch (P), the gate length (X), the width (B) of the contact structures (13), and a distance from one of the contact structures (13) to a boundary (C) of one of the active regions (14) in each of the standard cells (10).

10. The integrated circuit according to claim9, wherein a first spacing distance Y_i between the contact structures (13) and the polysilicon gate (11) in an i^{th} standard cell (10) is determined in the following manner:

$$Y_i = \frac{1}{2}P - \frac{1}{2}X_i - \frac{1}{2}B_i$$

wherein the P represents the first pitch, the X_i represents the gate length (X) of the i^{th} standard cell (10), and the B_i represents the width (B) of the contact structures (13) of the i^{th} standard cell (10).

11. The integrated circuit according to claim 9, wherein a second spacing distance Z_i between the virtual polysilicon gates (12) and the active regions (14) in an i^{th} standard cell (10) is determined in the following manner:

$$Z_i = \frac{1}{2}P - \frac{1}{2}X_i - \frac{1}{2}B_i - C_i$$

wherein the P represents the first pitch, the X_i represents the gate length (X) of

the i^{th} standard cell (10), the B_i represents the width (B) of the contact structures (13) in the i^{th} standard cell (10), and the C_i represents the distance from one of the contact structures (13) to the boundary (C) of one of the active regions (14) in the i^{th} standard cell (10).