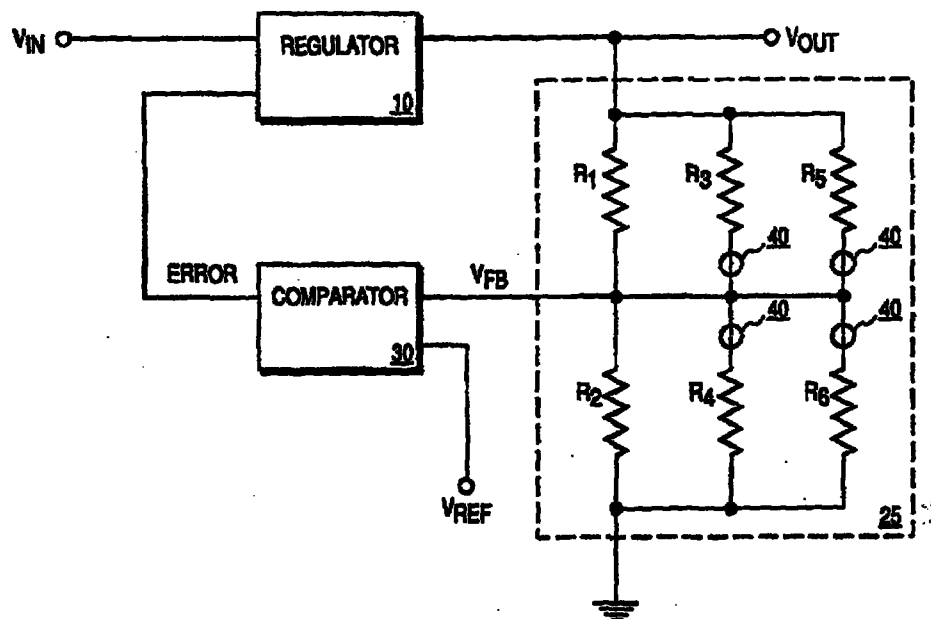


**PCT**WORLD INTELLECTUAL PROPERTY ORGANIZATION
International Bureau

INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(51) International Patent Classification ⁶ : G05F 1/40, 1/44, 1/56, 1/618, 1/569, 1/571, A61C 13/235, H01H 85/02, 85/14, 85/143, 85/165, H01R 9/09		A1	(11) International Publication Number: WO 96/35155
			(43) International Publication Date: 7 November 1996 (07.11.96)
(21) International Application Number: PCT/US96/05749		(81) Designated States: AL, AM, AT, AT (Utility model), AU, AZ, BB, BG, BR, BY, CA, CH, CN, CZ, CZ (Utility model), DE, DE (Utility model), DK, DK (Utility model), EE, EE (Utility model), ES, FI, FI (Utility model), GB, GE, HU, IS, JP, KE, KG, KP, KR, KZ, LK, LR, LS, LT, LU, LV, MD, MG, MK, MN, MW, MX, NO, NZ, PL, PT, RO, RU, SD, SE, SG, SI, SK, SK (Utility model), TJ, TM, TR, TT, UA, UG, UZ, VN, ARIPO patent (KE, LS, MW, SD, SZ, UG), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, CH, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, ML, MR, NE, SN, TD, TG).	
(22) International Filing Date: 25 April 1996 (25.04.96)			
(30) Priority Data: 08/434,521 4 May 1995 (04.05.95) US			
(71) Applicant: INTEL CORPORATION [US/US]; 2200 Mission College Boulevard, Santa Clara, CA 95052 (US).			
(72) Inventor: LANDOLF, David; 272 Pacific Grove, Beaverton, OR 97006 (US).			
(74) Agents: SALTER, James, H. et al.; Blakely, Sokoloff, Taylor & Zafman, 7th floor, 12400 Wilshire Boulevard, Los Angeles, CA 90025-1026 (US).		Published With international search report.	

(54) Title: PRINTED CIRCUIT BOARD WITH SELECTABLE ROUTING CONFIGURATION



(57) Abstract

A printed circuit board (60) having a selectable circuit routing configuration comprises a substrate (62), a plurality of electrical traces (42 and 44) mounted to the substrate for interconnecting electrical components, and at least one fusible connector (40) mounted to the substrate. Each of the fusible connectors has a fuse line (50) formed from a conductive layer of the printed circuit board and forms a fusible connection between at least two of the electrical traces. The circuit routing configuration can be selected by application of a predetermined current through at least one of the fusible connectors to break the fusible connection formed by the fusible connector.