

PROCESS FOR PRODUCING A SEMICONDUCTOR DEVICE

The present invention relates to a process for producing a semiconductor device.

PNP transistors are essential in current technology and play an important role in bipolar circuits. However, PNP transistors exhibit performance characteristics such as current amplification factor h_{fe} and gain-bandwidth product f_T which are considerably inferior to those of NPN transistors. For instance, the gain-bandwidth product f_T of an NPN transistor may be about 100 MHz. With a PNP transistor, however, the gain-bandwidth product f_T is, at best, several MHz.

The poor performance of a PNP transistor can be attributed to the following:

- (1) A PNP transistor is usually constructed in a lateral configuration in which p-type layers are arranged in the lateral direction, and using an epitaxial n-type layer, as disclosed in e.g. "Integrated Circuit Engineering (1)" published by Corona Publishing Co., 1979, pp. 165-168. With this structure, most of the holes injected through the emitter are stored in the epitaxial layer, and only a small proportion of the holes arrive at the collector.
- (2) The base width W_B , which is an important parameter in determining transistor performance, varies in dependence upon the precision of processing of the photomask and the photoresist and in dependence upon the diffusion

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conditions of the emitter and collector. It is therefore difficult to control the base width W_B , and in particular it is difficult to reduce greatly the base width.

(3) The distribution of impurity concentration varies in
5 the epitaxial layer that acts as the base of the transistor.

In view of the above-mentioned defects, the inventors have sought a PNP transistor with a vertical structure in an effort to enhance the performance of such a transistor.

10 The inventors have also found that the number of manufacturing steps increases considerably if it is attempted to form an NPN transistor and a vertical PNP transistor in the same semiconductor substrate, with a subsequent increase in manufacturing costs.

15 The present invention therefore provides a process for producing a bipolar semiconductor device, comprising:

selectively introducing impurities of a first conductivity type into a semiconductor substrate, to form first and second semiconductor regions separated from each
20 other;

introducing impurities of the first conductivity type into the first semiconductor region, to give the first semiconductor region a high impurity concentration, and simultaneously introducing impurities of the first
25 conductivity type selectively into a part of the second semiconductor region, to form a third semiconductor region having a high impurity concentration;

selectively depositing a semiconductor layer on a

surface of the substrate, thereby to cover the first, second and third semiconductor regions;

introducing impurities of the first conductivity type into the part of the semiconductor layer covering the third semiconductor region, thereby to form a fourth semiconductor region extending from the surface of the semiconductor layer to the third semiconductor region; and

forming a rectifying junction in the semiconductor layer overlying the second semiconductor region.

The rectifying junction may then form the base and collector of the vertical transistor, the second semiconductor region the emitter and the third and fourth regions provide contact to the emitter.

One way of forming the rectifying junction is by:

selectively introducing impurities of the second conductivity type into the semiconductor layer, to form a fifth semiconductor region which extends from the surface of the semiconductor layer to the second semiconductor region; and

introducing impurities of the first conductivity type into a part of the fifth semiconductor region, to form a sixth semiconductor region in the fifth semiconductor region. The fifth semiconductor layer then forms the base and the fifth semiconductor the collector.

Alternatively the rectifying junction may be formed by an electrode in contact with the semiconductor layer over the second semiconductor region, the electrode being treated to form a Schottky contact, which forms the rectifying junction.

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The present invention may make possible the formation of an NPN transistor and a vertical PNP transistor of high performance in the same semiconductor substrate without causing manufacture to become complex.

- 5 In one way of achieving the present invention an n-type silicon layer is formed on the surface of a silicon semiconductor substrate, the n-type silicon layer being electrically isolated therefrom by an isoplanar oxide film, thereby to form vertical PNP transistors in the n-type
- 10 silicon layer. The following steps may be utilized.
- (1) In order to form a part of the collector region of PNP transistor, a p-type buried layer (the second semiconductor region of the present invention) is formed in the bottom of the n-type silicon layer by
- 15 introducing p-type impurities, which may also form a channel stopper (the first semiconductor region of the present invention) just under the isoplanar oxide film.
- (2) P-type impurities are introduced into parts of the channel stopper region and the p-type buried
- 20 layer, to increase the impurity concentration in the channel stopper region, and to form a high concentration p⁺-type region (the third semiconductor region of the present invention) in a part of the p-type buried layer.
- 25 (3) A base width control layer (often called n-well) of the PNP transistor is created by forming a collector electrode take-out layer of the NPN transistor.

(4) An emitter region and a collector electrode take-out layer of the PNP transistor are created by forming a base region of the NPN transistor.

(5) A base electrode take-out layer of the PNP transistor is created by forming an emitter region of the NPN transistor.

As described above, the present invention may allow the vertical PNP transistor to be formed without increasing the number of steps for manufacturing high performance NPN transistors.

Moreover, the PNP transistor base width may be determined accurately, making it possible to increase the gain-bandwidth product f_T and the current amplification factor h_{fe} .

Embodiments of the present invention will now be described in detail, by way of example, with reference to the accompanying drawings, in which:

Figs. 1 to 9 illustrate the steps for producing a semiconductor device produced by a first embodiment of the present invention; wherein

Fig. 1 is a sectional view showing the formation of n^+ -type buried layers;

Fig. 2 is a sectional view showing the formation

of a channel stopper and a collector region (p-type buried layer) of the PNP transistor;

Fig. 3 is a sectional view showing the formation of a p^+ -type channel stopper of a high concentration and a p^+ -type buried layer of a high concentration by
5 implanting impurity ions into the channel stopper region and into a part of the collector region of PNP transistor;

Fig. 4 is a sectional view showing the formation
10 of an n -type well region in a part of the NPN transistor-forming region and in a part of the PNP transistor-forming region, after an n -type silicon layer has been epitaxially grown on a single crystalline p -type silicon substrate;

15 Fig. 5 is a sectional view showing the formation of grooves in the isolation regions;

Fig. 6 is a sectional view showing the oxidation of the substrate with an antioxidation film as a mask;

Fig. 7 is a sectional view showing the formation
20 of a base region in the NPN transistor-forming region, and an emitter region and a collector take-out layer

in the PNP transistor-forming region, the collector take-out layer being in contact with the p-type buried layer;

Fig. 8 is a sectional view showing the formation of an emitter region and a collector take-out layer in the NPN transistor-forming region, and a base take-out layer in the PNP transistor-forming region;

Fig. 9 is a sectional view showing the formation of electrodes in the NPN transistor and in the PNP transistor;

Fig. 10 is a graph showing the distribution of impurity concentrations along the line A-A' in Fig. 9;

Figs. 11 and 12 are plan views for comparing the pattern of an existing lateral PNP transistor with the pattern of a vertical PNP transistor of the present invention, wherein Figs. 11A and 12A are section views along the line A-A' in Figs. 11 and 12, respectively;

Fig. 13 is a vertical sectional view of a semiconductor device produced by a second embodiment

of the present invention;

Figs. 14 to 19 are sectional views illustrating steps in a process for producing a semiconductor device according to a third embodiment of the present invention;

5 Fig. 20 is a diagram of a current mirror circuit using PNP transistors; and

Fig. 21 is a diagram of h_{fe} -collector current curves of a lateral PNP transistor and a vertical PNP transistor.

Embodiment 1

10 Figs. 1 to 9 illustrate a first embodiment of the present invention in which a semiconductor substrate is isolated by an isoplanar region to form a vertical PNP transistor and an NPN transistor, and are sectional views of steps in a process for producing semiconductor devices.

15 These steps will be described below in detail.

(1) As shown in Fig. 1, a p^- -type silicon substrate 1 is prepared having a resistivity which is as high as, for example, 8 to 13 ohms·cm. This substrate is heat-treated at 1000°C for 120 minutes in a wet atmosphere, so that a
20 thermally oxidized film which is 5000 angstroms thick is formed on one surface of the silicon substrate. The

oxide film is then partially removed by e.g. a standard photolithographic method. Using the oxide film (SiO_2) 2 as a mask, a donor impurity such as antimony is deposited and is diffused at about 1200°C for 200 minutes to form n^+ -type buried layers 3a, 3b which have a diffusion depth of 2 to 3 μm and a resistance of about 45 ohms.

(2) As shown in Fig. 2, a photoresist mask 4 is formed, and boron, which is an acceptor impurity, is introduced via the photoresist film 4 into the substrate by ion implantation. The energy for ion implantation is 80 KeV and the dosage is 2×10^{14} atoms/ cm^2 . Then heat-treatment is effected at about 1200°C for 60 minutes to form a p-type diffusion layer 5 that serves as a channel stopper, and a p-type buried layer 6 is formed in a part of the surface of the N^+ -type buried layer 3a.

(3) As shown in Fig. 3, boron ions are implanted via a photoresist mask 7 that is formed on

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the semiconductor substrate, in order to form p⁺-type buried layers 8 and 5' of a high concentration in a portion of the p-type buried layer 6 and in the p-type layer 5 in the channel stopper portion. The energy of ion implantation is 50 KeV, and the dosage is 5×10^{13} atoms/cm². Ion implantation is effected twice. If ions are introduced large amounts at one time, the silicon crystal is seriously damaged, giving rise to crystalline flaws. Thus, there are formed diffusion layer 5' having a p-type impurity concentration which is high enough to serve as channel stoppers, and a p⁺-type collector layer 8 having a sufficiently small collector series resistance r_{cs} . Thereafter, the oxide film 2 and the photoresist mask 7 are removed from the surface.

(4) A silicon layer doped with phosphorus at a low concentration is epitaxially grown on the whole surface at 970°C for 15 minutes to form an n⁻-type silicon layer 9 which is 1 to 2 μm thick and which has a resistivity of 1.6 ohms·cm. As shown in Fig. 4, the n⁺-type buried layer and p⁺-type buried layer are upwardly diffused to some extent due to the heat treatment of epitaxial growth. Then, using a surface oxide film 10 of

5 n⁻-type silicon layer or the photoresist film as a mask, phosphorus ions are implanted into the n⁻-type silicon layer 9 under the conditions of an implantation energy of 150 KeV and a dosage of 1×10^{14} atoms/cm² and are diffused at 1200°C for 200 minutes to form n-type well regions 11a, 11b that reach the buried layers.

10 (5) As shown in Fig. 5, an oxide film (SiO₂) 12 and a nitride film (Si₃N₄) 13 newly formed on the surface are partially etched, and using these films as masks, the silicon layer 9 is anisotropically etched to form grooves 14 at positions over the channel stopper p-type layers 5'. The plane (100) is selected as a crystalline surface of the substrate that is to be subjected to anisotropic etching, and use is made of an alkaline etching solution consisting of hydrazine and hydrofluoric/nitric acid, to obtain the grooves 14 having steep side surfaces and a depth of about 0.9 μm.

25 (6) Using the nitride film 13 as an antioxidation mask, silicon is selectively oxidized in a steam atmosphere under the conditions of 5 atms., 1000°C, for 145 minutes, to form isolation oxide films 15 in the grooves as shown in Fig. 6.

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The regions 9a and 9b are electrically isolated from each other by the isolation oxide film 15 and the p-type layer 5. The region 9a forms a PNP transistor, and the region 9b forms an NPN transistor.

(7) The nitride film is removed. Then, using a photoresist mask 16 formed on the surface, portions of the oxide film 12 are opened as shown in Fig. 7, and boron ions are implanted under the conditions of an implantation energy of 50 KeV and a dosage of 2.2×10^{14} atoms/cm². Then, the heat-treatment is effected in an nitrogen atmosphere at 1000°C for about 90 minutes to diffuse the introduced impurities, thereby to form a p-type layer 17 and a p-type layer 18 in a portion of the surface of the region 9a and to form a p-type layer 19 in a portion of the surface of the region 9b. The p-type layer 17 serves as an emitter of the PNP transistor, the n-type well region 11a serves as a base, the p-type buried layers 6, 8 serve as collectors, and the p-type layer 18 serves as a collector take-out portion.

(8) Using a photoresist mask 20 which is newly formed, other portions of the oxide film 12 are opened as shown in Fig. 8, and arsenic ions are

implanted under the conditions of an implantation energy of 80 KeV and a dosage of 5×10^{15} atoms/cm², and are then diffused by heat-treatment effected at 1000°C for 60 minutes, in order to

5 form an n⁺-type layer 21 that serves as a base take-out portion in a portion of the surface of the region 9a and to form an n⁺-type layer 22 and an n⁺-type layer 23 in portions of the surface of the region 9b. The n⁺-type layer 22 on the surface

10 of the n-type well region 11b serves as a collector take-out portion of the npn transistor, the p-type layer 19 serves as a base, and the n⁺-type layer 23 on the surface of the p-type layer 19 serves as an emitter.

15 (9) The surface of the oxide film 12 is covered with an insulating film 24 such as PSG (phosphorus silicate glass) having a phosphorus concentration of 1 to 2 mol and a thickness of 3000 angstroms), followed by contact photoetching. Then,

20 aluminum is deposited thereon by vaporization or sputtering, and patterning of aluminum is effected by etching. Thereafter, heat-treatment is effected at 470°C for about 10 minutes to form an aluminum electrode 25 that comes into ohmic contact with

25 each of the regions as shown in Fig. 9, wherein

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symbols B_1 , E_1 and C_1 denote the base, emitter and collector of the PNP transistor, and symbols C_2 , B_2 and E_2 denote the collector, base and emitter of the NPN transistor.

5 Fig. 10 shows profiles of impurity concentration in the cross section along the line A-A' of Fig. 9, i.e., along the vertical section of the vertical PNP transistor.

10 Fig. 11 is a plan view of a pattern of the lateral PNP transistor, and Fig. 11A is a section view along the line A-A' of Fig. 11. Fig. 12 is a plan view of a pattern of the vertical PNP transistor, and Fig. 12A is a section view along the line A-A' of Fig. 12. As seen in these drawings, 15 particularly in the section views, in the case of the lateral transistor, the carriers are injected through narrow portions of the side junctions of the p-type diffusion layers. In the case of the vertical transistor, on the other hand, the carriers 20 are effectively injected over wide areas of plane junctions of the p-type diffusion layers, and the collector current can be sufficiently increased. This means that the time for charge and discharge can be reduced to realize a gain-bandwidth product 25 f_T which is as high as about 100 MHz.

Below are described the effects obtained from particularly important steps in the aforementioned production process.

In the aforementioned process, steps (3) and (4) are quite important. That is, in the step (3), the p^+ -type buried layer 8 of a high concentration is formed in a portion of the p-type buried layer 6. The isolation diffusion layers 5' of a high concentration are also formed. As shown in Fig. 4, these buried layers of high concentration are upwardly diffused accompanying the formation of the epitaxial layer.

As described above, the buried high concentration layer 8 serves as a portion of the collector of the vertical pnp transistor. Owing to the upward diffusion, therefore, the contact region 18 (Fig. 7) of collector electrode can be formed by effecting the diffusion by heat only to a slight degree. Further, presence of the buried high concentration layer 8 helps reduce the collector series resistance r_{cs} of the vertical PNP transistor.

Here, if the p-type buried layer has a high concentration to which the n-type well region 11a is connected, the p-type impurities diffuse from

the p-type buried layer into the n-type well region 11a, and the effective base width W_B of the vertical PNP transistor changes. In order to prevent such a change, therefore, the buried high concentration layer 8 is formed in a portion of the p-type buried layer 6.

The isolation diffusion layer 5' has an impurity concentration which is so high as to maintain a sufficiently large reverse withstand voltage and to prevent the occurrence of parasitic channels. Furthermore, as mentioned above, the isolation diffusion layer 5' is formed accompanying the formation of the epitaxially grown layer. When a groove for forming the isolation region is to be engraved in the epitaxial layer, therefore, the depth of the groove needs be small, enabling the time required for this step to be reduced (see Figs. 5 and 6).

Attention should further be given to the fact that by inserting the n-type well region 11a, in which the impurity concentration is precisely controlled, the base width W_B of the vertical PNP transistor can be correctly determined. That is, in Fig. 11, the base width W_B is greatly affected by the mask-alignment precision and by the precision

of photoresist processing, causing the transistor performance to vary greatly. Referring to Fig. 12, on the other hand, the base width, which is a distance between the p-type buried layer 6 and the p-type emitter layer 17, can be precisely determined by the n-type well region 11a. For instance, even when the p-type buried layer 6 is unnecessarily diffused, the n-type well region 11a offsets the unnecessary portions, leaving necessary base width WB only. Since the base width WB can be maintained small and constant, the current amplification factor h_{fe} can be increased and maintained constant. Further, the base width WB is determined by determining the impurity concentration in the n-type well region 11a; i.e., a base width WB of any size can be formed. That is, since the base width WB is reduced, the cut-off frequency f_T can be increased. Further, the n-type well region 11a prevents contact between the p-type collector take-out layer 18 and the p-type emitter layer 17. This makes it possible to form a vertical PNP transistor maintaining good reproducibility, uniform characteristics and high performance. Further, the n-type well region has a gradient of concentration and exhibits a drift function.

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Further, if the size of the lateral PNP transistor shown in Fig. 11 is compared with the size of the vertical PNP transistor shown in Fig. 12, calculation by the inventors indicates that the size of the vertical PNP transistor is as small as about 0.42 times the size of the lateral PNP transistor.

From the practical point of view, furthermore, the vertical transistor of the present invention exhibits a large current amplification factor h_{fe} and gives advantage.

Fig. 21 shows relations between the collector current and h_{fe} of the vertical PNP transistor of the present invention and the lateral PNP transistor. It will be comprehended from Fig. 21 that the vertical PNP transistor of the present invention exhibits very high performance. An example will be described below with reference to a constant-current circuit (current mirror circuit) which is shown in Fig. 20.

Emitter terminals E_1 , E_2 of the two PNP transistors Q_1 , Q_2 are connected to a power source voltage V_{CC} . Base terminals B_1 , B_2 are connected together and are further connected via wiring X to the collector terminal of the transistor Q_1 .

If these transistors have a current amplification factor h_{fe} , then $I_{BQ1} = I_{BQ2} = I_B$, and $I_C = I_B \times h_{fe}$. Therefore, $I_{in} = I_{CQ1} + 2I_{BQ1}$, and $I_{out} = I_{BQ2} \times h_{fe}$.

A current mirror ratio C is given by,

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$$C = \frac{I_{in}}{I_{out}} = \frac{I_B \times h_{fe} + 2I_B}{I_B \times h_{fe}} \dots\dots\dots (1)$$

The current mirror ratio C should ideally be

1. As will be obvious from equation (1), the current mirror ratio varies depending upon the current amplification factor h_{fe} . For convenience,

10 the case described below is when the current amplification factor h_{fe} is as small as 10. In this case, the current mirror ratio C is $C = 1.2$. However, when the current amplification factor h_{fe} is as great as 100 as with the vertical PNP transistor of the present invention, the current mirror

15 ratio C becomes $C = 1.02$ which is close to the ideal value.

We may conclude from this that if the vertical PNP transistors of the present invention are used

20 for a constant-current circuit, it is possible to obtain an excellent current mirror ratio.

Effects

According to the above-mentioned embodiment 1 of the present invention, the following effects

may be obtained.

(1) Diffusing p-type impurities, to form a channel stopper that constitutes an isolation layer in the isoplanar technique, makes it possible to form the
5 p-type buried layer 6 that serves as a collector of the vertical PNP transistor without the need of adding an extra diffusion step.

(2) The collector electrode take-out layer 116 of the NPN transistor and the n-type well region 11a
10 that serves as a base of the PNP transistor may be formed in the same step. Also, the p-type layer 17 that serves as an emitter of the PNP transistor and the p-type layer 18 that serves as a collector take-out portion may be formed in the same step as
15 the diffusion of p-type impurities which form a base of the NPN transistor. Moreover, the base electrode take-out layer of the PNP transistor may be formed in the same step as the formation of the emitter of the NPN transistor. By utilizing the
20 steps in common as mentioned above, the process may be prevented from becoming complex.

(3) Since the PNP transistor may be of the vertical type, the collector current can be increased compared with that of the lateral PNP transistor of

the same size.

(4) To obtain a sufficiently large drive current, the lateral PNP transistors should preferably be connected in parallel. The vertical PNP transistor, however, may be used alone to obtain a sufficiently large drive current, since it has a good current amplification factor h_{fe} as shown in Fig. 21.

(5) The vertical PNP transistor cell size can be smaller than the lateral PNP transistor. For instance, the area can be halved. This fact is evident from comparison of the plan view of Fig. 11 showing a pattern of the lateral PNP transistor with the plan view of Fig. 12 showing a pattern of the vertical PNP transistor.

(6) By forming the n-type well layer, the impurity concentration may be controlled correctly in the base of the PNP transistor. Also, the p-type buried layer 6 that serves as a collector, the collector take-out portion 18, and the p^+ -type buried layer 8 connecting thereto, may be prevented from contacting the p-type layer that serves as the emitter.

(7) Owing to the effect mentioned in (6) above, the base width WB of the vertical PNP transistor may be controlled precisely, to form a high performance

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transistor that is relatively easy to produce.

(8) The circuit can be easily constructed with vertical PNP transistors. A current mirror circuit, which uses PNP transistors in a complementary manner, depends greatly upon the current amplification factor h_{fe} . Therefore, the current mirror ratio decreases when the current amplification factor h_{fe} is small. However, a vertical PNP transistor produced by a method according to the present invention may have a high current amplification factor h_{fe} , which makes it possible to obtain a sufficiently large current mirror ratio.

(9) The operation region of such a vertical PNP transistor resides in the substrate, and is not affected by interface ions. Therefore, the noise factor NF can be improved.

Embodiment 2

Fig. 13 illustrates a second embodiment of the present invention in which a semiconductor substrate is isolated by grooves to form a vertical PNP transistor, a vertical NPN transistor, and an IIL (injection integrated logic circuit). Fig. 13 is a sectional view of a finished semiconductor device. Isolation of the element by grooves is called HIT (high density isolation technology), a technique

that was developed by the applicant of the present invention.

The process conditions are nearly the same as those of the aforementioned embodiment and are
5 not described here.

In Fig. 13, reference numeral 1 denotes a common p^- -type silicon substrate, reference numerals 3a, 3b and 3c denote n^+ -type buried layers, 6 denotes a p-type buried layer, and 8 denotes a
10 p^+ -type buried layer. These buried layers are formed in the step of forming a p-type isolation (channel stopper) layer 5.

Reference numeral 14 denotes grooves for
15 isolation that can be formed in the same manner as the formation of grooves in the isoplaner process. In this embodiment 2, the groove 5 is formed widely to stretch to a portion where a collector take-out portion (n^+ -type layer 22) of
20 the NPN transistor is formed, so that n^+ -type impurities need not be deeply diffused to form the collector take-out portion. A p-type emitter layer 17 and a p-type collector take-out layer 18 constituting the vertical PNP transistor are formed
25 simultaneously with the formation of a p-type diffusion layer 19 that serves as a base of the

vertical npn transistor. An n^+ -type layer 21 that serves as a base take-out portion of the PNP transistor is formed simultaneously with the formation of an n^+ -type diffusion layer 23 that serves as an emitter of the NPN transistor and a collector take-out portion 22.

In the IIL portion, a p-type injector layer 26 and a p-type base layer 27 of the inverse npn transistor are formed simultaneously with the formation of a p-type diffusion layer 19 that serves as a base of the NPN transistor. A multi-collector 28 of the inverse NPN transistor is formed simultaneously with the formation of the n^+ -type diffusion layer 23 that serves as the emitter of the NPN transistor.

The semiconductor device of embodiment 2 exhibits the same effects as those mentioned for embodiment 1. With an isolation structure using grooves, furthermore, the present invention can also be effectively applied even where an IIL is present.

Embodiment 3

Figs. 14 to 19 are section views illustrating major steps in a process for producing semiconductor devices according to an embodiment of the present

invention wherein a vertical PNP transistor that is partly constituted by a Schottky barrier electrode and an NPN transistor are formed in one semiconductor substrate.

- 5 (1) Fig. 14 illustrates the state where n^+ -type buried layers 30a, 30b, p-type buried layers 60, 80, p^+ -type isolation layer 50' and epitaxial n^- -type silicon layer 90 are formed on a p^- -type silicon substrate 10 having a resistivity of 8 to 10 13 ohms.cm (see (1) to (4) of embodiment 1).
- (2) With an oxide film 120 and a nitride film 130 as masks, grooves 50 are formed to a depth of 0.9 μ m as shown in Fig. 15 using hydrazine and hydrofluoric/nitric acid. Of these grooves 50, 15 groove 50a works to isolate the base of the PNP transistor, groove 50b works to isolate the collector of the NPN transistor, and groove 50c works to isolate the element.
- (3) Using the nitride film 130 as a mask, 20 oxidation is effected selectively in a steam atmosphere under the conditions of a pressure of 5 atms., at a temperature of 1000°C, for 145 minutes, in order to form an isolation oxide film 150 in the grooves as shown in Fig. 16, thereby 25 to isolate a region 90a for forming the PNP

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transistor and a region 90b for forming the NPN transistor.

(4) The nitride film 130 is removed, portions of the oxide film 120 are opened to introduce phosphorus ions by the implantation method under the conditions of an implantation energy of 80 KeV, and a dosage of 1×10^{20} atoms/cm², followed by diffusion at 1000°C for 120 minutes, thereby to form, as shown in Fig. 17, a p⁺-type base take-out layer 210 of the PNP transistor and an n⁺-type collector take-out layer 220 of the NPN transistor. These layers are connected to the n⁻-type base region 90a and to the n⁻-type collector region 90b via the n⁺-type buried layers 30a, 30b.

(5) Portions of the oxide film 120 are opened, and boron ions are implanted under the conditions of an implantation energy of 50 KeV and a dosage of 2.2×10^{14} atoms/cm², and are diffused by the heat-treatment in an nitrogen atmosphere at a temperature of 1000°C for 90 minutes, thereby to form, as shown in Fig. 18, a p-type emitter layer 170 of the transistor so as to be connected to the p⁺-type buried layer 80 and, at the same time, to form a p-type base layer 190 of the NPN transistor.

(6) As shown in Fig. 19, arsenic ions are implanted

into a portion of the surface of the p-type base layer 190 of the NPN transistor under the conditions of an implantation energy of 80 KeV and a dosage of 5×10^{15} atoms/cm², followed by

5 diffusion effected at 1000°C for 60 minutes, thereby to form an n⁺-type emitter layer 230.

Simultaneously with the diffusion of emitter, the n⁺-type impurities may be diffused to lower the surface resistance of the n⁺-type base take-out

10 layer 210 of the PNP transistor and of the n⁺-type collector take-out layer 220 of the NPN transistor.

Finally, contact photoetching is effected to deposit aluminum by sputtering. The patterning is then effected by etching to form aluminum

15 electrodes 250. Then, directly on the surface of the n⁻-type silicon layer 90a of the PNP transistor, aluminum is heat-treated at 470°C for about 10 minutes, thereby to establish ohmic contact between aluminum and silicon, and Schottky barrier contact.

20 The electrode contacting the n⁺-type layer 210 serves as a base electrode B₁, and the electrode contacting to the p-type emitter layer 170 serves as an emitter electrode, whereby the PNP transistor is completed with an SBD as a collector portion.

25 Effects

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(1) Because of the vertical structure, components in the vertical direction can be utilized as a collector current, and the operation time constant τ_F can be reduced for the same base-emitter voltage V_{BE} to increase the cut-off frequency f_T .

(2) Since the collector semiconductor region has been replaced by a Schottky barrier metal, injection of minority carriers can be substantially neglected from the Schottky barrier metal to the base region, and the switching speed does not decrease.

(3) The area of the element can be reduced compared with that of an ordinary lateral PNP transistor.

(4) Owing to the effects mentioned in (1) to (3) above, great effects can be obtained if the PNP transistors and NPN transistors are used for the complementary circuits and particularly for the high-frequency circuits.

Although the invention accomplished by the inventors was concretely described above by way of embodiments, it should be noted that the present invention is not limited to the aforementioned embodiments only, but can be modified in a variety of other ways,

The present invention can be adapted to general linear integrated circuits and digital integrated circuits.



(47)

CLAIMS:

1. A process for producing a bipolar semiconductor device, comprising:

selectively introducing impurities of a first conductivity type into a semiconductor substrate, to form first and second semiconductor regions separated from each other;

introducing impurities of the first conductivity type into the first semiconductor region, to give the first semiconductor region a high impurity concentration, and simultaneously introducing impurities of the first conductivity type selectively into a part of the second semiconductor region, to form a third semiconductor region having a high impurity concentration;

selectively depositing a semiconductor layer on a surface of the substrate, thereby to cover the first, second and third semiconductor regions;

introducing impurities of the first conductivity type into the part of the semiconductor layer covering the third semiconductor region, thereby to form a fourth semiconductor region extending from the surface of the semiconductor layer to the third semiconductor region; and

forming a rectifying junction in the semiconductor layer overlying the second semiconductor region.

2. A process according to claim 1 wherein the rectifying junction is formed by:

selectively introducing impurities of the second



conductivity type into the semiconductor layer, to form a fifth semiconductor region which extends from the surface of the semiconductor layer to the second semiconductor region; and

5 introducing impurities of the first conductivity type into a part of the fifth semiconductor region, to form a sixth semiconductor region in the fifth semiconductor region.

3. A process according to claim 2, wherein the fourth and
10 sixth semiconductor regions are formed simultaneously.

4. A process according to any one of the preceding claims, wherein, prior to the formation of the first and second layers, impurities of the second conductivity type are introduced into the substrate to form first and second
15 buried layers isolated from each other, and the second semiconductor region is formed in the second buried layer.



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5. A process according to claim 4, wherein impurities of the second conductivity type are introduced selectively into the semiconductor layer, to form a seventh semiconductor region which extends from the surface of the semiconductor layer to the first buried layer.

6. A process according to claim 4 as dependent on claim 2, wherein the fifth and seventh semiconductor regions are formed simultaneously.

7. A process according to claim 5 or claim 6, wherein impurities of the second conductivity type are introduced into a part of the seventh semiconductor region, to form an eighth semiconductor region having a high impurity concentration.

8. A process according to any one of the preceding claims, wherein impurities of the first conductivity type are selectively introduced into a part of the semiconductor layer, thereby to form a ninth semiconductor region.

9. A process according to claim 8 as dependent on claim 3, wherein the ninth semiconductor region is formed simultaneously with the fourth and sixth semiconductor regions.

10. A process according to claim 8 or claim 9, wherein



impurities of the second conductivity type are introduced into a part of the ninth semiconductor region, thereby to form a tenth semiconductor region.

11. A process according to claim 10 as dependent on claim 7, wherein the eighth and tenth semiconductor layers are formed simultaneously.

12. A process according to any one of the preceding claims, wherein impurities of the second conductivity type are selectively introduced into the semiconductor layer, thereby to form an eleventh semiconductor layer.

13. A process according to claim 12 as dependent on claim 11, wherein the eighth, tenth, and eleventh semiconductor layers are formed simultaneously.

14. A process according to any one of the preceding claims wherein at least one groove is formed in the semiconductor layer, the at least one groove extending to the first semiconductor region.

15. A process according to any one of claims 1 to 14, wherein an electrically isolating film is formed in the semiconductor layer, the film extending to the first semiconductor layer.

16. A process according to claim 15 wherein the film



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is silicon oxide.

17. A process according to claim 1 wherein an electrode is formed in contact with the semiconductor layer over the second semiconductor region, and is treated to form a Schottky contact forming the rectifying junction.

18. A process according to claim 17 wherein:
prior to the formation of the first and second layers, impurities of the second conductivity type are introduced into the substrate to form first and second buried layers isolated from each other, and the second semiconductor region is formed in the second buried layer;

an electrically isolated film is formed in the semiconductor layer, the film extending to the first semiconductor layer to form first and second island regions, the fourth semiconductor region being in the second island region;

selectively introducing impurities of the second conductivity type into the first island region to form a fifth semiconductor region which extends from the surface of the first island region to the first buried layer;

selectively introducing impurities of the second conductivity type into the second island region to form a sixth semiconductor region which extends from the surface of the second island region to the second buried layer;

selectively introducing impurities of the first



conductivity type into the first island region to form a seventh semiconductor region;

selectively introducing impurities of the second conductivity type into part of the seventh semiconductor region to form an eighth semiconductor region; and

forming electrodes to contact the fifth to eighth semiconductor regions of the first conductivity type into the second island region to form a seventh semiconductor region which extends to the third semiconductor region;

selectively introducing impurities of the first conductivity type into the sixth semiconductor region to form an eighth semiconductor region; and

forming an electrode to contact each of the second island regions, the fourth, the fifth, the sixth and the eighth semiconductor regions.

19. A process according to claim 18, wherein all the electrodes are heat treated.

20. A process according to claim 18 or claim 20, wherein the fifth and sixth semiconductor regions are formed simultaneously.

21. A process according to any one of claims 18 to 20 wherein the fourth and seventh semiconductor regions are formed simultaneously.



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22. A process according to any one of claims 17 to 21, wherein the first and second semiconductor regions are formed simultaneously.

23. A process according to any one of claims 17 to 22,
5 wherein impurities of the first conductivity type are introduced into the first semiconductor region simultaneously with the introduction of impurities into the part of the second semiconductor region, thereby to give the first semiconductor region a high impurity concentration.

10 24. A process according to any one of the preceding claims, wherein the substrate is of silicon.

25. A process according to any one of the preceding claims, wherein the substrate is of the first conductivity type.

15 26. A process for producing a semiconductor device substantially as any one herein described with reference to Figs. 1 to 9 or Fig. 12 or Fig. 13 or Figs. 14 to 19 of the accompanying drawings.
