What is claimed is:

1. A semiconductor memory device comprising:

a semiconductor substrate;

a plurality of element isolations formed in an upper portion of the semiconductor substrate and partitioning the upper portion into a plurality of active areas extending in a first direction;

a plurality of first stacked bodies provided on the semiconductor substrate and extending in a second direction crossing the first direction;

a second stacked body provided on the semiconductor substrate, located outside a region populated with the plurality of first stacked bodies, and extending in the second direction; and

an interlayer insulating film covering the first stacked bodies and the second stacked body,

each of the first stacked bodies including:

a first electrode provided above each of the active areas;

an insulating film provided on the first electrode; and

a second electrode provided on the insulating film and extending in the second direction,

distance between each of the first stacked bodies and the second stacked body being longer than distance between adjacent ones of the first stacked bodies,

a first void being formed in the interlayer insulating film between the first stacked bodies,

a second void being formed in the interlayer insulating film between one of the first stacked bodies and the second stacked body, and

a lower end of the second void being located above a lower end of the first void, wherein the lower end of the first void is located below an upper surface of the first electrode.

2. The device according to claim 1, wherein the lower end of the second void is located above an upper surface of the first electrode.

3. The device according to claim 1, wherein the lower end of the second void is located below a lower surface of the second electrode.

4. The device according to claim 1, wherein upper ends of the first and second voids are located above an upper surface of the second electrode.

5. The device according to claim 1, wherein

the second stacked body includes:

a first conductive portion provided on same level as the first electrode;

a second conductive portion provided on same level as the second electrode;

another insulating film provided on same level as the insulating film and including an opening; and

a connecting member provided in the opening and connecting the second conductive portion to the first conductive portion.

6. The device according to claim 1, wherein no program voltage is applied to the second electrode of one of the plurality of first stacked bodies, the one of the plurality of first stacked bodies is located next to the second stacked body.

~~7. A method for manufacturing a semiconductor memory device, comprising:~~

~~forming trenches extending in a first direction in an upper portion of a semiconductor substrate;~~

~~partitioning the upper portion into a plurality of active areas by burying an insulating material in the trenches;~~

~~forming a plurality of first stacked bodies and a second stacked body on the semiconductor substrate so that distance between the second stacked body and the neighboring one of the first stacked bodies is longer than that between adjacent ones of the first stacked bodies, each of the first stacked bodies extending in a second direction crossing the first direction and being formed by stacking a first electrode located above each of the active areas, an insulating film provided on the first electrode, and a second electrode provided on the insulating film and extending in the second direction, the second stacked body being located outside a region populated with the plurality of first stacked bodies, and extending in the second direction;~~

~~forming an interlayer insulating film so as to cover the first stacked bodies and the second stacked body, simultaneously forming a first void in the interlayer insulating film between the first stacked bodies and forming a second void in the interlayer insulating film between one of the first stacked bodies and the second stacked body, and locating a lower end of the second void above a lower end of the first void.~~

~~8. The method according to claim 7, wherein forming the interlayer insulating film is performed by chemical vapor deposition.~~

~~9. A method for manufacturing a semiconductor memory device, comprising:~~

~~forming trenches extending in a first direction in an upper portion of a semiconductor substrate;~~

~~partitioning the upper portion into a plurality of active areas by burying an insulating material in the trenches;~~

~~forming a plurality of first stacked bodies and a second stacked body on the semiconductor substrate so that distance between each of the first stacked bodies and the second stacked body is longer than distance between adjacent ones of the first stacked bodies, each of the first stacked bodies extending in a second direction crossing the first direction and being formed by stacking a first electrode located above each of the active areas, an insulating film provided on the first electrode, and a second electrode provided on the insulating film and extending in the second direction, the second stacked body being located~~

~~outside a region populated with the plurality of first stacked bodies, and extending in the second direction;~~

~~a first deposition being configured to form an interlayer insulating film so as to cover the first stacked bodies and the second stacked body, simultaneously form a first void in the interlayer insulating film between the first stacked bodies and form a second void in the interlayer insulating film between one of the first stacked bodies and the second stacked body, and seal an upper end of the first void with an upper end of the second void left open; and~~

~~a second deposition being configured to fill a lower portion of the second void and seal the upper end of the second void by depositing an insulating material.~~

~~10. The method according to claim 9, wherein the first deposition is performed by a method with lower buriability of the insulating material than the second deposition.~~

~~11. The method according to claim 9, wherein deposition of the insulating material in the first deposition is performed by chemical vapor deposition, and deposition of the insulating material in the second deposition is performed by atomic layer deposition.~~