NON-VOLATILE MEMORY DEVICE

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This patent application claims benefit of priority to Korean Patent Application No. 10-2022-0017738, filed on 10 February 2022, and Korean Patent Application No. 10-2022-0081506, filed on 1 July 2022, in the Korean Intellectual Property Office, the disclosures of which are incorporated by reference herein in their entireties.

TECHNICAL FIELD

[0002] The present disclosure relates to a memory device, and more particularly, to a three-dimensional non-volatile memory device in which a memory cell array overlaps a partial region of a peripheral circuit.

BACKGROUND

[0003] Related memory devices may be used to store data, and may be classified into volatile memory devices and non-volatile memory devices. In response to the demand for high capacity and miniaturization of non-volatile memory devices, related three-dimensional memory devices have been developed in which memory cell arrays and peripheral circuits are vertically arranged. In order to increase the capacity of a related non-volatile memory device, as the number of word lines stacked on a substrate increases, the area of a cell region in which a memory cell array is arranged may decrease. However, despite the decrease in the area of the cell region, the area of a peripheral circuit region in which a peripheral circuit is arranged under the memory cell array may not decrease.

SUMMARY

[0004] The present disclosure provides a non-volatile memory device in which some

circuits constituting a peripheral circuit are buried by a cell region and the other circuits constituting the peripheral circuit are not buried by the cell region, as the number of stacked word lines increases.

[0005] According to an aspect of the present disclosure, a non-volatile memory device includes a first semiconductor layer and a second semiconductor layer. The first semiconductor layer includes a first memory cell array, a second memory cell array, and a first metal pad. The first memory cell array is disposed on a first cell region of the first semiconductor layer, and includes a first plurality of word lines stacked in a vertical direction and a first plurality of memory cells respectively coupled to the first plurality of word lines. The second memory cell array is disposed on a second cell region of the first semiconductor layer, and includes a second plurality of word lines stacked in the vertical direction and a second plurality of memory cells respectively coupled to the second plurality of word lines. The second semiconductor layer includes a first peripheral circuit disposed on a first region of the second semiconductor layer and coupled to the first memory cell array, a second peripheral circuit disposed on a second region of the second semiconductor layer and coupled to the second memory cell array, and a second metal pad. The second semiconductor layer is coupled, in the vertical direction, to the first semiconductor layer by the first metal pad and the second metal pad in a bonding manner. The first region includes a first peripheral circuit region that overlaps the first cell region in the vertical direction, and a second peripheral circuit region that does not overlap the first cell region in the vertical direction. The second region overlaps the second cell region in the vertical direction.

[0006] According to an aspect of the present disclosure, a non-volatile memory device includes a first semiconductor layer and a second semiconductor layer. The first semiconductor layer includes a memory cell array disposed on a cell region of the first semiconductor layer, and a first metal pad. The memory cell array includes a plurality of

word lines stacked in a vertical direction and a plurality of memory cells respectively coupled to the plurality of word lines. The second semiconductor layer includes a peripheral circuit disposed on a peripheral circuit region of the second semiconductor layer, and a second metal pad. The second semiconductor layer is coupled, in the vertical direction, to the first semiconductor layer by the first metal pad and the second metal pad in a bonding manner. The peripheral circuit region includes a first peripheral circuit region that overlaps the cell region in the vertical direction, and a second peripheral circuit region that does not overlap the cell region in the vertical direction. An area of the peripheral circuit region is greater than an area of the cell region. The peripheral circuit includes a page buffer circuit connected to the plurality of memory cells through a plurality of bit lines. A portion of the page buffer circuit is disposed on the first peripheral circuit region. Another portion of the page buffer circuit is disposed on the second peripheral circuit region.

[0007] According to an aspect of the present disclosure, a non-volatile memory device includes a first semiconductor layer and a second semiconductor layer. The first semiconductor layer includes a cell region on which a memory cell array is disposed, and a first metal pad. The memory cell array includes a plurality of word lines stacked in a vertical direction and a plurality of memory cells respectively coupled to the plurality of word lines. The second semiconductor layer includes a peripheral circuit region on which a peripheral circuit is disposed, and a second metal pad. The second semiconductor layer is coupled, in the vertical direction, to the first semiconductor layer by the first metal pad and the second metal pad in a bonding manner. The peripheral circuit region includes a first peripheral circuit region that overlaps the cell region in the vertical direction, and a second peripheral circuit region that does not overlap the cell region in the vertical direction. An area of the peripheral circuit region is greater than an area of the cell region. The peripheral circuit further includes a row decoder connected to the plurality of word lines. A portion of the row decoder is

arranged in the first peripheral circuit region. Another portion of the row decoder is arranged in the second peripheral circuit region.

BRIEF DESCRIPTION OF DRAWINGS

[0008] The above and other aspects, features, and advantages of certain embodiments of the present disclosure will be more apparent from the following description taken in conjunction with the accompanying drawings in which:

[0009] FIG. 1 is a block diagram illustrating a memory device according, to an embodiment;

[0010] FIG. 2 is a circuit diagram illustrating a memory block, according to an embodiment;

[0011] FIGS. 3A and 3B are perspective views respectively illustrating memory blocks, according to some embodiments;

[0012] FIG. 4 is a diagram schematically illustrating a memory device having a cell-over-periphery (COP) structure, according to an embodiment;

[0013] FIG. 5 is a cross-sectional view of a memory device having a bonding-vertical-NAND (B-VNAND) structure, according to an embodiment;

[0014] FIG. 6 is a diagram illustrating a memory device according to a comparative example, and a memory device, according to an embodiment;

[0015] FIGS. 7A and 7B are diagrams respectively illustrating memory devices, according to some embodiments;

[0016] FIG. 8 is a circuit diagram illustrating a page buffer circuit, according to an embodiment;

[0017] FIG. 9 is a circuit diagram illustrating a page buffer decoder, according to an

embodiment;

[0018] FIG. 10 is a diagram illustrating a row decoder and a pass transistor circuit, according to an embodiment;

[0019] FIGS. 11A to 11D are diagrams respectively illustrating memory devices, according to some embodiments;

[0020] FIGS. 12A to 12F are diagrams respectively illustrating memory devices, according to some embodiments;

[0021] FIGS. 13A and 13B are diagrams respectively illustrating memory devices, according to some embodiments;

[0022] FIGS. 14A and 14B are diagrams respectively illustrating memory devices, according to some embodiments;

[0023] FIGS. 15A to 15D are diagrams respectively illustrating memory devices, according to some embodiments;

[0024] FIGS. 16A and 16B are diagrams respectively illustrating memory devices, according to some embodiments;

[0025] FIGS. 17A to 17D are diagrams respectively illustrating memory devices, according to some embodiments;

[0026] FIGS. 18A and 18B are diagrams respectively illustrating memory devices, according to some embodiments;

[0027] FIGS. 19A to 19D are diagrams respectively illustrating memory devices, according to some embodiments;

[0028] FIGS. 20A and 20B are diagrams respectively illustrating memory devices, according to some embodiments;

[0029] FIGS. 21A to 21D are diagrams respectively illustrating memory devices, according to some embodiments;

[0030] FIGS. 22A and 22B are diagrams respectively illustrating memory devices, according to some embodiments;

[0031] FIGS. 23A to 23D are diagrams respectively illustrating memory devices, according to some embodiments;

[0032] FIGS. 24A and 24B are diagrams respectively illustrating memory devices, according to some embodiments;

[0033] FIGS. 25A to 25D are diagrams respectively illustrating memory devices, according to some embodiments;

[0034] FIGS. 26A and 26B are diagrams respectively illustrating memory devices, according to some embodiments; and

[0035] FIG. 27 is a block diagram illustrating a solid-state drive (SSD) system to which a memory device, according to an embodiment.

DETAILED DESCRIPTION

[0036] The following description with reference to the accompanying drawings is provided to assist in a comprehensive understanding of embodiments of the present disclosure defined by the claims and their equivalents. Various specific details are included to assist in understanding, but these details are considered to be exemplary only. Therefore, those of ordinary skill in the art will recognize that various changes and modifications of the embodiments described herein can be made without departing from the scope and spirit of the disclosure. In addition, descriptions of well-known functions and structures are omitted for clarity and conciseness.

[0037] With regard to the description of the drawings, similar reference numerals may be used to refer to similar or related elements. It is to be understood that a singular form of a noun corresponding to an item may include one or more of the things, unless the relevant context clearly indicates otherwise. As used herein, each of such phrases as “A or B,” “at least one of A and B,” “at least one of A or B,” “A, B, or C,” “at least one of A, B, and C,” and “at least one of A, B, or C,” may include any one of, or all possible combinations of the items enumerated together in a corresponding one of the phrases. As used herein, such terms as “1st” and “2nd,” or “first” and “second” may be used to simply distinguish a corresponding component from another, and does not limit the components in other aspect (e.g., importance or order). It is to be understood that if an element (e.g., a first element) is referred to, with or without the term “operatively” or “communicatively”, as “coupled with,” “coupled to,” “connected with,” or “connected to” another element (e.g., a second element), it means that the element may be coupled with the other element directly (e.g., wired), wirelessly, or via a third element.

[0038] It will be understood that when an element or layer is referred to as being “over,” “above,” “on,” “below,” “under,” “beneath,” “connected to” or “coupled to” another element or layer, it can be directly over, above, on, below, under, beneath, connected or coupled to the other element or layer or intervening elements or layers may be present. In contrast, when an element is referred to as being “directly over,” “directly above,” “directly on,” “directly below,” “directly under,” “directly beneath,” “directly connected to” or “directly coupled to” another element or layer, there are no intervening elements or layers present.

[0039] FIG. 1 is a block diagram illustrating a memory device 10, according to an embodiment.

[0040] Referring to FIG. 1, the memory device 10 may include a memory cell array

11 and a peripheral circuit PECT, and the peripheral circuit PECT may include a page buffer circuit 12, a row decoder 13, a control logic circuit 14, and a voltage generator 15. In some embodiments, the peripheral circuit PECT may further include a data input/output circuit, an input/output interface, and the like (not shown). Alternatively or additionally, the peripheral circuit PECT may further include a pre-decoder, a temperature sensor, a command decoder, an address decoder, and the like. As used herein, the memory device 10 may refer to a "non-volatile memory device".

[0041] The memory cell array 11 may include a plurality of memory blocks BLK1 to BLKz (hereinafter "BLK", generally), where z is a positive integer. Each of the plurality of memory blocks BLK may include a plurality of memory cells. The memory cell array 11 may be connected to the page buffer circuit 12 through bit lines BL, and may be connected to the row decoder 13 through word lines WL, string select lines SSL, and ground select lines GSL. For example, the memory cells may be flash memory cells. Hereinafter, embodiments are described with reference to an example in which the memory cells are NAND flash memory cells. However, the present disclosure is not limited thereto, and in some embodiments, the memory cells may be resistive memory cells, such as resistive random-access memory (RAM) (ReRAM) memory cells, phase-change RAM (PRAM) memory cells, or magnetic RAM (MRAM) memory cells.

[0042] In some embodiments, the memory cell array 11 may include a three-dimensional memory cell array, which may include a plurality of NAND strings, each of which may include memory cells respectively connected (coupled) to word lines vertically stacked on a substrate, as described in detail with reference to FIGS. 2 to 3B. U.S. Patent Nos. 7,679,133, 8,553,466, 8,654,587, 8,559,235, and 9,536,970 disclose appropriate configurations of a three-dimensional memory array in which the three-dimensional memory array is configured in a plurality of levels, and word lines and/or bit lines are shared between

the levels, the disclosures of which are incorporated in their entirety by reference herein. However, the present disclosure is not limited thereto, and in some embodiments, the memory cell array 11 may include a two-dimensional memory cell array, which may include a plurality of NAND strings arranged in row and column directions.

[0043] The page buffer circuit 12 may include a plurality of page buffers PB1 to PBn (hereinafter “PB”, generally), where n is a positive integer. The plurality of page buffers PB may be connected (coupled) to the memory cells of the memory cell array 11 through the corresponding bit lines, respectively. The page buffer circuit 12 may select at least one of the bit lines BL under control by the control logic circuit 14. For example, the page buffer circuit 12 may select some of the bit lines BL in response to a column address Y_ADDR received from the control logic circuit 14.

[0044] Each of the plurality of page buffers PB may operate as a write driver or a sense amplifier. For example, in a program operation, each of the plurality of page buffers PB may store, in a memory cell, data DATA to be programmed, by applying a voltage corresponding to the data DATA to a bit line. For example, in a program verify operation or a read operation, each of the plurality of page buffers PB may detect the programmed data DATA by sensing a current or a voltage through a bit line.

[0045] Based on a command CMD, an address ADDR, and a control signal CTRL, the control logic circuit 14 may output various control signals for programming data to the memory cell array 11, reading data from the memory cell array 11, or erasing data stored in the memory cell array 11, for example, a voltage control signal CTRL_vol, a row address X_ADDR, and the column address Y_ADDR. Accordingly, the control logic circuit 14 may generally control various operations of the memory device 10. For example, the control logic circuit 14 may receive the command CMD, the address ADDR, and the control signal CTRL from a memory controller (not shown).

[0046] The voltage generator 15 may generate various types of voltages to perform program, read, and erase operations on the memory cell array 11, based on the voltage control signal CTRL_vol. For example, the voltage generator 15 may generate a word line voltage VWL, such as, but not limited to, a program voltage, a read voltage, a pass voltage, an erase verify voltage, or a program verify voltage. Alternatively or additionally, the voltage generator 15 may further generate a string select line voltage VSSL and a ground select line voltage VGSL based on the voltage control signal CTRL_vol.

[0047] In response to the row address X_ADDR received from the control logic circuit 14, the row decoder 13 may select one of the plurality of memory blocks BLK, select one of the word lines WL of the selected memory block, and select one of the plurality of string select lines SSL. For example, in a program operation, the row decoder 13 may apply a program voltage and a program verify voltage to the selected word line. For another example, in a read operation, the row decoder 13 may apply a read voltage to the selected word line.

[0048] According to some embodiments, the memory cell array 11 may be arranged (disposed) in a first semiconductor layer (e.g., L1 in FIG. 4 or CELL1 and CELL2 in FIG. 5), the peripheral circuit PECT may arranged (disposed) in a second semiconductor layer (e.g., L2 in FIG. 4 or PERI in FIG. 5), and a partial region of the peripheral circuit PECT may be buried by the memory cell array 11, and the remaining region of the peripheral circuit PECT may not be buried by the memory cell array 11. That is, the partial region of the peripheral circuit PECT may overlap the memory cell array 11 in the vertical direction, and the remaining region of the peripheral circuit PECT may not vertically overlap the memory cell array 11.

[0049] FIG. 2 is a circuit diagram illustrating a memory block BLK, according to an embodiment.

[0050] Referring to FIG. 2, the memory block BLK may correspond to one of the plurality of memory blocks BLK of FIG. 1. The memory block BLK may include NAND strings NS11 to NS33, and each NAND string (e.g., NS11) may include a string select transistor SST, a plurality of memory cells MCs, and a ground select transistor GST, which are connected in series. The string select and ground select transistors SST and GST and the memory cells MCs included in each NAND string may form a stacked structure on a substrate in a vertical direction.

[0051] Bit lines BL1 to BL3 (hereinafter, also referred to as the first to third bit lines BL1 to BL3) may extend in a first direction or a first horizontal direction, and word lines WL1 to WL8 may extend in a second direction or a second horizontal direction. As used herein, the first horizontal direction refers to the first direction, and the second horizontal direction refers to the second direction. The NAND strings NS11, NS21, and NS31 may be between the first bit line BL1 and a common source line CSL, the NAND strings NS12, NS22, and NS32 may be between the second bit line BL2 and the common source line CSL, and the NAND strings NS13, NS23, and NS33 may be between the third bit line BL3 and the common source line CSL.

[0052] The string select transistors SST may be connected to corresponding string select lines SSL1 to SSL3, respectively. The memory cells MCs may be connected to the corresponding word lines WL1 to WL8, respectively. The ground select transistors GST may be connected to corresponding ground select lines GSL1 to GSL3, respectively. The string select transistors SST may be connected to the corresponding bit lines, and the ground select transistors GST may be connected to the common source line CSL. In some embodiments, the number of NAND strings, the number of word lines, the number of bit lines, the number of ground select lines, and the number of string select lines may vary depending on embodiments.

[0053] FIG. 3A is a perspective view illustrating a memory block BLKa, according to an embodiment.

[0054] Referring to FIG. 3A, the memory block BLKa may correspond to one of the plurality of memory blocks BLK of FIG. 1. The memory block BLKa is formed in a vertical direction VD with respect to a substrate SUB. The substrate SUB may have a first conductivity type (e.g., p-type) and may extend in the second direction or a second horizontal direction HD2 on the substrate SUB. In some embodiments, the common source line CSL doped with impurities of a second conductivity type (e.g., n type) may be provided on the substrate SUB. In other embodiments, the common source line CSL may be implemented as a conductive layer, such as a metal layer. A plurality of insulating films IL extending in the second horizontal direction HD2 are sequentially provided in the vertical direction VD in a region of the substrate SUB, and the plurality of insulating films IL are spaced a certain distance from each other in the vertical direction VD. For example, the plurality of insulating films IL may include an insulating material, such as, but not limited to, silicon oxide.

[0055] A plurality of pillars P are provided in a region of the substrate SUB, to be sequentially arranged in the first direction or a first horizontal direction HD1 and penetrate the plurality of insulating films IL in the vertical direction VD. For example, the plurality of pillars P may penetrate the plurality of insulating films IL and be in contact with the substrate SUB. For example, a surface layer S of each of the pillars P may include a first-type silicon material and function as a channel region. Accordingly, in some embodiments, the pillar P may be referred to as a channel structure or a vertical channel structure. An inner layer I of each of the pillars P may include an insulating material, such as silicon oxide, or an air gap, and the like.

[0056] In a region between two adjacent common source lines CSL, a charge storage layer CS is provided along exposed surfaces of the insulating films IL, the pillars P, and the

substrate SUB. The charge storage layer CS may include a gate insulating layer (also referred to as a 'tunneling insulating layer'), a charge trapping layer, and a blocking insulating layer. For example, the charge storage layer CS may have an oxide-nitride-oxide (ONO) structure. Alternatively or additionally, in a region between two adjacent common source lines CSL, gate electrodes GE including the select lines GSL and SSL and the word lines WL1 to WL8 are provided on the exposed surface of the charge storage layer CS. Drain contacts or drains DR are provided on the plurality of pillars P, respectively. For example, the drains DR may include a silicon material doped with impurities having the second conductivity type. The bit lines BL1 to BL3 extending in the first horizontal direction HD1 and spaced a certain distance from each other in the second horizontal direction HD2 are provided on the drains DR.

[0057] FIG. 3B is a perspective view illustrating a memory block BLKb according to an embodiment.

[0058] Referring to FIG. 3B, the memory block BLKb may correspond to one of the plurality of memory blocks BLK of FIG. 1. Alternatively or additionally, the memory block BLKb corresponds to a modification of the memory block BLKa of FIG. 3A, and the descriptions provided above with reference to FIG. 3A may also be applied to memory block BLKb of FIG. 3B. The memory block BLKb may be formed in a direction perpendicular to the substrate SUB. The memory block BLKb may include a first memory stack ST1 and a second memory stack ST2, which are stacked in the vertical direction VD.

[0059] FIG. 4 is a diagram schematically illustrating a memory device 40 having a cell-over-periphery (COP) structure, according to an embodiment.

[0060] Referring to FIGS. 1 and 4, the memory device 40 may include a first semiconductor layer L1 and a second semiconductor layer L2, and the first semiconductor

layer L1 may be stacked in the vertical direction VD with respect to the second semiconductor layer L2. For example, the second semiconductor layer L2 may be arranged below the first semiconductor layer L1 in the vertical direction VD, and accordingly, may be arranged close to the substrate.

[0061] In some embodiments, the memory cell array 11 may be formed in the first semiconductor layer L1, and the peripheral circuit PECT may be formed in the second semiconductor layer L2. Accordingly, the memory device 40 may have a structure in which the memory cell array 11 is arranged on top of the peripheral circuit PECT, (e.g., a COP structure). The COP structure may effectively reduce a horizontal area and improve the degree of integration of the memory device 40.

[0062] In some embodiments, the second semiconductor layer L2 may include a substrate, and the peripheral circuit PECT may be formed in the second semiconductor layer L2 by forming transistors and metal patterns for the wiring of the transistors on the substrate. After the peripheral circuit PECT is formed in the second semiconductor layer L2, the first semiconductor layer L1 including the memory cell array 11 may be formed, and metal patterns for electrically connecting the word lines WL and the bit lines BL of the memory cell array 11 to the peripheral circuit PECT formed in the second semiconductor layer L2 may be formed. For example, the bit lines BL may extend in the first horizontal direction HD1, and the word lines WL may extend in the second horizontal direction HD2. For example, the memory block BLKa of FIG. 3A or the memory block BLKb of FIG. 3B may be formed in the first semiconductor layer L1.

[0063] With the development of semiconductor processes, as the number of memory cells arranged (disposed) in the memory cell array 11 of the first semiconductor layer L1 increases, (e.g., as the number of stacked word lines WL increases), the area of the memory cell array 11, (e.g., the area of a cell region) decreases. For example, the cell region may be

defined as a region in which a plurality of NAND strings (e.g., NS11 to NS33 of FIG. 2) or a plurality of pillars (e.g., P of FIGS. 3A and 3B) are arranged. For another example, the cell region may be defined as a region in which a plurality of word lines (e.g., WL1 to WL8 of FIGS. 2, 3A, and 3B) are arranged. For another example, the cell region may be defined as a region in which a plurality of bit lines (e.g., BL1, BL2, BL3 of FIGS. 2, 3A, and 3B) are arranged. However, the cell region is not limited thereto, and may be defined as a region including the memory cell array 11.

[0064] Alternatively or additionally, the area of a peripheral circuit region in which the peripheral circuit PECT of the second semiconductor layer L2 is arranged may not decrease as much as does the area of the cell region. Accordingly, in some embodiments, a first peripheral circuit region of the peripheral circuit region of the second semiconductor layer L2 overlaps the memory cell array 11 in the vertical direction VD, and a second peripheral circuit region of the peripheral circuit region of the second semiconductor layer L2 may not overlap the memory cell array 11 in the vertical direction VD.

[0065] FIG. 5 is a diagram illustrating a memory device 50, according to some embodiments.

[0066] Referring to FIG. 5, the memory device 50 may have a chip-to-chip (C2C) structure. At least one upper chip including a cell region and a lower chip including a peripheral circuit region PERI may be manufactured separately, and then, the at least one upper chip and the lower chip may be connected to each other by a bonding method to realize the C2C structure. For example, the bonding method may refer to a method of electrically and/or physically connecting a bonding metal pattern formed in an uppermost metal layer of the upper chip to a bonding metal pattern formed in an uppermost metal layer of the lower chip. For example, in a case in which the bonding metal patterns are formed of copper (Cu), the bonding method may be a Cu-Cu bonding method. Alternatively or additionally, the

bonding metal patterns may be formed of aluminum (Al) or tungsten (W).

[0067] The memory device 50 may include the at least one upper chip including the cell region. For example, as illustrated in FIG. 5, the memory device 50 may include two upper chips. However, the number of the upper chips is not limited thereto. In the case in which the memory device 50 includes the two upper chips, a first upper chip including a first cell region CELL1, a second upper chip including a second cell region CELL2 and the lower chip including the peripheral circuit region PERI may be manufactured separately, and then, the first upper chip, the second upper chip and the lower chip may be connected to each other by the bonding method to manufacture the memory device 50. The first upper chip may be turned over and then may be connected to the lower chip by the bonding method, and the second upper chip may also be turned over and then may be connected to the first upper chip by the bonding method. Hereinafter, upper and lower portions of each of the first and second upper chips will be defined based on before each of the first and second upper chips is turned over. That is, an upper portion of the lower chip may mean an upper portion defined based on a +Z-axis direction, and the upper portion of each of the first and second upper chips may mean an upper portion defined based on a -Z-axis direction in FIG. 5. However, embodiments are not limited thereto. In some embodiments, one of the first upper chip and the second upper chip may be turned over and then may be connected to a corresponding chip by the bonding method.

[0068] Each of the peripheral circuit region PERI and the first and second cell regions CELL1 and CELL2 of the memory device 50 may include an external pad bonding region PA, a word line bonding region WLBA, and a bit line bonding region BLBA.

[0069] The peripheral circuit region PERI may include a first substrate 210 and a plurality of circuit elements 220a, 220b and 220c formed on the first substrate 210. An interlayer insulating layer 215 including one or more insulating layers may be provided on

the plurality of circuit elements 220a, 220b and 220c, and a plurality of metal lines electrically connected (coupled) to the plurality of circuit elements 220a, 220b and 220c may be provided in the interlayer insulating layer 215. For example, the plurality of metal lines may include first metal lines 230a, 230b and 230c connected to the plurality of circuit elements 220a, 220b and 220c, and second metal lines 240a, 240b and 240c formed on the first metal lines 230a, 230b and 230c. The plurality of metal lines may be formed of at least one of various conductive materials. For example, the first metal lines 230a, 230b and 230c may be formed of tungsten having a relatively high electrical resistivity, and the second metal lines 240a, 240b and 240c may be formed of copper having a relatively low electrical resistivity.

[0070] The first metal lines 230a, 230b and 230c and the second metal lines 240a, 240b and 240c are illustrated and described in the present embodiments. However, embodiments are not limited thereto. In some embodiments, at least one or more additional metal lines may further be formed on the second metal lines 240a, 240b and 240c. In this case, the second metal lines 240a, 240b and 240c may be formed of aluminum, and at least some of the additional metal lines formed on the second metal lines 240a, 240b and 240c may be formed of copper having an electrical resistivity lower than that of aluminum of the second metal lines 240a, 240b and 240c.

[0071] The interlayer insulating layer 215 may be arranged on the first substrate 210 and may include an insulating material such as, but not limited to, silicon oxide and/or silicon nitride.

[0072] Each of the first and second cell regions CELL1 and CELL2 may include at least one memory block. The first cell region CELL1 may include a second substrate 310 and a common source line 320. A plurality of word lines 330 (e.g., 331 to 338) may be stacked on the second substrate 310 in a direction (e.g., the Z-axis direction) perpendicular to a top

surface of the second substrate 310. String select lines and a ground select line may be arranged on and under the word lines 330, and the plurality of word lines 330 may be arranged between the string select lines and the ground select line. Similarly, the second cell region CELL2 may include a third substrate 410 and a common source line 420, and a plurality of word lines 430 (431 to 438) may be stacked on the third substrate 410 in a direction (e.g., the Z-axis direction) perpendicular to a top surface of the third substrate 410. Each of the second substrate 310 and the third substrate 410 may be formed of at least one of various materials and may be, for example, a silicon substrate, a silicon-germanium substrate, a germanium substrate, or a substrate having a single-crystalline epitaxial layer grown on a single-crystalline silicon substrate. A plurality of channel structures CH may be formed in each of the first and second cell regions CELL1 and CELL2.

[0073] In some embodiments, as illustrated in a region A1, the channel structure CH may be provided in the bit line bonding region BLBA and may extend in the direction perpendicular to the top surface of the second substrate 310 to penetrate the word lines 330, the string select lines, and the ground select line. The channel structure CH may include a data storage layer, a channel layer, and a filling insulation layer. The channel layer may be electrically connected to a first metal line 350c and a second metal line 360c in the bit line bonding region BLBA. For example, the second metal line 360c may be a bit line and may be connected to the channel structure CH through the first metal line 350c. The bit line 360c may extend in a first direction (e.g., a Y-axis direction) parallel to the top surface of the second substrate 310.

[0074] In some embodiments, as illustrated in a region A2, the channel structure CH may include a lower channel LCH and an upper channel UCH, which are connected to each other. For example, the channel structure CH may be formed by a process of forming the lower channel LCH and a process of forming the upper channel UCH. The lower channel

LCH may extend in the direction perpendicular to the top surface of the second substrate 310 to penetrate the common source line 320 and lower word lines 331 and 332. The lower channel LCH may include a data storage layer, a channel layer, and a filling insulation layer and may be connected to the upper channel UCH. The upper channel UCH may penetrate upper word lines 333 to 338. The upper channel UCH may include a data storage layer, a channel layer, and a filling insulation layer, and the channel layer of the upper channel UCH may be electrically connected to the first metal line 350c and the second metal line 360c. As a length of a channel increases, due to characteristics of manufacturing processes, it may be difficult to form a channel having a substantially uniform width. The memory device 50 according to the present embodiments may include a channel having improved width uniformity due to the lower channel LCH and the upper channel UCH which are formed by the processes performed sequentially.

[0075] In the case in which the channel structure CH includes the lower channel LCH and the upper channel UCH as illustrated in the region A2, a word line located near to a boundary between the lower channel LCH and the upper channel UCH may be a dummy word line. For example, the word lines 332 and 333 adjacent to the boundary between the lower channel LCH and the upper channel UCH may be the dummy word lines. In this case, data may not be stored in memory cells connected to the dummy word line. Alternatively or additionally, the number of pages corresponding to the memory cells connected to the dummy word line may be less than the number of pages corresponding to the memory cells connected to a general word line. A level of a voltage applied to the dummy word line may be different from a level of a voltage applied to the general word line, and, as such, may reduce an influence of a non-uniform channel width between the lower and upper channels LCH and UCH on an operation of the memory device.

[0076] In some embodiments, the number of the lower word lines 331 and 332

penetrated by the lower channel LCH is less than the number of the upper word lines 333 to 338 penetrated by the upper channel UCH in the region A2. However, embodiments are not limited thereto. In some embodiments, the number of the lower word lines penetrated by the lower channel LCH may be equal to or more than the number of the upper word lines penetrated by the upper channel UCH. Alternatively or additionally, structural features and connection relation of the channel structure CH arranged in the second cell region CELL2 may be substantially the same as those of the channel structure CH arranged in the first cell region CELL1.

[0077] In the bit line bonding region BLBA, a first through-electrode THV1 may be provided in the first cell region CELL1, and a second through-electrode THV2 may be provided in the second cell region CELL2. As illustrated in FIG. 5, the first through-electrode THV1 may penetrate the common source line 320 and the plurality of word lines 330. In some embodiments, the first through-electrode THV1 may further penetrate the second substrate 310. The first through-electrode THV1 may include a conductive material. Alternatively or additionally, the first through-electrode THV1 may include a conductive material surrounded by an insulating material. The second through-electrode THV2 may have the same shape and structure as the first through-electrode THV1.

[0078] In some embodiments, the first through-electrode THV1 and the second through-electrode THV2 may be electrically connected to each other through a first through-metal pattern 372d and a second through-metal pattern 472d. The first through-metal pattern 372d may be formed at a bottom end of the first upper chip including the first cell region CELL1, and the second through-metal pattern 472d may be formed at a top end of the second upper chip including the second cell region CELL2. The first through-electrode THV1 may be electrically connected to the first metal line 350c and the second metal line 360c. A lower via 371d may be formed between the first through-electrode THV1 and the first through-

metal pattern 372d, and an upper via 471d may be formed between the second through-electrode THV2 and the second through-metal pattern 472d. The first through-metal pattern 372d and the second through-metal pattern 472d may be connected to each other by the bonding method.

[0079] Alternatively or additionally, in the bit line bonding region BLBA, an upper metal pattern 252 may be formed in an uppermost metal layer of the peripheral circuit region PERI, and an upper metal pattern 392 having the same shape as the upper metal pattern 252 may be formed in an uppermost metal layer of the first cell region CELL1. The upper metal pattern 392 of the first cell region CELL1 and the upper metal pattern 252 of the peripheral circuit region PERI may be electrically connected to each other by the bonding method. In the bit line bonding region BLBA, the bit line 360c may be electrically connected to a page buffer included in the peripheral circuit region PERI. For example, some of the circuit elements 220c of the peripheral circuit region PERI may constitute the page buffer, and the bit line 360c may be electrically connected to the circuit elements 220c constituting the page buffer through an upper bonding metal pattern 370c of the first cell region CELL1 and an upper bonding metal pattern 270c of the peripheral circuit region PERI.

[0080] Continuing to refer to FIG. 5, in the word line bonding region WLBA, the word lines 330 of the first cell region CELL1 may extend in a second direction (e.g., an X-axis direction) parallel to the top surface of the second substrate 310 and may be connected to a plurality of cell contact plugs 340 (e.g., 341 to 347). First metal lines 350b and second metal lines 360b may be sequentially connected onto the cell contact plugs 340 connected to the word lines 330. In the word line bonding region WLBA, the cell contact plugs 340 may be connected to the peripheral circuit region PERI through upper bonding metal patterns 370b of the first cell region CELL1 and upper bonding metal patterns 270b of the peripheral circuit region PERI.

[0081] The cell contact plugs 340 may be electrically connected to a row decoder included in the peripheral circuit region PERI. For example, some of the circuit elements 220b of the peripheral circuit region PERI may constitute the row decoder, and the cell contact plugs 340 may be electrically connected to the circuit elements 220b constituting the row decoder through the upper bonding metal patterns 370b of the first cell region CELL1 and the upper bonding metal patterns 270b of the peripheral circuit region PERI. In some embodiments, an operating voltage of the circuit elements 220b constituting the row decoder may be different from an operating voltage of the circuit elements 220c constituting the page buffer. For example, the operating voltage of the circuit elements 220c constituting the page buffer may be greater than the operating voltage of the circuit elements 220b constituting the row decoder.

[0082] Similarly, in the word line bonding region WLBA, the word lines 430 of the second cell region CELL2 may extend in the second direction (e.g., the X-axis direction) parallel to the top surface of the third substrate 410 and may be connected to a plurality of cell contact plugs 440 (e.g., 441 to 447). The cell contact plugs 440 may be connected to the peripheral circuit region PERI through an upper metal pattern of the second cell region CELL2 and lower and upper metal patterns and a cell contact plug 348 of the first cell region CELL1.

[0083] In the word line bonding region WLBA, the upper bonding metal patterns 370b may be formed in the first cell region CELL1, and the upper bonding metal patterns 270b may be formed in the peripheral circuit region PERI. The upper bonding metal patterns 370b of the first cell region CELL1 and the upper bonding metal patterns 270b of the peripheral circuit region PERI may be electrically connected to each other by the bonding method. The upper bonding metal patterns 370b and the upper bonding metal patterns 270b may be formed of aluminum, copper, or tungsten.

[0084] In the external pad bonding region PA, a lower metal pattern 371e may be formed in a lower portion of the first cell region CELL1, and an upper metal pattern 472a may be formed in an upper portion of the second cell region CELL2. The lower metal pattern 371e of the first cell region CELL1 and the upper metal pattern 472a of the second cell region CELL2 may be connected to each other by the bonding method in the external pad bonding region PA. Similarly, an upper metal pattern 372a may be formed in an upper portion of the first cell region CELL1, and an upper metal pattern 272a may be formed in an upper portion of the peripheral circuit region PERI. The upper metal pattern 372a of the first cell region CELL1 and the upper metal pattern 272a of the peripheral circuit region PERI may be connected to each other by the bonding method.

[0085] Common source line contact plugs 380 and 480 may be disposed in the external pad bonding region PA. The common source line contact plugs 380 and 480 may be formed of a conductive material such as a metal, a metal compound, and/or doped polysilicon. The common source line contact plug 380 of the first cell region CELL1 may be electrically connected to the common source line 320, and the common source line contact plug 480 of the second cell region CELL2 may be electrically connected to the common source line 420. A first metal line 350a and a second metal line 360a may be sequentially stacked on the common source line contact plug 380 of the first cell region CELL1, and a first metal line 450a and a second metal line 460a may be sequentially stacked on the common source line contact plug 480 of the second cell region CELL2.

[0086] Input/output pads 205, 405 and 406 may be arranged in the external pad bonding region PA. Referring to FIG. 5, a lower insulating layer 201 may cover a bottom surface of the first substrate 210, and a first input/output pad 205 may be formed on the lower insulating layer 201. The first input/output pad 205 may be connected to at least one of a plurality of the circuit elements 220a disposed in the peripheral circuit region PERI through a

first input/output contact plug 203 and may be separated from the first substrate 210 by the lower insulating layer 201. Alternatively or additionally, a side insulating layer may be arranged between the first input/output contact plug 203 and the first substrate 210 to electrically isolate the first input/output contact plug 203 from the first substrate 210.

[0087] An upper insulating layer 401 covering a top surface of the third substrate 410 may be formed on the third substrate 410. A second input/output pad 405 and/or a third input/output pad 406 may be arranged on the upper insulating layer 401. The second input/output pad 405 may be connected to at least one of the plurality of circuit elements 220a arranged in the peripheral circuit region PERI through second input/output contact plugs 403 and 303, and the third input/output pad 406 may be connected to at least one of the plurality of circuit elements 220a arranged in the peripheral circuit region PERI through third input/output contact plugs 404 and 304.

[0088] In some embodiments, the third substrate 410 may not be arranged in a region in which the input/output contact plug is arranged. For example, as illustrated in a region B, the third input/output contact plug 404 may be separated from the third substrate 410 in a direction parallel to the top surface of the third substrate 410 and may penetrate an interlayer insulating layer 415 of the second cell region CELL2 so as to be connected to the third input/output pad 406. In this case, the third input/output contact plug 404 may be formed by at least one of various processes.

[0089] In some embodiments, as illustrated in a region B1, the third input/output contact plug 404 may extend in a third direction (e.g., the Z-axis direction), and a diameter of the third input/output contact plug 404 may become progressively greater toward the upper insulating layer 401. That is, a diameter of the channel structure CH described in the region A1 may become progressively less toward the upper insulating layer 401, but the diameter of the third input/output contact plug 404 may become progressively greater toward the upper

insulating layer 401. For example, the third input/output contact plug 404 may be formed after the second cell region CELL2 and the first cell region CELL1 are bonded to each other by the bonding method.

[0090] In some embodiments, as illustrated in a region B2, the third input/output contact plug 404 may extend in the third direction (e.g., the Z-axis direction), and a diameter of the third input/output contact plug 404 may become progressively less toward the upper insulating layer 401.That is, like the channel structure CH, the diameter of the third input/output contact plug 404 may become progressively less toward the upper insulating layer 401. For example, the third input/output contact plug 404 may be formed together with the cell contact plugs 440 before the second cell region CELL2 and the first cell region CELL1 are bonded to each other.

[0091] In some embodiments, the input/output contact plug may overlap with the third substrate 410. For example, as illustrated in a region C, the second input/output contact plug 403 may penetrate the interlayer insulating layer 415 of the second cell region CELL2 in the third direction (e.g., the Z-axis direction) and may be electrically connected to the second input/output pad 405 through the third substrate 410. In this case, a connection structure of the second input/output contact plug 403 and the second input/output pad 405 may be realized by various methods.

[0092] In some embodiments, as illustrated in a region C1, an opening 408 may be formed to penetrate the third substrate 410, and the second input/output contact plug 403 may be connected directly to the second input/output pad 405 through the opening 408 formed in the third substrate 410. In this case, as illustrated in the region C1, a diameter of the second input/output contact plug 403 may become progressively greater toward the second input/output pad 405. However, embodiments are not limited thereto, and in some embodiments, the diameter of the second input/output contact plug 403 may become

progressively less toward the second input/output pad 405.

[0093] In some embodiments, as illustrated in a region C2, the opening 408 penetrating the third substrate 410 may be formed, and a contact 407 may be formed in the opening 408. An end of the contact 407 may be connected to the second input/output pad 405, and another end of the contact 407 may be connected to the second input/output contact plug 403. Thus, the second input/output contact plug 403 may be electrically connected to the second input/output pad 405 through the contact 407 in the opening 408. In this case, as illustrated in the region C2, a diameter of the contact 407 may become progressively greater toward the second input/output pad 405, and a diameter of the second input/output contact plug 403 may become progressively less toward the second input/output pad 405. For example, the second input/output contact plug 403 may be formed together with the cell contact plugs 440 before the second cell region CELL2 and the first cell region CELL1 are bonded to each other, and the contact 407 may be formed after the second cell region CELL2 and the first cell region CELL1 are bonded to each other.

[0094] In some embodiments, as shown in a region C3, a stopper 409 may further be formed on a bottom end of the opening 408 of the third substrate 410, as compared with the embodiments of the region C2. The stopper 409 may be a metal line formed in the same layer as the common source line 420. Alternatively or additionally, the stopper 409 may be a metal line formed in the same layer as at least one of the word lines 430. The second input/output contact plug 403 may be electrically connected to the second input/output pad 405 through the contact 407 and the stopper 409.

[0095] Like the second and third input/output contact plugs 403 and 404 of the second cell region CELL2, a diameter of each of the second and third input/output contact plugs 303 and 304 of the first cell region CELL1 may become progressively less toward the lower metal pattern 371e or may become progressively greater toward the lower metal pattern

371e.

[0096] In some embodiments, a slit 411 may be formed in the third substrate 410. For example, the slit 411 may be formed at a certain position of the external pad bonding region PA. For example, as illustrated in a region 'D', the slit 411 may be located between the second input/output pad 405 and the cell contact plugs 440 when viewed in a plan view. Alternatively or additionally, the second input/output pad 405 may be located between the slit 411 and the cell contact plugs 440 when viewed in a plan view.

[0097] In some embodiments, as illustrated in a region D1, the slit 411 may be formed to penetrate the third substrate 410. For example, the slit 411 may be used to prevent the third substrate 410 from being finely cracked when the opening 408 is formed. However, embodiments are not limited thereto, and in some embodiments, the slit 411 may be formed to have a depth ranging from about 60% to about 70% of a thickness of the third substrate 410.

[0098] In some embodiments, as illustrated in a region D2, a conductive material 412 may be formed in the slit 411. For example, the conductive material 412 may be used to discharge a leakage current occurring in driving of the circuit elements in the external pad bonding region PA to the outside. In this case, the conductive material 412 may be connected to an external ground line.

[0099] In some embodiments, as illustrated in a region D3, an insulating material 413 may be formed in the slit 411. For example, the insulating material 413 may be used to electrically isolate the second input/output pad 405 and the second input/output contact plug 403 arranged in the external pad bonding region PA from the word line bonding region WLBA. Since the insulating material 413 is formed in the slit 411, a voltage provided through the second input/output pad 405 may be prevented from affecting a metal layer

arranged on the third substrate 410 in the word line bonding region WLBA.

[0100] In some embodiments, the first to third input/output pads 205, 405 and 406 may be selectively formed. For example, the memory device 50 may be realized to include only the first input/output pad 205 arranged on the first substrate 210, to include only the second input/output pad 405 arranged on the third substrate 410, or to include only the third input/output pad 406 arranged on the upper insulating layer 401.

[0101] In some embodiments, at least one of the second substrate 310 of the first cell region CELL1 or the third substrate 410 of the second cell region CELL2 may be used as a sacrificial substrate and may be completely or partially removed before or after a bonding process. An additional layer may be stacked after the removal of the substrate. For example, the second substrate 310 of the first cell region CELL1 may be removed before or after the bonding process of the peripheral circuit region PERI and the first cell region CELL1, and then, an insulating layer covering a top surface of the common source line 320 or a conductive layer for connection may be formed. Similarly, the third substrate 410 of the second cell region CELL2 may be removed before or after the bonding process of the first cell region CELL1 and the second cell region CELL2, and then, the upper insulating layer 401 covering a top surface of the common source line 420 or a conductive layer for connection may be formed.

[0102] Referring to FIGS. 1 and 5, with the development of semiconductor process, as the number of stages of memory cells arranged in the memory cell array 11 of the first and second cell regions CELL1 and CELL2 increases (e.g., as the number of stacked word lines WL increases), the area of the memory cell array 11 (e.g., the area of a cell region) decreases. For example, the cell region may be defined as a region in which a plurality of NAND strings (e.g., NS11 to NS33 of FIG. 2) or a plurality of pillars (e.g., P of FIGS. 3A and 3B) are arranged. For another example, the cell region may be defined as a region in which a plurality

of word lines (e.g., WL1 to WL8 of FIGS. 2, 3A, and 3B) are arranged. For another example, the cell region may be defined as a region in which a plurality of bit lines (e.g., BL1, BL2, BL3 of FIGS. 2, 3A, and 3B) are arranged. However, the cell region is not limited thereto, and may be defined as a region including the memory cell array 11.

[0103] Moreover, the area of a peripheral circuit region PERI in which the peripheral circuit PECT is arranged may not decrease as much as does the area of the cell region. Accordingly, in some embodiments, a first peripheral circuit region of the peripheral circuit region PERI overlaps the memory cell array 11 in the vertical direction VD, and a second peripheral circuit region of the peripheral circuit region PERI may not overlap the memory cell array 11 in the vertical direction VD.

[0104] FIG. 6 is a diagram illustrating a memory device 60a according to a comparative example, and a memory device 60b, according to an embodiment.

[0105] Referring to FIG. 6, the memory device 60a according to the comparative example may include a first semiconductor layer 61a in which a memory cell array MCA is arranged, and a second semiconductor layer 62a in which page buffer circuits PGBUF1 and PGBUF2 and row decoders XDEC1 and XDEC2 are arranged. When the memory cell array MCA includes M word lines stacked in the vertical direction, that is, when the memory cell array MCA includes a stack structure of M word lines, the memory cell array MCA may have a first size S1 in the first horizontal direction HD1, where M is an integer greater than 1. Alternatively or additionally, the second semiconductor layer 62a may also have the first size S1 in the first horizontal direction HD1, and accordingly, the memory cell array MCA may be on and overlap the second semiconductor layer 62a. In this case, the area of an overlap region 63a on the second semiconductor layer 62a may correspond to the area of the memory cell array MCA. That is, the size of the overlap region 63a on the second semiconductor layer 62a in the first horizontal direction HD1 may correspond to the first size s1, which is equal to

the size of the memory cell array MCA in the first horizontal direction HD1.

[0106] The memory device 60b, according to some embodiments, may include a first semiconductor layer 61b in which the memory cell array MCA is arranged, and a second semiconductor layer 62b in which the page buffer circuits PGBUF1 and PGBUF2 and the row decoders XDEC1 and XDEC2 are arranged. With the development of semiconductor processing technology, the number of word lines stacked in the vertical direction may increase from M to N, where N is an integer greater than M). Accordingly, when the memory cell array MCA includes N word lines stacked in the vertical direction, that is, when the memory cell array MCA includes a stack structure of N word lines, the area of the memory cell array MCA may decrease. For example, the area of the memory cell array MCA may decrease by 60% compared to the comparative example.

[0107] For another example, the memory cell array MCA may have a second size S2 less than the first size S1 in the first horizontal direction HD1. The second semiconductor layer 62b may have the first size S1 in the first horizontal direction HD1, and accordingly, the memory cell array MCA may be on and overlap a partial region of the second semiconductor layer 62b. In this case, the area of an overlap region 63b on the second semiconductor layer 62b may correspond to the area of the memory cell array MCA. That is, the size of the overlap region 63b on the second semiconductor layer 62b in the first horizontal direction HD1 may correspond to the second size s2, which is equal to the size of the memory cell array MCA in the first horizontal direction HD1.

[0108] The first semiconductor layer 61b may correspond to the first semiconductor layer L1 of FIG. 4 or the cell region CELL1 or CELL2 of FIG. 5, and the second semiconductor layer 62b may correspond to the second semiconductor layer L2 of FIG. 4 or the peripheral circuit region PERI of FIG. 5. As described above, according to some embodiments, the memory cell array MCA may be on and overlap the partial region of the

second semiconductor layer 62b rather than the entire region thereof. For example, the memory cell array MCA may be on and overlap partial regions of the page buffer circuits PGBUF1 and PGBUF2. For example, the memory cell array MCA may be on and overlap partial regions of the row decoders XDEC1 and XDEC2.

[0109] In some embodiments, the memory cell array MCA may be on and overlap partial regions of the page buffer circuits PGBUF1 and PGBUF2 and entire regions of the row decoders XDEC1 and XDEC2. That is, the page buffer circuits PGBUF1 and PGBUF2 may be partially buried by the memory cell array MCA, and the row decoders XDEC1 and XDEC2 may be completely buried by the memory cell array MCA. In some embodiments, the memory cell array MCA may be on and overlap partial regions of the page buffer circuits PGBUF1 and PGBUF2 and the entire region of one of the row decoders XDEC1 and XDEC2. That is, the page buffer circuits PGBUF1 and PGBUF2 may be partially buried by the memory cell array MCA, and one of the row decoders XDEC1 and XDEC2 may be completely buried by the memory cell array MCA.

[0110] In some embodiments, the memory cell array MCA may be on and overlap the entire regions of the page buffer circuits PGBUF1 and PGBUF2 and partial regions of the row decoders XDEC1 and XDEC2. That is, the page buffer circuits PGBUF1 and PGBUF2 may be completely buried by the memory cell array MCA, and the row decoders XDEC1 and XDEC2 may be partially buried by the memory cell array MCA. Alternatively or additionally, the memory cell array MCA may be on and overlap the entire region of one of the page buffer circuits PGBUF1 and PGBUF2 and partial regions of the row decoders XDEC1 and XDEC2. That is, one of the page buffer circuits PGBUF1 and PGBUF2 may be completely buried by the memory cell array MCA, and the row decoders XDEC1 and XDEC2 may be partially buried by the memory cell array MCA.

[0111] FIGS. 7A and 7B are diagrams illustrating memory devices 70a and 70b,

respectively, according to some embodiments. The memory devices 70a and 70b correspond to modifications of the memory device 60b of FIG. 6, and the descriptions provided above with reference to FIG. 6 may also be applied to the present embodiments.

[0112] Referring to FIG. 7A, the memory device 70a may include a first semiconductor layer 71a in which the memory cell array MCA and the page buffer circuits PGBUF1 and PGBUF2 are arranged, and a second semiconductor layer 72a in which the row decoders XDEC1 and XDEC2 are arranged. The memory cell array MCA may be on and overlap a partial region of the second semiconductor layer 72a. In this case, the size of an overlap region 73a on the second semiconductor layer 72a may correspond to the second size S2 of the memory cell array MCA. In some embodiments, some components of the page buffer circuits PGBUF1 and PGBUF2 may be arranged in the first semiconductor layer 71a, and the remaining components of the page buffer circuits PGBUF1 and PGBUF2 may be arranged in the second semiconductor layer 72a. For example, a high-voltage unit (e.g., HV of FIG. 8) and/or a page buffer (e.g., PB of FIG. 8) may be arranged in the first semiconductor layer 71a, and a cache unit (e.g., the CU of FIG. 8) and/or a page buffer decoder (e.g., PBDEC of FIG. 9) may be arranged in the second semiconductor layer 72a. In some embodiments, the page buffer circuit PGBUF1 may be arranged in the first semiconductor layer 71a, and the page buffer circuit PGBUF2 may be arranged in the second semiconductor layer 72a.

[0113] In some embodiments, the memory cell array MCA may be on and overlap partial regions of the row decoders XDEC1 and XDEC2, and accordingly, the row decoders XDEC1 and XDEC2 may be partially buried by the memory cell array MCA. In some embodiments, the memory cell array MCA may be on and overlap one of the row decoders XDEC1 and XDEC2, and accordingly, the one of the row decoders XDEC1 and XDEC2 may be completely buried by the memory cell array MCA, and the other one of the row decoders

XDEC1 and XDEC2 may not be buried by the memory cell array MCA. In some embodiments, the memory cell array MCA may be on and overlap a partial region of one of the row decoders XDEC1 and XDEC2, and accordingly, the one of the row decoders XDEC1 and XDEC2 may be partially buried by the memory cell array MCA, and the other one of the row decoders XDEC1 and XDEC2 may be completely buried by the memory cell array MCA.

[0114] Referring to FIG. 7B, the memory device 70b may include a first semiconductor layer 71b in which the memory cell array MCA and the row decoders XDEC1 and XDEC2 are arranged, and a second semiconductor layer 72b in which the page buffer circuits PGBUF1 and PGBUF2 are arranged. The memory cell array MCA may be on and overlap a partial region of the second semiconductor layer 72b. In this case, the size of an overlap region 73b on the second semiconductor layer 72b may correspond to the second size S2 of the memory cell array MCA. In some embodiments, some components of the row decoders XDEC1 and XDEC2 may be arranged in the first semiconductor layer 71b, and the remaining components of the row decoders XDEC1 and XDEC2 may be arranged in the second semiconductor layer 72b. For example, a pass transistor circuit (e.g., 101 of FIG. 10) may be arranged in the first semiconductor layer 71b, and a row decoder (e.g., 102 of FIG. 10) may be arranged in the second semiconductor layer 72b. In some embodiments, the row decoder XDEC1 may be arranged in the first semiconductor layer 71a, and the row decoder XDEC2 may be arranged in the second semiconductor layer 72a.

[0115] In some embodiments, the memory cell array MCA may be on and overlap partial regions of the page buffer circuits PGBUF1 and PGBUF2, and accordingly, the page buffer circuits PGBUF1 and PGBUF2 may be partially buried by the memory cell array MCA. In some embodiments, the memory cell array MCA may be on and overlap one of the page buffer circuits PGBUF1 and PGBUF2, and accordingly, the one of the page buffer

circuits PGBUF1 and PGBUF2 may be completely buried by the memory cell array MCA, and the other one of the page buffer circuits PGBUF1 and PGBUF2 may not be buried by the memory cell array MCA. In some embodiments, the memory cell array MCA may be on and overlap a partial region of one of the page buffer circuits PGBUF1 and PGBUF2, and accordingly, the one of the page buffer circuits PGBUF1 and PGBUF2 may be partially buried by the memory cell array MCA, and the other one of the page buffer circuits PGBUF1 and PGBUF2 may be completely buried by the memory cell array MCA.

[0116] FIG. 8 is a circuit diagram illustrating a page buffer circuit PGBUF according to an embodiment.

[0117] Referring to FIG. 8, the page buffer circuit PGBUF may correspond to one of the page buffer circuits PGBUF1 and PGBUF2 of FIG. 6, and may correspond to one of the plurality of page buffers PB of FIG. 1. The page buffer circuit PGBUF may include a high-voltage unit HV, a page buffer PB, and a cache unit CU, and the cache unit CU may include a cache latch (C-LATCH) CL.

[0118] The high-voltage unit HV may include a bit line select transistor TR_hv connected to a bit line BL and driven by a bit line select signal BLSLT. The bit line select transistor TR_hv may be implemented as a “high-voltage transistor” and may be arranged in a well region other than that of the page buffer PB. According to some embodiments, the bit line select transistor TR_hv may be referred to as a bit line select switch or a high-voltage switch.

[0119] The page buffer PB may include a sensing latch (S-LATCH) SL, a force latch (F-LATCH) FL, an upper-bit latch (M-LATCH) ML and a lower-bit latch (L-LATCH) LL. According to some embodiments, the S-LATCH SL, the F-LATCH FL, the M-LATCH ML, or the L-LATCH LL may be referred to as a “main latch”. Alternatively or additionally, the

page buffer PB may further include a precharge circuit capable of controlling a precharge operation on the bit line BL or a sensing node SO based on a bit line clamping control signal, and may further include a transistor driven by a bit line setup signal.

[0120] The S-LATCH SL may store, in a read operation or a program verify operation, data stored in a memory cell or a result of sensing a threshold voltage of the memory cell. Alternatively or additionally, the S-LATCH SL may be used to apply, in a program operation, a program bit line voltage or a program inhibit voltage to the bit line BL. The F-LATCH FL may be used to store, in a program operation, force data and improve threshold voltage distribution. After the force data is initially set to '1', the force data may be converted to '0' when the threshold voltage of the memory cell enters a forcing region that has a voltage less than that of a target region. The M-LATCH ML, the L-LATCH LL, and the C-LATCH CL may be used to store, in a program operation, data input from an external source. In a read operation, the C-LATCH CL may receive, from the S-LATCH SL, data read from a memory cell and output the data to the outside through a data input/output line.

[0121] The page buffer PB may further include first to fourth transistors NM1 to NM4. The first transistor NM1 may be connected between the sensing node SO and the S-LATCH SL, and may be driven by a ground control signal SOGND. The second transistor NM2 may be connected between the sensing node SO and the F-LATCH FL, and may be driven by a forcing monitoring signal MON_F. The third transistor NM3 may be connected between the sensing node SO and the M-LATCH ML, and may be driven by an upper-bit monitoring signal MON_M. The fourth transistor NM4 may be connected between the sensing node SO and the L-LATCH LL and may be driven by a lower-bit monitoring signal MON_L.

[0122] The page buffer PB may further include fifth and sixth transistors NM5 and NM6 connected in series between the bit line select transistor TR_hv and the sensing node

SO. The fifth transistor NM5 may be driven by a bit line shut-off signal BLSHF, and the sixth transistor NM6 may be driven by a bit line connection control signal CLBLK. Alternatively or additionally, the page buffer PB may further include a precharge transistor PM. The precharge transistor PM is connected to the sensing node SO, is driven by a load signal LOAD, and precharges the sensing node SO to a precharge level in a precharge period.

[0123] The cache unit CU may include the C-LATCH CL and a seventh transistor NM7. The seventh transistor NM7 may be connected between the sensing node SO and the C-LATCH CL, and may be driven by a cache monitoring signal MON_C. The C-LATCH CL may be connected to the data input/output line, and accordingly, the cache unit CU may be arranged adjacent to the data input/output line. As such, the page buffer PB and the cache unit CU may be arranged to be spaced apart from each other, and the page buffer circuit PGBUF may have a structure in which the page buffer PB and the cache unit CU are separated from each other.

[0124] In some embodiments, the page buffer PB of the page buffer circuit PGBUF may be buried by a cell region in which a memory cell array is arranged, and thus overlap the cell region in a vertical direction, whereas the high-voltage unit HV and the cache unit CU may not be buried by the cell region, and thus not overlap the cell region in the vertical direction. In some embodiments, the high-voltage unit HV of the page buffer circuit PGBUF may be buried by the cell region and thus overlap the cell region in the vertical direction, whereas the page buffer PB and the cache unit CU may not be buried by the cell region, and thus not overlap the cell region in the vertical direction. In some embodiments, the page buffer PB and the high-voltage unit HV of the page buffer circuit PGBUF may be buried by the cell region and thus overlap the cell region in the vertical direction, whereas the cache unit CU may not be buried by the cell region, and thus not overlap the cell region in the vertical direction. In some embodiments, the page buffer PB, the high-voltage unit HV, and

the cache unit CU of the page buffer circuit PGBUF may be buried by the cell region and thus overlap the cell region in the vertical direction.

[0125] FIG. 9 is a circuit diagram illustrating a page buffer decoder PBDEC according to an embodiment.

[0126] Referring to FIG. 9, the page buffer decoder PBDEC may include a plurality of page buffer decoders for addressing and driving a memory cell array, for example, first and second page buffer decoders 91 and 92. The first page buffer decoder 91 may include a first inverter 911 and transistors N1, N2, and N3. The first inverter 911 may receive a first page buffer signal PBS1 from a first page buffer circuit (e.g., PGBUF of FIG. 8), and an output of the first inverter 911 may be provided to the gate of the transistor N1. The source of the transistor N1 may be connected to a ground terminal, and the drain of the transistor N1 may be connected to the transistor N2. The transistors N2 and N3 are connected to each other in series, and a reference current signal REF_CUR is applied to the gate of the transistor N3. The second page buffer decoder 92 may include an inverter 921 and transistors N1a, N2a, and N3a, and may receive a second page buffer PBS2 from a second page buffer circuit. The description of the first page buffer decoder 91 may be applied to the second page buffer decoder 92, and thus will be omitted.

[0127] Referring to FIGS. 8 and 9, for example, when a memory cell connected to the page buffer circuit PGBUF is program-failed, a logic low level may be stored in the S-LATCH SL of the page buffer PB, and in this case, the first page buffer signal PBS1 may be at a logic low level that is the voltage level of the sensing node SO. In this case, the first inverter 911 may output a logic high signal, accordingly, the transistor N1 may be turned on, and the page buffer decoder 91 may operate as a current sink. The transistor N3 may output a first signal, that is, a reference current, to a wired OR terminal WOR_OUT based on the reference current signal REF_CUR. Here, the reference current may correspond to a current

flowing through the transistor N3 when the transistor N3 is turned on according to the reference current signal REF_CUR.

[0128] For example, each of the page buffer circuit 12 of FIG. 1 and the page buffer circuits PGBUF1 and PGBUF2 of FIGS. 6, 7A, and 7B may include the page buffer circuit PGBUF of FIG. 8. For example, each of the page buffer circuit 12 of FIG. 1 and the page buffer circuits PGBUF1 and PGBUF2 of FIGS. 6, 7A, and 7B may include the page buffer circuit PGBUF of FIG. 8 and the page buffer decoder PBDEC of FIG. 9. Hereinafter, according to some embodiments, the page buffer decoder PBDEC may be described as being included in the page buffer circuit, and the page buffer decoder PBDEC may be described as being arranged outside the page buffer circuit.

[0129] Referring to FIGS. 8 and 9, in some embodiments, the page buffer PB may be buried by a cell region in which a memory cell array is arranged, and thus overlap the cell region in a vertical direction, whereas the high-voltage unit HV, the cache unit CU, and the page buffer decoder PBDEC may not be buried by the cell region, and thus not overlap the cell region in the vertical direction. In some embodiments, the high-voltage unit HV may be buried by the cell region and thus overlap the cell region in the vertical direction, whereas the page buffer PB, the cache unit CU, and the page buffer decoder PBDEC may not be buried by the cell region and thus not overlap the cell region in the vertical direction. In some embodiments, the page buffer PB and the high-voltage unit HV may be buried by a cell region in which a memory cell array is arranged, and thus overlap the cell region in the vertical direction, whereas the cache unit CU and the page buffer decoder PBDEC may not be buried by the cell region and thus not overlap the cell region in the vertical direction. In some embodiments, the page buffer PB, the high-voltage unit HV, and the cache unit CU may be buried by a cell region in which a memory cell array is arranged, and thus overlap the cell region in the vertical direction, whereas the page buffer decoder PBDEC may not be buried

by the cell region and thus not overlap the cell region in the vertical direction.

[0130] FIG. 10 is a diagram illustrating a pass transistor circuit 101 and a row decoder 102 according to an embodiment.

[0131] Referring to FIG. 10, a memory device 100 may include the memory block BLK, the pass transistor circuit 101, and the row decoder 102. The row decoder 102 may include a block decoder 102a and a driving signal line decoder 102b. For example, each of the row decoder 13 of FIG. 1 and the row decoders XDEC1 and XDEC2 of FIGS. 6, 7A, and 7B may include the row decoder 102. For example, each of the row decoder 13 of FIG. 1 and the row decoders XDEC1 and XDEC2 of FIGS. 6, 7A, and 7B may include the pass transistor circuit 101 and the row decoder 102.

[0132] The pass transistor circuit 101 may include a plurality of pass transistors TRg, TR1 to TRn, and TRs. The block decoder 102a may be connected to the pass transistor circuit 101 through a block select signal line BS. The block select signal line BS may be connected to gates of the plurality of pass transistors TRg, TR1 to TRn, and TRs. For example, when a block select signal provided through the block select signal line BS is activated, the plurality of pass transistors TRg, TR1 to TRn, and TRs may be turned on, and accordingly, the memory block BLK may be selected.

[0133] The driving signal line decoder 102b may be connected to the pass transistor circuit 101 through a ground select line driving signal line GS, word line driving signal lines SI1 to SIn, and a string select line driving signal line SS. For example, the ground select line driving signal line GS, the word line driving signal lines SI1 to SIn, and the string select line driving signal line SS may be connected to sources of the plurality of pass transistors TRg, TR1 to TRn, and TRs, respectively.

[0134] The pass transistor circuit 101 may be connected to the memory block BLK

through a ground select line GSL, word lines WL1 to WLn, and a string select line SSL. The pass transistor TRg may be connected between the ground select line driving signal line GS and the ground select line GSL. The plurality of pass transistors TR1 to TRn may be respectively connected between the word line driving signal lines SI1 to SIn and the plurality of word lines WL1 to WLn. The pass transistor TRs may be connected between the string select line driving signal line SS and the string select line SSL. For example, when a block select signal is activated, the plurality of pass transistors TRg, TR1 to TRn, and TRs may provide the ground select line GSL, the word lines WL1 to WLn, and the string select line SSL with driving signals provided through the ground select line driving signal line GS, the word line driving signal lines SI1 to SIn, and the string select line driving signal line SS, respectively.

[0135] FIGS. 11A to 11D are diagrams illustrating memory devices 110a, 110b, 110c, and 110d, respectively, according to some embodiments.

[0136] Referring to FIG. 11A, the memory device 110a may include a first semiconductor layer 111a and a second semiconductor layer 112a, the first semiconductor layer 111a may include the memory cell array MCA, and the second semiconductor layer 112a may include the page buffers PB, the high-voltage unit HV, the C-LATCH CL, the page buffer decoder PBDEC, and a row decoder XDEC. The page buffers PB, the high-voltage unit HV, the C-LATCH CL, and the page buffer decoder PBDEC may correspond to, for example, the page buffer circuits PGBUF1 and PGBUF2 of FIGS. 6, 7A, and 7B, the row decoder XDEC may correspond to, for example, the row decoders XDEC1 and XDEC2 of FIGS. 6, 7A, and 7B, and this may be equally applied to the following embodiments.

[0137] The area of a cell region in which the memory cell array MCA is arranged may be smaller than the area of the first semiconductor layer 111a, and the area of a peripheral circuit region in which a peripheral circuit including the page buffers PB, the high-

voltage unit HV, the C-LATCH CL, the page buffer decoder PBDEC, and the row decoder XDEC is arranged may be similar to the area of the second semiconductor layer 112a. In some embodiments, in the first semiconductor layer 111a, an insulating layer may be arranged in a region in which the memory cell array MCA is not arranged. Alternatively or additionally, in the first semiconductor layer 111a, a wiring structure including a plurality of metal layers may be arranged in a region in which the memory cell array MCA is not arranged. In some embodiments, in the first semiconductor layer 111a, some elements of a peripheral circuit (e.g., PECT of FIG. 1) may be arranged in a region in which the memory cell array MCA is not arranged. This may be equally applied to the following embodiments.

[0138] In some embodiments, the memory cell array MCA may be on and overlap the page buffers PB and the high-voltage unit HV. As such, a portion of the page buffer circuit, for example, the page buffers PB and the high-voltage unit HV may be buried by the memory cell array MCA, and the remaining portions of the page buffer circuit, for example, the C-LATCH CL and the page buffer decoder PBDEC may not be buried by the memory cell array MCA. Alternatively or additionally, the row decoder XDEC may not be buried by the memory cell array MCA.

[0139] As such, the second semiconductor layer 112a may include a first peripheral circuit region in which the page buffers PB and the high-voltage unit HV are arranged, and a second peripheral circuit region in which the C-LATCH CL, the page buffer decoder PBDEC, and the row decoder XDEC are arranged. The first peripheral circuit region may overlap, in the vertical direction, the cell region in which the memory cell array MCA is arranged, and the second peripheral circuit region may not overlap, in the vertical direction, the cell region in which the memory cell array MCA is arranged.

[0140] In some embodiments, the second semiconductor layer 112a may further include a control logic circuit (e.g., 14 of FIG. 1) and/or a voltage generator (e.g., 15 of FIG.

1) arranged adjacent to the page buffer PB, and the control logic circuit and/or the voltage generator may be arranged adjacent to the page buffer PB in the first peripheral circuit region. In some embodiments, the second semiconductor layer 112a may further include a macrocell logic arranged adjacent to the C-LATCH CL, the page buffer decoder PBDEC, and the row decoder XDEC, and the macrocell logic may be arranged in the second peripheral circuit region, that is, may not overlap the memory cell array MCA in the vertical direction. For example, the macrocell logic may include a row decoder driving logic or a page buffer driving logic.

[0141] Referring to FIG. 11B, the memory device 110b may include a first semiconductor layer 111b and a second semiconductor layer 112b, and may correspond to a modification of the memory device 110a of FIG. 11A. In the memory device 110a of FIG. 11A, the page buffer circuit may be implemented to be partially buried, whereas in the memory device 110b, according to some embodiments, the page buffer circuit may be implemented to be completely buried. The memory cell array MCA may be on and overlap the page buffers PB, the high-voltage unit HV, the C-LATCH CL, and the page buffer decoder PBDEC. As such, the entire page buffer circuit of the second semiconductor layer 112b may be buried by the memory cell array MCA. The row decoder XDEC may not be buried by the memory cell array MCA, but the present disclosure is not limited thereto, and in some embodiments, the row decoder XDEC may also be buried by the memory cell array MCA.

[0142] Referring to FIG. 11C, the memory device 110c may include a first semiconductor layer 111c and a second semiconductor layer 112c, and may correspond to a modification of the memory device 110a of FIG. 11A. In the memory device 110c, the row decoder XDEC may be implemented to be completely buried, and the page buffer circuit may be implemented to be partially buried. For example, the memory cell array MCA may be on

and overlap the page buffers PB, the high-voltage unit HV, and the row decoder XDEC.

[0143] Referring to FIG. 11D, the memory device 110d may include a first semiconductor layer 111d and a second semiconductor layer 112d, and may correspond to a modification of the memory device 110c of FIG. 11C. In the memory device 110d, the row decoder XDEC may be implemented to be partially buried, and the page buffer circuit may also be implemented to be partially buried. For example, the memory cell array MCA may be on and overlap the page buffers PB, the high-voltage unit HV, and a partial region of the row decoder XDEC. For example, the memory cell array MCA may be on and overlap a pass transistor circuit included in the row decoder XDEC. For example, the memory cell array MCA may be on and overlap a ground select line driver and a string select line driver included in the row decoder XDEC. For example, the memory cell array MCA may be on and overlap a word line driver included in the row decoder XDEC.

[0144] In some embodiments, when a memory device includes a plurality of memory cell arrays, some memory cell arrays and corresponding peripheral circuits may be arranged as illustrated in FIG. 11A, and the remaining memory cell arrays and corresponding peripheral circuits may be arranged as illustrated in at least one of FIGS. 11B, 11C, and 11D. However, the present disclosure is not limited thereto, and in some embodiments, when the memory device includes a plurality of memory cell arrays, the plurality of memory cell arrays and corresponding peripheral circuits may be arranged as illustrated in FIG. 11A, 11B, 11C, or 11D. These various embodiments are described with reference to FIGS. 12A to 12F.

[0145] FIG. 12A is a diagram illustrating a memory device 120a according to an embodiment.

[0146] Referring to FIG. 12A, the memory device 120a may include a first semiconductor layer 121a and a second semiconductor layer 122a, and first to fourth memory

cell arrays MCA1, MCA2, MCA3, and MCA4 may be arranged in the first semiconductor layer 121a. According to some embodiments, the first to fourth memory cell arrays MCA1, MCA2, MCA3, and MCA4 may be referred to as a memory plane or MAT. The second semiconductor layer 122a may include the page buffers PB, the high-voltage unit HV, the C-LATCH CL, the page buffer decoder PBDEC, and the row decoder XDEC, which correspond to each of the first to fourth memory cell arrays MCA1, MCA2, MCA3, and MCA4. Alternatively or additionally, the second semiconductor layer 122a may further include a pad region PA. In some embodiments, the pad region PA may be arranged in an edge region or a bottom region of the second semiconductor layer 122a, and may include a plurality of bonding pads PD arranged in the second horizontal direction HD2. In this case, the pad region PA may not be buried by cell overlap regions C_OVR, that is, may not overlap the cell overlap regions C_OVR in the vertical direction.

[0147] In some embodiments, the first to fourth memory cell arrays MCA1, MCA2, MCA3, and MCA4 and corresponding peripheral circuits may be implemented as illustrated in FIG. 11A. For example, each of the first to fourth memory cell arrays MCA1, MCA2, MCA3, and MCA4 may be on the corresponding page buffers PB and high-voltage unit HV. That is, the page buffers PB and the high-voltage unit HV of the second semiconductor layer 122a may be partially buried by the cell overlap region C_OVR, and the C-LATCH CL, the page buffer decoder PBDEC, and the row decoder XDEC of the second semiconductor layer 122a may not be buried by the cell overlap region C_OVR.

[0148] In some embodiments, the peripheral circuits arranged under some of the first to fourth memory cell arrays MCA1, MCA2, MCA3, and MCA4 may be partially buried, and the peripheral circuits arranged under the remaining memory cell arrays may be completely buried. In some embodiments, a relatively large number of elements may be buried in the peripheral circuits arranged under some of the first to fourth memory cell arrays MCA1,

MCA2, MCA3, and MCA4, and a relatively small number of elements may be buried in the peripheral circuits arranged under the remaining memory cell arrays. For example, the cell overlap regions C_OVR respectively corresponding to the first to fourth memory cell arrays MCA1, MCA2, MCA3, and MCA4 may have different sizes.

[0149] FIG. 12B is a diagram illustrating a memory device 120b according to an embodiment.

[0150] Referring to FIG. 12B, the memory device 120b may include a first semiconductor layer 121b and a second semiconductor layer 122b. The memory device 120b corresponds to a modification of the memory device 120a of FIG. 12A, and hereinafter, differences between the memory device 120b and the memory device 120a of FIG. 12A will be mainly described. In some embodiments, the pad region PA may be arranged in a center region of the second semiconductor layer 122b, and may include the plurality of bonding pads PD arranged in the second horizontal direction HD2. For example, the pad region PA may extend between the first memory cell array MCA1 and the third memory cell array MCA3, and between the second memory cell array MCA2 and the fourth memory cell array MCA4, in the second horizontal direction HD2. In this case, the pad region PA may not be buried by the cell overlap regions C_OVR, that is, may not overlap the cell overlap regions C_OVR in the vertical direction.

[0151] FIG. 12C is a diagram illustrating a memory device 120c according to an embodiment.

[0152] Referring to FIG. 12C, the memory device 120c may include a first semiconductor layer 121c and a second semiconductor layer 122c. The memory device 120c corresponds to a modification of the memory device 120a of FIG. 12A, and hereinafter, differences between the memory device 120c and the memory device 120a of FIG. 12A will

be mainly described. In some embodiments, the first and second memory cell arrays MCA1 and MCA2 and the corresponding peripheral circuits may be implemented as illustrated in FIG. 11B, and the third and fourth memory cell arrays MCA3 and MCA4 and the corresponding peripheral circuits may be implemented as illustrated in FIG. 11A. For example, the peripheral circuits corresponding to each of the first and second memory cell arrays MCA1 and MCA2, for example, the page buffers PB, the high-voltage unit HV, the C-LATCH CL, and the page buffer decoder PBDEC may be completely buried by the cell overlap region C_OVR, and the peripheral circuits corresponding to each of the third and fourth memory cell arrays MCA3 and MCA4, for example, the page buffers PB and the high-voltage unit HV may be partially buried by the cell overlap region C_OVR. In this case, a cell region of each of the first and second memory cell arrays MCA1 and MCA2 may be larger than a cell region of each of the third and fourth memory cell arrays MCA3 and MCA4.

[0153] FIG. 12D is a diagram illustrating a memory device 120d according to an embodiment.

[0154] Referring to FIG. 12D, the memory device 120d may include a first semiconductor layer 121d and a second semiconductor layer 122d. The memory device 120d corresponds to a modification of the memory device 120b of FIG. 12B, and hereinafter, differences between the memory device 120d and the memory device 120b of FIG. 12B will be mainly described. In some embodiments, the first and second memory cell arrays MCA1 and MCA2 and the corresponding peripheral circuits may be implemented as illustrated in FIG. 11B, and the third and fourth memory cell arrays MCA3 and MCA4 and the corresponding peripheral circuits may be implemented as illustrated in FIG. 11A. For example, the peripheral circuits corresponding to each of the first and second memory cell arrays MCA1 and MCA2, for example, the page buffers PB, the high-voltage unit HV, the C-

LATCH CL, and the page buffer decoder PBDEC may be completely buried by the cell overlap region C_OVR, and the peripheral circuits corresponding to each of the third and fourth memory cell arrays MCA3 and MCA4, for example, the page buffers PB and the high-voltage unit HV may be partially buried by the cell overlap region C_OVR. In this case, a cell region of each of the first and second memory cell arrays MCA1 and MCA2 may be larger than a cell region of each of the third and fourth memory cell arrays MCA3 and MCA4.

[0155] FIG. 12E is a diagram illustrating a memory device 120e according to an embodiment.

[0156] Referring to FIG. 12E, the memory device 120e may include a first semiconductor layer 121e and a second semiconductor layer 122e. The memory device 120e corresponds to a modification of the memory device 120c of FIG. 12C, and hereinafter, differences between the memory device 120e and the memory device 120c of FIG. 12C will be mainly described. In some embodiments, the first and second memory cell arrays MCA1 and MCA2 and the corresponding peripheral circuits may be implemented as illustrated in FIG. 11D, and the third and fourth memory cell arrays MCA3 and MCA4 and the corresponding peripheral circuits may be implemented as illustrated in FIG. 11A. For example, a partial region of the page buffer circuit corresponding to each of the first and second memory cell arrays MCA1 and MCA2, for example, partial regions of the page buffers PB, the high-voltage unit HV, and the row decoder XDEC may be partially buried by the cell overlap region C_OVR, and the peripheral circuits corresponding to each of the third and fourth memory cell arrays MCA3 and MCA4, for example, the page buffers PB and the high-voltage unit HV may be partially buried by the cell overlap region C_OVR. In this case, a cell region of each of the first and second memory cell arrays MCA1 and MCA2 may be larger than a cell region of each of the third and fourth memory cell arrays MCA3 and MCA4

in the second direction HD2.

[0157] FIG. 12F is a diagram illustrating a memory device 120f according to an embodiment.

[0158] Referring to FIG. 12F, the memory device 120f may include a first semiconductor layer 121f and a second semiconductor layer 122f. The memory device 120f corresponds to a modification of the memory device 120d of FIG. 12D, and hereinafter, differences between the memory device 120f and the memory device 120d of FIG. 12D will be mainly described. In some embodiments, the first and second memory cell arrays MCA1 and MCA2 and the corresponding peripheral circuits may be implemented as illustrated in FIG. 11D, and the third and fourth memory cell arrays MCA3 and MCA4 and the corresponding peripheral circuits may be implemented as illustrated in FIG. 11A. For example, a partial region of the page buffer circuit corresponding to each of the first and second memory cell arrays MCA1 and MCA2, for example, partial regions of the page buffers PB, the high-voltage unit HV, and the row decoder XDEC may be partially buried by the cell overlap region C_OVR, and the peripheral circuits corresponding to each of the third and fourth memory cell arrays MCA3 and MCA4, for example, the page buffers PB and the high-voltage unit HV may be partially buried by the cell overlap region C_OVR. In this case, a cell region of each of the first and second memory cell arrays MCA1 and MCA2 may be larger than a cell region of each of the third and fourth memory cell arrays MCA3 and MCA4 in the second direction HD2.

[0159] FIG. 13A is a diagram illustrating a memory device 130a according to an embodiment.

[0160] Referring to FIG. 13A, the memory device 130a may include a first semiconductor layer 131a and a second semiconductor layer 132a, the first semiconductor

layer 131a may include the memory cell array MCA, and the second semiconductor layer 132a may include the page buffers PB, the high-voltage units HV, the C-LATCH CL, the page buffer decoder PBDEC, and the row decoder XDEC. In some embodiments, the page buffers PB may be arranged in a multi-stage page buffer structure, and may be arranged in the first horizontal direction HD1. In this case, the memory cell array MCA may be on and overlap some of the page buffers PB and the high-voltage units HV, in the multi-stage page buffer structure. As such, some of the page buffers PB of the multi-stage page buffer structure and some of the high-voltage units HV may be buried by the memory cell array MCA, and the other page buffers PB of the multi-stage page buffer structure, the other high-voltage units HV, the C-LATCH CL, and the page buffer decoder PBDEC may not be buried by the memory cell array MCA. Alternatively or additionally, the row decoder XDEC may not be buried by the memory cell array MCA.

[0161] FIG. 13B is a diagram illustrating a memory device 130b according to an embodiment.

[0162] Referring to FIG. 13B, the memory device 130b may include a first semiconductor layer 131b and a second semiconductor layer 132b, and may correspond to a modification of the memory device 130a of FIG. 13A. The memory cell array MCA may be on and overlap some of the page buffers PB and the high-voltage units HV in the multi-stage page buffer structure, and may be on and overlap a partial region of the row decoder XDEC. As such, some of the page buffers PB of the multi-stage page buffer structure, some of the high-voltage units HV, and the partial region of the row decoder XDEC may be buried by the memory cell array MCA, and the other page buffers PB of the multi-stage page buffer structure, the other high-voltage units HV, the C-LATCH CL, the page buffer decoder PBDEC, and the remaining region of the row decoder XDEC may not be buried by the memory cell array MCA.

[0163] FIGS. 14A and 14B are diagrams illustrating memory devices 140a and 140b, respectively, according to some embodiments.

[0164] Referring to FIG. 14A, the memory device 140a may include a first semiconductor layer 141a and a second semiconductor layer 142a, the first semiconductor layer 141a may include the memory cell array MCA, and the second semiconductor layer 142a may include the page buffers PB, the high-voltage unit HV, the C-LATCH CL, the page buffer decoder PBDEC, and the row decoder XDEC. For example, the size of a cell region in which the memory cell array MCA is arranged in the first semiconductor layer 141a may be smaller than the size of the cell region of FIG. 11A, but the present disclosure is not limited thereto. In some embodiments, the memory cell array MCA may be on and overlap one page buffer PB and the high-voltage unit HV. As such, a portion of the page buffer circuit, for example, and one page buffer PB and the high-voltage unit HV may be buried by the memory cell array MCA, and the remaining portions of the page buffer circuit, for example, the other page buffer PB, the C-LATCH CL, and the page buffer decoder PBDEC may not be buried by the memory cell array MCA. Alternatively or additionally, the row decoder XDEC may not be buried by the memory cell array MCA.

[0165] Referring to FIG. 14B, the memory device 140b may include a first semiconductor layer 141b and a second semiconductor layer 142b, and may correspond to a modification of the memory device 140a of FIG. 14A. The memory device 140a of FIG. 14A may be implemented to be partially buried, whereas the memory device 140b according to some embodiments may be implemented to be completely buried. The memory cell array MCA may be on and overlap the page buffers PB, the high-voltage unit HV, the C-LATCH CL, and the page buffer decoder PBDEC. As such, the entire page buffer circuit may be buried by the memory cell array MCA. The row decoder XDEC may not be buried by the memory cell array MCA, but the present disclosure is not limited thereto, and in some

embodiments, the row decoder XDEC may also be buried by the memory cell array MCA.

[0166] In some embodiments, when a memory device includes a plurality of memory cell arrays, some memory cell arrays and corresponding peripheral circuits may be arranged as illustrated in FIG. 14A, and the remaining memory cell arrays and corresponding peripheral circuits may be arranged as illustrated in FIG. 14B. However, the present disclosure is not limited thereto, and in some embodiments, when the memory device includes a plurality of memory cell arrays, the plurality of memory cell arrays and corresponding peripheral circuits may be arranged as illustrated in FIG. 14A or 14B. These various embodiments are described with reference to FIGS. 15A to 15D.

[0167] FIG. 15A is a diagram illustrating a memory device 150a according to an embodiment.

[0168] Referring to FIG. 15A, the memory device 150a may have a structure corresponding to the second semiconductor layer 142a of FIG. 14A. For example, the memory device 150a may include the page buffers PB, the high-voltage unit HV, the C-LATCH CL, the page buffer decoder PBDEC, and the row decoder XDEC, which correspond to each of a plurality of memory cell arrays, and a portion of a page buffer circuit, for example, one page buffer PB and the high-voltage unit HV may be buried by the cell overlap region C_OVR, that is, may overlap the cell overlap region C_OVR in the vertical direction. In some embodiments, the remaining portion of the page buffer circuit, for example, the other page buffer PB, the C-LATCH CL, and the page buffer decoder PBDEC, and the row decoder XDEC may not be buried by the cell overlap region C_OVR, that is, may not overlap the cell overlap region C_OVR in the vertical direction. Furthermore, the memory device 150a may further include the pad region PA arranged in an edge region, and the pad region PA may include the plurality of bonding pads PD arranged in the second horizontal direction HD2. In this case, the pad region PA may not be buried by the cell overlap regions C_OVR,

that is, may not overlap the cell overlap regions C_OVR in the vertical direction.

[0169] FIG. 15B is a diagram illustrating a memory device 150b according to an embodiment.

[0170] Referring to FIG. 15B, the memory device 150b may have a structure corresponding to the second semiconductor layer 142a of FIG. 14A. the memory device 150b may correspond to a modification of the memory device 150a of FIG. 15A, and the descriptions thereof provided above will be omitted. The memory device 150b may further include the pad region PA arranged in a center region, and the pad region PA may include the plurality of bonding pads PD arranged in the second horizontal direction HD2. In this case, the pad region PA may not be buried by the cell overlap regions C_OVR, that is, may not overlap the cell overlap regions C_OVR in the vertical direction.

[0171] FIG. 15C is a diagram illustrating a memory device 150c according to an embodiment.

[0172] Referring to FIG. 15C, the memory device 150c corresponds to a modification of the memory device 150a of FIG. 15A, and may include both a structure corresponding to the second semiconductor layer 142a of FIG. 14A and a structure corresponding to the second semiconductor layer 142b of FIG. 14B. In some embodiments, the peripheral circuits corresponding to each of first and second memory cell arrays (e.g., MCA1 and MCA2 of FIG. 12A), for example, the page buffers PB, the high-voltage unit HV, the C-LATCH CL, and the page buffer decoder PBDEC may be completely buried by the cell overlap region C_OVR, and the peripheral circuits corresponding to each of third and fourth memory cell arrays (e.g., MCA3 and MCA4 of FIG. 12A), for example, the page buffers PB and the high-voltage unit HV may be partially buried by the cell overlap region C_OVR.

[0173] FIG. 15D is a diagram illustrating a memory device 150d according to an

embodiment.

[0174] Referring to FIG. 15D, the memory device 150d corresponds to a modification of the memory device 150b of FIG. 15B, and may include both a structure corresponding to the second semiconductor layer 142a of FIG. 14A and a structure corresponding to the second semiconductor layer 142b of FIG. 14B. In some embodiments, the peripheral circuits corresponding to each of the first and second memory cell arrays MCA1 and MCA2, for example, the page buffers PB, the high-voltage unit HV, the C-LATCH CL, and the page buffer decoder PBDEC may be completely buried by the cell overlap region C_OVR, and the peripheral circuits corresponding to each of the third and fourth memory cell arrays MCA3 and MCA4, for example, the page buffers PB and the high-voltage unit HV may be partially buried by the cell overlap region C_OVR.

[0175] FIGS. 16A and 16B are diagrams illustrating memory devices 160a and 160b, respectively, according to some embodiments.

[0176] Referring to FIG. 16A, the memory device 160a may include a first semiconductor layer 161a and a second semiconductor layer 162a, the first semiconductor layer 161a may include the memory cell array MCA, and the second semiconductor layer 162a may include the page buffers PB, the high-voltage unit HV, the C-LATCH CL, the page buffer decoder PBDEC, and the row decoder XDEC. For example, the size of a cell region in which the memory cell array MCA is arranged in the first semiconductor layer 161a may be smaller than the size of the cell region of FIG. 14A, but the present disclosure is not limited thereto. In some embodiments, the memory cell array MCA may be on and overlap the high-voltage unit HV. As such, a portion of the page buffer circuit, for example, and the high-voltage unit HV may be buried by the memory cell array MCA, and the remaining portions of the page buffer circuit, for example, the page buffer PB, the C-LATCH CL, the page buffer decoder PBDEC, and the row decoder XDEC may not be buried by the memory cell array

MCA.

[0177] Referring to FIG. 16B, the memory device 160b may include a first semiconductor layer 161b and a second semiconductor layer 162b, and may correspond to a modification of the memory device 160a of FIG. 16A. The memory device 160a of FIG. 16A may be implemented to be partially buried, whereas the memory device 160b according to some embodiments may be implemented to be completely buried. The memory cell array MCA may be on and overlap the page buffers PB, the high-voltage unit HV, the C-LATCH CL, and the page buffer decoder PBDEC. As such, the entire page buffer circuit may be buried by the memory cell array MCA. The row decoder XDEC may not be buried by the memory cell array MCA, but the present disclosure is not limited thereto, and in some embodiments, the row decoder XDEC may also be buried by the memory cell array MCA.

[0178] In some embodiments, when a memory device includes a plurality of memory cell arrays, some memory cell arrays and corresponding peripheral circuits may be arranged as illustrated in FIG. 16A, and the remaining memory cell arrays and corresponding peripheral circuits may be arranged as illustrated in FIG. 16B. However, the present disclosure is not limited thereto, and in some embodiments, when the memory device includes a plurality of memory cell arrays, the plurality of memory cell arrays and corresponding peripheral circuits may be arranged as illustrated in FIG. 16A or 16B. These various embodiments are described with reference to FIGS. 17A to 17D.

[0179] FIG. 17A is a diagram illustrating a memory device 170a according to an embodiment.

[0180] Referring to FIG. 17A, the memory device 170a may have a structure corresponding to the second semiconductor layer 162a of FIG. 16A. For example, the memory device 170a may include the page buffers PB, the high-voltage unit HV, the C-

LATCH CL, the page buffer decoder PBDEC, and the row decoder XDEC, which correspond to each of a plurality of memory cell arrays, and a portion of a page buffer circuit, for example, the high-voltage unit HV may be buried by the cell overlap region C_OVR, that is, may overlap the cell overlap region C_OVR in the vertical direction. In some embodiments, the remaining portion of the page buffer circuit, for example, the page buffer PB, the C-LATCH CL, and the page buffer decoder PBDEC, and the row decoder XDEC may not be buried by the cell overlap region C_OVR, that is, may not overlap the cell overlap region C_OVR in the vertical direction. In this case, the memory device 170a may further include the pad region PA arranged in an edge region, and the pad region PA may include the plurality of bonding pads PD arranged in the second horizontal direction HD2. In this case, the pad region PA may not be buried by cell overlap regions C_OVR, that is, may not overlap the cell overlap regions C_OVR in the vertical direction.

[0181] FIG. 17B is a diagram illustrating a memory device 170b according to an embodiment.

[0182] Referring to FIG. 17B, the memory device 170b may have a structure corresponding to the second semiconductor layer 162a of FIG. 16A. Alternatively or additionally, the memory device 170b may correspond to a modification of the memory device 170a of FIG. 17A, and the descriptions thereof provided above will be omitted. The memory device 170b may further include the pad region PA arranged in a center region, and the pad region PA may include the plurality of bonding pads PD arranged in the second horizontal direction HD2. In this case, the pad region PA may not be buried by cell overlap regions C_OVR, that is, may not overlap the cell overlap regions C_OVR in the vertical direction.

[0183] FIG. 17C is a diagram illustrating a memory device 170c according to an embodiment.

[0184] Referring to FIG. 17C, the memory device 170c corresponds to a modification of the memory device 170a of FIG. 17A, and may include both a structure corresponding to the second semiconductor layer 162a of FIG. 16A and a structure corresponding to the second semiconductor layer 162b of FIG. 16B. In some embodiments, the peripheral circuits corresponding to each of first and second memory cell arrays (e.g., MCA1 and MCA2 of FIG. 12A), for example, the page buffers PB, the high-voltage unit HV, the C-LATCH CL, and the page buffer decoder PBDEC may be completely buried by the cell overlap region C_OVR, and the peripheral circuits corresponding to each of third and fourth memory cell arrays (e.g., MCA3 and MCA4 of FIG. 12A), for example, the high-voltage unit HV may be partially buried by the cell overlap region C_OVR.

[0185] FIG. 17D is a diagram illustrating a memory device 170d according to an embodiment.

[0186] Referring to FIG. 17D, the memory device 170d corresponds to a modification of the memory device 170b of FIG. 17B, and may include both a structure corresponding to the second semiconductor layer 162a of FIG. 16A and a structure corresponding to the second semiconductor layer 162b of FIG. 16B. In some embodiments, the peripheral circuits corresponding to each of the first and second memory cell arrays MCA1 and MCA2, for example, the page buffers PB, the high-voltage unit HV, the C-LATCH CL, and the page buffer decoder PBDEC may be completely buried by the cell overlap region C_OVR, and the peripheral circuits corresponding to each of the third and fourth memory cell arrays MCA3 and MCA4, for example, the high-voltage unit HV may be partially buried by the cell overlap region C_OVR.

[0187] FIGS. 18A and 18B are diagrams illustrating memory devices 180a and 180b, respectively, according to some embodiments.

[0188] Referring to FIG. 18A, the memory device 180a may include a first semiconductor layer 181a and a second semiconductor layer 182a, the first semiconductor layer 181a may include the memory cell array MCA, and the second semiconductor layer 182a may include first and second page buffer circuits 1821a and 1822a and the row decoders XDEC. Each of the first and second page buffer circuits 1821a and 1822a may include the page buffers PB, the high-voltage unit HV, the C-LATCH CL, and the page buffer decoder PBDEC. In this case, the page buffers PB, the high-voltage unit HV, the C-LATCH CL, and the page buffer decoder PBDEC included in the first page buffer circuit 1821a may be buried by the memory cell array MCA, some of elements included in the second page buffer circuit 1822a may be buried by the memory cell array MCA, and the other elements may not be buried by the memory cell array MCA. For example, the page buffers PB and the high-voltage unit HV included in the second page buffer circuit 1822a may be buried by the memory cell array MCA, and the C-LATCH CL and the page buffer decoder PBDEC included in the second page buffer circuit 1822a may not be buried by the memory cell array MCA. In this case, the row decoders XDEC may be buried by the memory cell array MCA. For example, the row decoders XDEC may differ in size in the first horizontal direction HD1 from each other, but the present disclosure is not limited thereto.

[0189] Referring to FIG. 18B, the memory device 180b may include a first semiconductor layer 181b and a second semiconductor layer 182b, and the second semiconductor layer 182b may include first and second page buffer circuits 1821b and 1822b and the row decoders XDEC, and may correspond to a modification of the memory device 180a of FIG. 18A. The memory device 180a of FIG. 18A may be implemented to be partially buried, whereas the memory device 180b according to some embodiments may be implemented to be completely buried. The memory cell array MCA may be on and overlap the page buffers PB, the high-voltage unit HV, the C-LATCH CL, the page buffer decoder

PBDEC, and the row decoders XDEC. As such, both the page buffer circuit and the row decoders XDEC may be buried by the memory cell array MCA.

[0190] In some embodiments, when a memory device includes a plurality of memory cell arrays, some memory cell arrays and corresponding peripheral circuits may be arranged as illustrated in FIG. 18A, and the remaining memory cell arrays and corresponding peripheral circuits may be arranged as illustrated in FIG. 18B. However, the present disclosure is not limited thereto, and in some embodiments, when the memory device includes a plurality of memory cell arrays, the plurality of memory cell arrays and corresponding peripheral circuits may be arranged as illustrated in FIG. 18A or 18B. These various embodiments are described with reference to FIGS. 19A to 19D.

[0191] FIG. 19A is a diagram illustrating a memory device 190a according to an embodiment.

[0192] Referring to FIG. 19A, the memory device 190a may have a structure corresponding to the second semiconductor layer 182a of FIG. 18A. For example, the memory device 190a may include the page buffers PB, the high-voltage unit HV, the C-LATCH CL, the page buffer decoder PBDEC, and the row decoders XDEC, which correspond to each of a plurality of memory cell arrays, and a first page buffer circuit (e.g., 1821a of FIG. 18A), a portion of a second page buffer circuit (e.g., 1822a of FIG. 18A), for example, the page buffers PB and the high-voltage unit HV, and the row decoders XDEC may be buried by the cell overlap region C_OVR, that is, may overlap the cell overlap region C_OVR in the vertical direction.

[0193] In some embodiments, the remaining portion of the second page buffer circuit (e.g., 1822a of FIG. 18A), for example, the C-LATCH CL and the page buffer decoder PBDEC, may be arranged in an edge region and thus may not be buried by the cell overlap

region C_OVR, that is, may not overlap the cell overlap region C_OVR in the vertical direction. Alternatively or additionally, the memory device 190a may further include an external peripheral circuit OUTER_PERI arranged in an edge region, for example, an input/output circuit (e.g., a data input/output buffer, etc.), and the external peripheral circuit OUTER_PERI may not be buried by the cell overlap region C_OVR, that is, may not overlap the cell overlap region C_OVR in the vertical direction. Furthermore, the memory device 190a may further include the pad region PA arranged in an edge region, and the pad region PA may include the plurality of bonding pads PD arranged in the second horizontal direction HD2. In this case, the pad region PA may not be buried by cell overlap regions C_OVR, that is, may not overlap the cell overlap regions C_OVR in the vertical direction.

[0194] FIG. 19B is a diagram illustrating a memory device 190b according to an embodiment.

[0195] Referring to FIG. 19B, the memory device 190b may have a structure corresponding to the second semiconductor layer 182a of FIG. 18A. Also, the memory device 190b may correspond to a modification of the memory device 190a of FIG. 19A, and the descriptions thereof provided above will be omitted. A first page buffer circuit (e.g., 1821a of FIG. 18A), a portion of a second page buffer circuit (e.g., 1822a of FIG. 18A), for example, the page buffers PB and the high-voltage unit HV, and the row decoders XDEC may be buried by the cell overlap region C_OVR, that is, may overlap the cell overlap region C_OVR in the vertical direction. The remaining portion of the second page buffer circuit (e.g., 1822a of FIG. 18A), for example, the C-LATCH CL and the page buffer decoder PBDEC, may be arranged in a center region and thus may not be buried by the cell overlap region C_OVR, that is, may not overlap the cell overlap region C_OVR in the vertical direction.

[0196] The memory device 190b may further include the external peripheral circuit

OUTER_PERI arranged in a center region, for example, an input/output circuit (e.g., a data input/output buffer, etc.), and the external peripheral circuit OUTER_PERI may not be buried by the cell overlap region C_OVR, that is, may not overlap the cell overlap region C_OVR in the vertical direction. Also, the memory device 190b may further include the pad region PA arranged in a center region, and the pad region PA may include the plurality of bonding pads PD arranged in the second horizontal direction HD2. In this case, the pad region PA may not be buried by cell overlap regions C_OVR, that is, may not overlap the cell overlap regions C_OVR in the vertical direction.

[0197] FIG. 19C is a diagram illustrating a memory device 190c according to an embodiment.

[0198] Referring to FIG. 19C, the memory device 190c corresponds to a modification of the memory device 190a of FIG. 19A, and may include both a structure corresponding to the second semiconductor layer 182a of FIG. 18A and a structure corresponding to the second semiconductor layer 182b of FIG. 18B. In some embodiments, the peripheral circuits corresponding to each of first and second memory cell arrays (e.g., MCA1 and MCA2 of FIG. 12A), for example, the page buffers PB, the high-voltage unit HV, the C-LATCH CL, the page buffer decoder PBDEC, and the row decoders XDEC may be completely buried by the cell overlap region C_OVR, and the peripheral circuits corresponding to each of third and fourth memory cell arrays (e.g., MCA3 and MCA4 of FIG. 12A) may be partially buried by the cell overlap region C_OVR.

[0199] FIG. 19D is a diagram illustrating a memory device 190d according to an embodiment.

[0200] Referring to FIG. 19D, the memory device 190d corresponds to a modification of the memory device 190b of FIG. 19B, and may include both a structure corresponding to

the second semiconductor layer 182a of FIG. 18A and a structure corresponding to the second semiconductor layer 182b of FIG. 18B. In some embodiments, the peripheral circuits corresponding to each of the first and second memory cell arrays MCA1 and MCA2, for example, the page buffers PB, the high-voltage unit HV, the C-LATCH CL, the page buffer decoder PBDEC, and the row decoders XDEC may be completely buried by the cell overlap region C_OVR, and the peripheral circuits corresponding to each of the third and fourth memory cell arrays MCA3 and MCA4 may be partially buried by the cell overlap region C_OVR.

[0201] FIGS. 20A and 20B are diagrams illustrating memory devices 200a and 200b, respectively, according to some embodiments.

[0202] Referring to FIG. 20A, the memory device 200a may include a first semiconductor layer 201a and a second semiconductor layer 202a, the first semiconductor layer 201a may include the memory cell array MCA, and the second semiconductor layer 202a may include first and second page buffer circuits 2021a and 2022a and the row decoders XDEC. Each of the first and second page buffer circuits 2021a and 2022a may include the page buffers PB, the high-voltage unit HV, the C-LATCH CL, and the page buffer decoder PBDEC. Some of elements included in the first page buffer circuit 2021a may be buried by the memory cell array MCA, and the other elements may not be buried by the memory cell array MCA. For example, the page buffers PB and the high-voltage unit HV included in the first page buffer circuit 2021a may be buried by the memory cell array MCA, and the C-LATCH CL and the page buffer decoder PBDEC included in the first page buffer circuit 2021a may not be buried by the memory cell array MCA.

[0203] In some embodiments, some of elements included in the second page buffer circuit 2022a may be buried by the memory cell array MCA, and the other elements may not be buried by the memory cell array MCA. For example, the page buffers PB and the high-

voltage unit HV included in the second page buffer circuit 2022a may be buried by the memory cell array MCA, and the C-LATCH CL and the page buffer decoder PBDEC included in the second page buffer circuit 2022a may not be buried by the memory cell array MCA. In this case, the row decoders XDEC may be buried by the memory cell array MCA.

[0204] Referring to FIG. 20B, the memory device 200b may include a first semiconductor layer 201b and a second semiconductor layer 202b, and the second semiconductor layer 202b may include first and second page buffer circuits 2021b and 2022b and the row decoders XDEC, and may correspond to a modification of the memory device 200a of FIG. 20A. The memory device 200a of FIG. 20A may be implemented to be partially buried, whereas the memory device 200b according to some embodiments may be implemented to be completely buried. The memory cell array MCA may be on and overlap the page buffers PB, the high-voltage unit HV, the C-LATCH CL, the page buffer decoder PBDEC, and the row decoders XDEC. As such, both the page buffer circuit and the row decoders XDEC may be buried by the memory cell array MCA.

[0205] In some embodiments, when a memory device includes a plurality of memory cell arrays, some memory cell arrays and corresponding peripheral circuits may be arranged as illustrated in FIG. 20A, and the remaining memory cell arrays and corresponding peripheral circuits may be arranged as illustrated in FIG. 20B. However, the present disclosure is not limited thereto, and in some embodiments, when the memory device includes a plurality of memory cell arrays, the plurality of memory cell arrays and corresponding peripheral circuits may be arranged as illustrated in FIG. 20A or 20B. These various embodiments are described with reference to FIGS. 21A to 21D.

[0206] FIG. 21A is a diagram illustrating a memory device 210a according to an embodiment.

[0207] Referring to FIG. 21A, the memory device 210a may have a structure corresponding to the second semiconductor layer 202a of FIG. 20A. For example, the memory device 210a may include the page buffers PB, the high-voltage unit HV, the C-LATCH CL, the page buffer decoder PBDEC, and the row decoders XDEC, which correspond to each of a plurality of memory cell arrays, and a portion of each of first and second page buffer circuits (e.g., 2021a and 2022a of FIG. 20A), for example, the page buffers PB and the high-voltage unit HV, and the row decoders XDEC may be buried by the cell overlap region C_OVR, that is, may overlap the cell overlap region C_OVR in the vertical direction. In some embodiments, the remaining portion of each of the first and second page buffer circuits (e.g., 2021a and 2022a of FIG. 20A), for example, the C-LATCH CL and the page buffer decoder PBDEC, may be arranged in an edge region or a center region, and may not be buried by the cell overlap region C_OVR, that is, may not overlap the cell overlap region C_OVR in the vertical direction.

[0208] Alternatively or additionally, the memory device 210a may further include the external peripheral circuit OUTER_PERI arranged in an edge region or a center region, for example, an input/output circuit (e.g., a data input/output buffer, etc.), and the external peripheral circuit OUTER_PERI may not be buried by the cell overlap region C_OVR, that is, may not overlap the cell overlap region C_OVR in the vertical direction. Furthermore, the memory device 210a may further include the pad region PA arranged in an edge region, and the pad region PA may include the plurality of bonding pads PD arranged in the second horizontal direction HD2. In this case, the pad region PA may not be buried by cell overlap regions C_OVR, that is, may not overlap the cell overlap regions C_OVR in the vertical direction.

[0209] FIG. 21B is a diagram illustrating a memory device 210b according to an embodiment.

[0210] Referring to FIG. 21B, the memory device 210b may have a structure corresponding to the second semiconductor layer 202a of FIG. 20A. Also, the memory device 210b may correspond to a modification of the memory device 210a of FIG. 21A, and the descriptions thereof provided above will be omitted. The memory device 210b may further include the pad region PA arranged in a center region, and the pad region PA may include the plurality of bonding pads PD arranged in the second horizontal direction HD2. In this case, the pad region PA may not be buried by cell overlap regions C_OVR, that is, may not overlap the cell overlap regions C_OVR in the vertical direction.

[0211] FIG. 21C is a diagram illustrating a memory device 210c according to an embodiment.

[0212] Referring to FIG. 21C, the memory device 210c corresponds to a modification of the memory device 210a of FIG. 21A, and may include both a structure corresponding to the second semiconductor layer 202a of FIG. 20A and a structure corresponding to the second semiconductor layer 202b of FIG. 20B. In some embodiments, the peripheral circuits corresponding to each of first and second memory cell arrays (e.g., MCA1 and MCA2 of FIG. 12A), for example, the page buffers PB, the high-voltage unit HV, the C-LATCH CL, the page buffer decoder PBDEC, and the row decoders XDEC may be completely buried by the cell overlap region C_OVR, and the peripheral circuits corresponding to each of third and fourth memory cell arrays (e.g., MCA3 and MCA4 of FIG. 12A) may be partially buried by the cell overlap region C_OVR.

[0213] FIG. 21D is a diagram illustrating a memory device 210d according to an embodiment.

[0214] Referring to FIG. 21D, the memory device 210d corresponds to a modification of the memory device 210b of FIG. 21B, and may include both a structure corresponding to

the second semiconductor layer 202a of FIG. 20A and a structure corresponding to the second semiconductor layer 202b of FIG. 20B. In some embodiments, the peripheral circuits corresponding to each of the first and second memory cell arrays MCA1 and MCA2, for example, the page buffers PB, the high-voltage unit HV, the C-LATCH CL, the page buffer decoder PBDEC, and the row decoders XDEC may be completely buried by the cell overlap region C_OVR, and the peripheral circuits corresponding to each of the third and fourth memory cell arrays MCA3 and MCA4 may be partially buried by the cell overlap region C_OVR.

[0215] FIGS. 22A and 22B are diagrams illustrating memory devices 220A and 220B, respectively, according to some embodiments.

[0216] Referring to FIG. 22A, the memory device 220A may include a first semiconductor layer 221a and a second semiconductor layer 222a, the first semiconductor layer 221a may include the memory cell array MCA, and the second semiconductor layer 222a may include first and second page buffer circuits 2221a and 2222a and the row decoders XDEC. Each of the first and second page buffer circuits 2221a and 2222a may include the page buffers PB, the high-voltage unit HV, the C-LATCH CL, and the page buffer decoder PBDEC. Some of elements included in the first page buffer circuit 2221a may be buried by the memory cell array MCA, and the other elements may not be buried by the memory cell array MCA. For example, one page buffer PB and the high-voltage unit HV included in the first page buffer circuit 2221a may be buried by the memory cell array MCA, and the other page buffer PB, the C-LATCH CL, and the page buffer decoder PBDEC included in the first page buffer circuit 2221a may not be buried by the memory cell array MCA. In some embodiments, the second page buffer circuit 2222a may be buried by the memory cell array MCA. In this case, the row decoders XDEC may be buried by the memory cell array MCA.

[0217] Referring to FIG. 22B, the memory device 220B may include a first

semiconductor layer 221b and a second semiconductor layer 222b, and the second semiconductor layer 222b may include first and second page buffer circuits 2221b and 2222b and the row decoders XDEC, and may correspond to a modification of the memory device 220A of FIG. 22A. The memory device 220A of FIG. 22A may be implemented to be partially buried, whereas the memory device 220B according to some embodiments may be implemented to be completely buried. The memory cell array MCA may be on and overlap the page buffers PB, the high-voltage unit HV, the C-LATCH CL, the page buffer decoder PBDEC, and the row decoders XDEC. As such, both the page buffer circuit and the row decoders XDEC may be buried by the memory cell array MCA.

[0218] In some embodiments, when a memory device includes a plurality of memory cell arrays, some memory cell arrays and corresponding peripheral circuits may be arranged as illustrated in FIG. 22A, and the remaining memory cell arrays and corresponding peripheral circuits may be arranged as illustrated in FIG. 22B. However, the present disclosure is not limited thereto, and in some embodiments, when the memory device includes a plurality of memory cell arrays, the plurality of memory cell arrays and corresponding peripheral circuits may be arranged as illustrated in FIG. 22A or 22B. These various embodiments are described with reference to FIGS. 23A to 23D.

[0219] FIG. 23A is a diagram illustrating a memory device 230A according to an embodiment.

[0220] Referring to FIG. 23A, the memory device 230A may have a structure corresponding to the second semiconductor layer 222a of FIG. 22A. For example, the memory device 230A may include the page buffers PB, the high-voltage unit HV, the C-LATCH CL, the page buffer decoder PBDEC, and the row decoder XDEC, which correspond to each of a plurality of memory cell arrays. A portion of a first page buffer circuit (e.g., 2221a of FIG. 22A), for example, one page buffer PB and the high-voltage unit HV, and the

row decoders XDEC may be buried by the cell overlap region C_OVR, that is, may overlap the cell overlap region C_OVR in the vertical direction. The remaining portion of the first page buffer circuit, for example, one page buffer PB, the C-LATCH CL, and the page buffer decoder PBDEC may be arranged in an edge region and thus may not be buried by the cell overlap region C_OVR, that is, may not overlap the cell overlap region C_OVR in the vertical direction. On the other hand, a second page buffer circuit (e.g., 2222a of FIG. 22A) may be arranged in a center region and thus buried by the cell overlap region C_OVR, that is, may overlap the cell overlap region C_OVR in the vertical direction.

[0221] Alternatively or additionally, the memory device 230A may further include the external peripheral circuit OUTER_PERI arranged in an edge region, for example, an input/output circuit (e.g., a data input/output buffer, etc.), and the external peripheral circuit OUTER_PERI may not be buried by the cell overlap region C_OVR, that is, may not overlap the cell overlap region C_OVR in the vertical direction. Furthermore, the memory device 230A may further include the pad region PA arranged in an edge region, and the pad region PA may include the plurality of bonding pads PD arranged in the second horizontal direction HD2. In this case, the pad region PA may not be buried by cell overlap regions C_OVR, that is, may not overlap the cell overlap regions C_OVR in the vertical direction.

[0222] FIG. 23B is a diagram illustrating a memory device 230B according to an embodiment.

[0223] Referring to FIG. 23B, the memory device 230B may have a structure corresponding to the second semiconductor layer 222a of FIG. 22A. Also, the memory device 230B may correspond to a modification of the memory device 230A of FIG. 23A, and the descriptions thereof provided above will be omitted. A portion of a first page buffer circuit (e.g., 2221a of FIG. 22A), for example, one page buffer PB and the high-voltage unit HV, and the row decoders XDEC may be buried by the cell overlap region C_OVR, that is, may

overlap the cell overlap region C_OVR in the vertical direction. The remaining portion of the first page buffer circuit, for example, one page buffer PB, the C-LATCH CL, and the page buffer decoder PBDEC may be arranged in a center region and thus may not be buried by the cell overlap region C_OVR, that is, may not overlap the cell overlap region C_OVR in the vertical direction. On the other hand, a second page buffer circuit (e.g., 2222a of FIG. 22A) may be arranged in a corner region and thus buried by the cell overlap region C_OVR, that is, may overlap the cell overlap region C_OVR in the vertical direction.

[0224] The memory device 230B may further include the external peripheral circuit OUTER_PERI and the pad region PA, which are arranged in a center region. In this case, the external peripheral circuit OUTER_PERI and the pad region PA may not be buried by the cell overlap region C_OVR, that is, may not overlap the cell overlap region C_OVR in the vertical direction.

[0225] FIG. 23C is a diagram illustrating a memory device 230C according to an embodiment.

[0226] Referring to FIG. 23C, the memory device 230C corresponds to a modification of the memory device 230A of FIG. 23A, and may include both a structure corresponding to the second semiconductor layer 222a of FIG. 22A and a structure corresponding to the second semiconductor layer 222b of FIG. 22B. In some embodiments, the peripheral circuits corresponding to each of first and second memory cell arrays (e.g., MCA1 and MCA2 of FIG. 12A), for example, the page buffers PB, the high-voltage unit HV, the C-LATCH CL, the page buffer decoder PBDEC, and the row decoders XDEC may be completely buried by the cell overlap region C_OVR, and the peripheral circuits corresponding to each of third and fourth memory cell arrays (e.g., MCA3 and MCA4 of FIG. 12A) may be partially buried by the cell overlap region C_OVR.

[0227] FIG. 23D is a diagram illustrating a memory device 230D according to an embodiment.

[0228] Referring to FIG. 23D, the memory device 230D corresponds to a modification of the memory device 230B of FIG. 23B, and may include both a structure corresponding to the second semiconductor layer 222a of FIG. 22A and a structure corresponding to the second semiconductor layer 222b of FIG. 22B. In some embodiments, the peripheral circuits corresponding to each of the first and second memory cell arrays MCA1 and MCA2, for example, the page buffers PB, the high-voltage unit HV, the C-LATCH CL, the page buffer decoder PBDEC, and the row decoders XDEC may be completely buried by the cell overlap region C_OVR, and the peripheral circuits corresponding to each of the third and fourth memory cell arrays MCA3 and MCA4 may be partially buried by the cell overlap region C_OVR.

[0229] FIGS. 24A and 24B are diagrams illustrating memory devices 240A and 240B, respectively, according to some embodiments.

[0230] Referring to FIG. 24A, the memory device 240A may include a first semiconductor layer 241a and a second semiconductor layer 242a, the first semiconductor layer 241a may include the memory cell array MCA, and the second semiconductor layer 242a may include first and second page buffer circuits 2421a and 2422a and the row decoders XDEC. Each of the first and second page buffer circuits 2421a and 2422a may include the page buffers PB, the high-voltage unit HV, the C-LATCH CL, and the page buffer decoder PBDEC. Some of elements included in the first and second page buffer circuits 2421a and 2422a may be buried by the memory cell array MCA, and the other elements may not be buried by the memory cell array MCA. For example, one page buffer PB and the high-voltage unit HV included in each of the first and second page buffer circuits 2421a and 2422a may be buried by the memory cell array MCA, and the other page buffer PB, the C-LATCH

CL, and the page buffer decoder PBDEC included in each of the first and second page buffer circuits 2421a and 2422a may not be buried by the memory cell array MCA. In this case, the row decoders XDEC may be buried by the memory cell array MCA.

[0231] Referring to FIG. 24B, the memory device 240B may include a first semiconductor layer 241b and a second semiconductor layer 242b, and the second semiconductor layer 242b may include first and second page buffer circuits 2421b and 2422b and the row decoders XDEC, and may correspond to a modification of the memory device 240A of FIG. 24A. The memory device 240A of FIG. 24A may be implemented to be partially buried, whereas the memory device 240B according to some embodiments may be implemented to be completely buried. The memory cell array MCA may be on and overlap the page buffers PB, the high-voltage unit HV, the C-LATCH CL, the page buffer decoder PBDEC, and the row decoders XDEC. As such, the entire page buffer circuit may be buried by the memory cell array MCA.

[0232] In some embodiments, when a memory device includes a plurality of memory cell arrays, some memory cell arrays and corresponding peripheral circuits may be arranged as illustrated in FIG. 24A, and the remaining memory cell arrays and corresponding peripheral circuits may be arranged as illustrated in FIG. 24B. However, the present disclosure is not limited thereto, and in some embodiments, when the memory device includes a plurality of memory cell arrays, the plurality of memory cell arrays and corresponding peripheral circuits may be arranged as illustrated in FIG. 24A or 24B. These various embodiments are described with reference to FIGS. 25A to 25D.

[0233] FIG. 25A is a diagram illustrating a memory device 250a according to an embodiment.

[0234] Referring to FIG. 25A, the memory device 250a may have a structure

corresponding to the second semiconductor layer 242a of FIG. 24A. For example, the memory device 250a may include the page buffers PB, the high-voltage unit HV, the C-LATCH CL, the page buffer decoder PBDEC, and the row decoder XDEC, which correspond to each of a plurality of memory cell arrays. A portion of each of first and second page buffer circuits (e.g., 2421a and 2422a of FIG. 24A), for example, one page buffer PB and the high-voltage unit HV, and the row decoders XDEC may be buried by the cell overlap region C_OVR, that is, may overlap the cell overlap region C_OVR in the vertical direction. The remaining portion of each of the first and second page buffer circuits, for example, one page buffer PB, the C-LATCH CL, and the page buffer decoder PBDEC may be arranged in a center region or an edge region and thus may not be buried by the cell overlap region C_OVR, that is, may not overlap the cell overlap region C_OVR in the vertical direction.

[0235] Alternatively or additionally, the memory device 250a may further include the external peripheral circuit OUTER_PERI arranged in a center region or an edge region, for example, an input/output circuit (e.g., a data input/output buffer, etc.), and the external peripheral circuit OUTER_PERI may not be buried by the cell overlap region C_OVR, that is, may not overlap the cell overlap region C_OVR in the vertical direction. Furthermore, the memory device 250a may further include the pad region PA arranged in an edge region, and the pad region PA may include the plurality of bonding pads PD arranged in the second horizontal direction HD2. In this case, the pad region PA may not be buried by cell overlap regions C_OVR, that is, may not overlap the cell overlap regions C_OVR in the vertical direction.

[0236] FIG. 25B is a diagram illustrating a memory device 250b according to an embodiment.

[0237] Referring to FIG. 25B, the memory device 250b may have a structure corresponding to the second semiconductor layer 242a of FIG. 24A. Also, the memory device

250b may correspond to a modification of the memory device 250a of FIG. 25A, and the descriptions thereof provided above will be omitted. The memory device 250b may further include the external peripheral circuit OUTER_PERI arranged in a center region or an edge region, and the pad region PA arranged in a center region. In this case, the external peripheral circuit OUTER_PERI and the pad region PA may not be buried by the cell overlap region C_OVR, that is, may not overlap the cell overlap region C_OVR in the vertical direction.

[0238] FIG. 25C is a diagram illustrating a memory device 250c according to an embodiment.

[0239] Referring to FIG. 25C, the memory device 250c corresponds to a modification of the memory device 250a of FIG. 25A, and may include both a structure corresponding to the second semiconductor layer 242a of FIG. 24A and a structure corresponding to the second semiconductor layer 242b of FIG. 24B. In some embodiments, the peripheral circuits corresponding to each of first and second memory cell arrays (e.g., MCA1 and MCA2 of FIG. 12A), for example, the page buffers PB, the high-voltage unit HV, the C-LATCH CL, the page buffer decoder PBDEC, and the row decoders XDEC may be completely buried by the cell overlap region C_OVR, and the peripheral circuits corresponding to each of third and fourth memory cell arrays (e.g., MCA3 and MCA4 of FIG. 12A) may be partially buried by the cell overlap region C_OVR.

[0240] FIG. 25D is a diagram illustrating a memory device 250d according to an embodiment.

[0241] Referring to FIG. 25D, the memory device 250d corresponds to a modification of the memory device 250b of FIG. 25B, and may include both a structure corresponding to the second semiconductor layer 242a of FIG. 24A and a structure corresponding to the second semiconductor layer 242b of FIG. 24B. In some embodiments, the peripheral circuits

corresponding to each of the first and second memory cell arrays MCA1 and MCA2, for example, the page buffers PB, the high-voltage unit HV, the C-LATCH CL, the page buffer decoder PBDEC, and the row decoders XDEC may be completely buried by the cell overlap region C_OVR, and the peripheral circuits corresponding to each of the third and fourth memory cell arrays MCA3 and MCA4 may be partially buried by the cell overlap region C_OVR.

[0242] FIG. 26A is a diagram illustrating a memory device 260a according to an embodiment.

[0243] Referring to FIG. 26A, the memory device 260a may include a first semiconductor layer 261a and a second semiconductor layer 262a, and first to sixth memory cell arrays MCA1 to MCA6 may be arranged in the first semiconductor layer 261a. The second semiconductor layer 262a may include the page buffers PB, the high-voltage unit HV, the C-LATCH CL, the page buffer decoder PBDEC, and the row decoder XDEC, which correspond to each of the first to sixth memory cell arrays MCA1 to MCA6. As such, the memory device 260a may be implemented in a 6-MAT structure, but the present disclosure is not limited thereto, and the number of memory cell arrays or the number of mats included in the memory device 260a may vary depending on embodiments.

[0244] The second semiconductor layer 262a may further include the pad region PA. In some embodiments, the pad region PA may be arranged in an edge region, a bottom region, or a top region of the second semiconductor layer 262a, and may include the plurality of bonding pads PD arranged in the second horizontal direction HD2. In this case, the pad region PA may not be buried by cell overlap regions C_OVR, that is, may not overlap the cell overlap regions C_OVR in the vertical direction.

[0245] In some embodiments, the first to fourth memory cell arrays MCA1 to MCA4

and the corresponding peripheral circuits may be implemented as illustrated in FIG. 18B, and the fifth and sixth memory cell arrays MCA5 and MCA6 and the corresponding peripheral circuits may be implemented as illustrated in FIG. 18A. For example, the peripheral circuits corresponding to each of the first to fourth memory cell arrays MCA1 to MCA4 may be completely buried, and the peripheral circuits corresponding to each of the fifth and sixth memory cell arrays MCA5 and MCA6 may be partially buried. For example, in the second semiconductor layer 262a, a partial region of the page buffer circuit corresponding to each of the fifth and sixth memory cell arrays MCA5 and MCA6, for example, the C-LATCH CL and the page buffer decoder PBDEC, may not be buried by the cell overlap region C_OVR. For example, the cell overlap regions C_OVR respectively corresponding to the first to sixth memory cell arrays MCA1 to MCA6 may have different sizes.

[0246] FIG. 26B is a diagram illustrating a memory device 260b according to an embodiment.

[0247] Referring to FIG. 26B, the memory device 260b may include a first semiconductor layer 261b and a second semiconductor layer 262b, and may correspond to a modification of the memory device 260a of FIG. 26A. The memory device 260b may further include the pad region PA arranged in a center region, and the pad region PA may include the plurality of bonding pads PD arranged in the second horizontal direction HD2. In this case, the pad region PA may not be buried by cell overlap regions C_OVR, that is, may not overlap the cell overlap regions C_OVR in the vertical direction. In some embodiments, the first and second memory cell arrays MCA1 and MCA2 and the corresponding peripheral circuits may be implemented as illustrated in FIG. 18B, and the third to sixth memory cell arrays MCA3 to MCA6 and the corresponding peripheral circuits may be implemented as illustrated in FIG. 18A.

[0248] FIG. 27 is a block diagram illustrating a solid-state drive (SSD) system 1000

to which a memory device according to an embodiment.

[0249] Referring to FIG. 27, the SSD system 1000 may include a host 1100 and an SSD 1200. The SSD 1200 transmits and receives signals to and from the host 1100 through a signal connector 1201, and receives power through a power connector 1202. The SSD 1200 may include an SSD controller 1210, an auxiliary power supply 1230, and memory devices 1221, 1222, and 122n. The memory devices 1221, 1222, and 122n may be vertically stacked NAND flash memory devices. In this case, the SSD 1200 may be implemented by using the embodiments described above with reference to FIGS. 1 to 26B.

[0250] While the present disclosure has been particularly shown and described with reference to embodiments thereof, it will be understood that various changes in form and details may be made therein without departing from the spirit and scope of the following claims.

What is Claimed is:

1. A non-volatile memory device, comprising:

a first semiconductor layer that includes:

a first memory cell array that is disposed on a first cell region of the first semiconductor layer, wherein the first memory cell array includes a first plurality of word lines stacked in a vertical direction and a first plurality of memory cells respectively coupled to the first plurality of word lines;

a second memory cell array that is disposed on a second cell region of the first semiconductor layer, wherein the second memory cell array includes a second plurality of word lines stacked in the vertical direction and a second plurality of memory cells respectively coupled to the second plurality of word lines; and

a first metal pad; and

a second semiconductor layer that includes:

a first peripheral circuit disposed on a first region of the second semiconductor layer and coupled to the first memory cell array;

a second peripheral circuit disposed on a second region of the second semiconductor layer and coupled to the second memory cell array; and

a second metal pad,

wherein the second semiconductor layer is coupled, in the vertical direction, to the first semiconductor layer by the first metal pad and the second metal pad in a bonding manner,

wherein the first region includes a first peripheral circuit region that overlaps the first cell region in the vertical direction, and a second peripheral circuit region that does not overlap the first cell region in the vertical direction, and

wherein the second region overlaps the second cell region in the vertical direction.

2. The non-volatile memory device of claim 1, wherein the first peripheral circuit includes a first page buffer circuit,

wherein a portion of the first page buffer circuit is disposed on the first peripheral circuit region,

wherein another portion of the first page buffer circuit is disposed on the second peripheral circuit region,

wherein the second peripheral circuit includes a second page buffer circuit, and

wherein the second page buffer circuit is disposed on the second region.

3. The non-volatile memory device of claim 2, wherein the first page buffer circuit includes a sensing latch and a cache latch,

wherein the sensing latch is disposed on the first peripheral circuit region, and

wherein the cache latch is disposed on the second peripheral circuit region.

4. The non-volatile memory device of claim 2 or claim 3, wherein the first page buffer circuit includes a force latch, an upper-bit latch, and a lower-bit latch, and

wherein the force latch, the upper-bit latch, and the lower-bit latch are disposed on the first peripheral circuit region.

5. The non-volatile memory device of any one of claims 2 to 4, wherein the first page buffer circuit includes a high-voltage transistor coupled to one of a plurality of bit lines, and

wherein the high-voltage transistor is disposed on the first peripheral circuit region.

6. The non-volatile memory device of claim 2, wherein the first page buffer circuit includes a sensing latch, a cache latch, and a high-voltage transistor that is coupled to one of a plurality of bit lines,

wherein the high-voltage transistor is disposed on the first peripheral circuit region, and

wherein the sensing latch and the cache latch are disposed on the second peripheral circuit region.

7. The non-volatile memory device of any one of claims 2 to 6, wherein the first page buffer circuit includes a page buffer decoder configured to address and drive the first memory cell array, and

wherein the page buffer decoder is disposed on the second peripheral circuit region.

8. The non-volatile memory device of any one of claims 1 to 7, wherein the first peripheral circuit further includes a first row decoder,

wherein a portion of the first row decoder is disposed on the first peripheral circuit region,

wherein another portion of the first row decoder is disposed on the second peripheral circuit region,

wherein the second peripheral circuit further includes a second row decoder, and

wherein the second row decoder is disposed on the second region.

9. The non-volatile memory device of any one of claims 1 to 7, wherein the first semiconductor layer further includes a row decoder coupled to the first plurality of word

lines, and

wherein the second peripheral circuit region overlaps the row decoder in the vertical direction.

10. The non-volatile memory device of any one of claims 1 to 7, wherein the first semiconductor layer further includes a pass transistor circuit coupled to the first plurality of word lines,

wherein the first peripheral circuit further includes a row decoder coupled to the pass transistor circuit, and

wherein the second peripheral circuit region overlaps the pass transistor circuit in the vertical direction.

11. The non-volatile memory device of claim 1, wherein the first peripheral circuit includes a row decoder coupled to the first plurality of word lines,

wherein a portion of the row decoder is disposed on the first peripheral circuit region, and

wherein another portion of the row decoder is disposed on the second peripheral circuit region.

12. The non-volatile memory device of claim 11, wherein the first semiconductor layer further includes a page buffer circuit coupled to the first plurality of memory cells through a plurality of bit lines, and

wherein the second peripheral circuit region overlaps the page buffer circuit in the vertical direction.

13. The non-volatile memory device of any one of claims 1 to 12, wherein the second semiconductor layer further includes a pad region in which a plurality of bonding pads are disposed, and wherein the pad region does not overlap the first cell region and the second cell region.

14. The non-volatile memory device of any one of claims 1 to 13, wherein the second semiconductor layer further includes an external peripheral circuit including a data input/output buffer, and

wherein the external peripheral circuit does not overlap the first cell region and the second cell region.

15. The non-volatile memory device of claim 1, wherein the first peripheral circuit includes a first page buffer circuit and a second page buffer circuit that are coupled to the first memory cell array,

wherein the first page buffer circuit completely overlaps the first cell region in the vertical direction, and wherein the second page buffer circuit partially overlaps the first cell region in the vertical direction.

16. The non-volatile memory device of claim 15, wherein the second page buffer circuit includes a sensing latch, a cache latch, a high-voltage transistor, and a page buffer decoder,

wherein the sensing latch and the high-voltage transistor overlap the first cell region in the vertical direction, and

wherein the cache latch and the page buffer decoder do not overlap the first cell region in the vertical direction.

17. The non-volatile memory device of claim 1, wherein the first peripheral circuit includes a first page buffer circuit and a second page buffer circuit that are coupled to the first memory cell array, and

wherein the first page buffer circuit and the second page buffer circuit partially overlap the first cell region in the vertical direction.

18. A non-volatile memory device, comprising:

a first semiconductor layer that includes:

a memory cell array disposed on a cell region of the first semiconductor layer, wherein the memory cell array includes a plurality of word lines stacked in a vertical direction and a plurality of memory cells respectively coupled to the plurality of word lines; and

a first metal pad; and

a second semiconductor layer that includes:

a peripheral circuit disposed on a peripheral circuit region of the second semiconductor layer; and

a second metal pad,

wherein the second semiconductor layer is coupled, in the vertical direction, to the first semiconductor layer by the first metal pad and the second metal pad in a bonding manner,

wherein the peripheral circuit region includes a first peripheral circuit region that overlaps the cell region in the vertical direction, and a second peripheral circuit region that does not overlap the cell region in the vertical direction,

wherein an area of the peripheral circuit region is greater than an area of the cell

region,

wherein the peripheral circuit includes a page buffer circuit connected to the plurality of memory cells through a plurality of bit lines,

wherein a portion of the page buffer circuit is disposed on the first peripheral circuit region, and

wherein another portion of the page buffer circuit is disposed on the second peripheral circuit region.

19. The non-volatile memory device of claim 18, wherein the page buffer circuit includes a sensing latch and a cache latch,

wherein the sensing latch is disposed on the first peripheral circuit region, and

wherein the cache latch is disposed on the second peripheral circuit region.

20. A non-volatile memory device, comprising:

a first semiconductor layer that includes a cell region on which a memory cell array is disposed, and a first metal pad, wherein the memory cell array includes a plurality of word lines stacked in a vertical direction and a plurality of memory cells respectively coupled to the plurality of word lines; and

a second semiconductor layer that includes a peripheral circuit region on which a peripheral circuit is disposed, and a second metal pad, wherein the second semiconductor layer is coupled, in the vertical direction, to the first semiconductor layer by the first metal pad and the second metal pad in a bonding manner,

wherein the peripheral circuit region includes a first peripheral circuit region that overlaps the cell region in the vertical direction, and a second peripheral circuit region that does not overlap the cell region in the vertical direction,

wherein an area of the peripheral circuit region is greater than an area of the cell region,

wherein the peripheral circuit further includes a row decoder connected to the plurality of word lines,

wherein a portion of the row decoder is arranged in the first peripheral circuit region, and

wherein another portion of the row decoder is arranged in the second peripheral circuit region.