

## Description

Method and arrangement for converting memory addresses  
5 into memory selection signals

In processor-controlled devices, a memory - usually  
dynamic or static RAMs (Random Access Memory) - is  
provided for the storage of programmes and data. In order  
10 to write data to memory areas of the memory or read data  
from the individual memory areas, the processor generates  
a memory area address and passes it to a memory control-  
ler - known as an SRAM or DRAM controller to technical  
specialists. The memory controller forwards this memory  
15 area address via address lines to address inputs of the  
memory. The memory area addresses generally represent a  
binary number, the smallest addressable memory area  
usually comprising one or more bytes.

The memory is formed by a plurality of insertion  
20 regions, into which in each case at least one memory  
module - usually an integrated memory chip - can be  
inserted. The insertion regions, which are realized by  
plug-in devices, are frequently configured in such a way  
that memory modules or memory chips having different  
25 storage capacities can be inserted - for example memory  
modules with 1 or 4 Kbytes or Mbytes. Consequently, by  
virtue of different population of the insertion regions,  
optimum matching of the storage capacity of the memory to  
the respective application is possible. This means that  
30 the memory modules must be inserted into the address-  
conforming insertion regions as a function of their  
storage capacity in order to ensure error-free memory  
addressing. Incorrect population as regards the storage  
capacity and the insertion regions leads to the [sic]  
35 considerable disturbances in the processor system and/or  
to its failure.

The object on which the invention is based  
consists in ensuring memory addressing which is suitable  
for the memory configuration, starting from the memory

area address generated by the processor and taking account of a flexible configuration of the memory. The object is achieved by means of the features of Claim 1.

The essential aspect of the method according to the invention is to be seen in the formation of conversion information items with the aid of which the memory area addresses generated by the processor are converted into memory selection signals which are co-ordinated with the current memory configuration. In this case, capacity information items, assigned to each inserted memory module and one indicating the storage capacity of the respective memory modules, and configuration information items, indicating the presence of inserted memory modules, of all the insertion regions are acquired in each case and logical capacity information items indicating the address space as a function of the acquired configuration information item [sic] and logical configuration information items indicating the virtual configuration of the memory are derived from the acquired capacity information items and the configuration information items. The logical capacity information items represent, together with the configuration information items, the conversion information items.

In the case of an m-digit, binary memory area address, n most significant digits are provided for the configuration of  $2^n$  insertion regions, it being possible to insert memory modules having a total storage capacity of  $2^{m-n}$  addressable memory areas into each insertion region, and one capacity and one configuration information item is acquired for each insertion region - Claim 2. This division takes account of memory modules having  $2^x$  storage capacity gradations. Other storage capacity gradations are possible but lead to addressing restrictions and to increased complexity for a realization of the method according to the invention.

According to an advantageous development of the method according to the invention, it is possible to insert memory modules having two different storage capacities, the larger storage capacity comprising  $2^{m-n}$

addressable memory areas and the smaller storage capacity comprising  $2^{m-n-k}$  ( $k, l, m, n = 1, 2, \dots$ ) addressable memory areas. The memory modules having the larger storage capacity are, beginning with the insertion region with  
5 the smallest assigned memory area addresses, progressively inserted into the insertion regions with the next more significant assigned memory area addresses. The acquired capacity information items are represented by a binary capacity information item indicating the small or  
10 large storage capacity, and the configuration information item is represented by a binary configuration information item indicating the presence or absence of an inserted memory module - Claim 3. Although this restriction permits incorrect population, it nevertheless reduces the  
15 storage capacity of the incorrectly mounted memory modules. Furthermore, the restriction makes it possible to realize a conversion device even more simply, i.e. more economically.

A further aspect which is essential to the  
20 invention is to be seen in the use of the conversion information items for converting memory area addresses formed by a processor-controlled device into memory selection signals which are co-ordinated with a structure and storage capacity of a memory, the memory being formed  
25 by memory modules which have uniform and/or different storage capacities and are each inserted into a physical insertion region. For this purpose, an insertion region-related logical memory selection signal is derived from  $n+k$  digits, referring to the configuration of the memory,  
30 of a currently present  $m$ -digit memory area address with the aid of logical capacity information items derived from capacity information items which indicate the storage capacity and with the aid from [sic] logical configuration information items derived from con-  
35 figuration information items which indicate the virtual memory configuration, and, with the aid of the configuration information items, a physical memory selection signal is derived from the insertion region-related logical memory selection signal for the relevant inser-

tion region.

Further advantageous refinements of the method according to the invention both for forming conversion information items and for converting the memory area address into memory selection signals as well as arrangements for carrying out the methods according to the invention can be found in the further claims.

The invention is explained in more detail below with reference to graphical illustrations, in which

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FIG 1 shows a configuration of a memory with the conversion device according to the invention,

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FIG 2 shows a block diagram of the conversion device,

FIG 3 shows the first shifting stage for forming the logical capacity and configuration information items,

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FIG 4 shows a capacity correction stage for forming correction information items,

FIG 5 show, in a block diagram, a module selection unit

FIG 6 for forming logical memory selection signals, and

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FIG 7 shows a second shifting stage for forming physical memory selection signals.

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FIG 1 shows a configuration, assumed for the exemplary embodiment, of a memory SP, which is formed by four insertion regions EB1..4, i.e.  $n = 2$ . Memory modules SM having a predetermined storage capacity K1 or four times the predetermined storage capacity K4 can be inserted or plugged into each of these insertion regions EB1..4, which are generally realized by plug-in locations, - .e.  $k = 2$  -, the predetermined storage capacity K1 being, for example, 1 Mbyte. Of the 24 - i.e.  $m = 24$  - address lines ADL required for addressing,  $n+k$ , in the exemplary embodiment four, most significant address lines AD0..3

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are passed to a conversion device KVE. The remaining n-m address lines ADL2..m, which are likewise passed in parallel to the insertion regions EB1..4, are passed directly to the memory SP. The conversion device KVE is  
5 connected, via two lines which communicate a logical capacity and a logical configuration information item lki, lkoi, to a device EBK for forming conversion information items, in which device supplied capacity and configuration information items ki, koi are acquired. The  
10 conversion device KVE and the device EBK for forming configuration information items each constitute a separate unit or a subunit of a memory controller SPA, whose further functions (not illustrated) correspond to the known DRAM or SRAM controllers. For the exemplary embodiment, it will furthermore be determined that first the  
15 memory modules SM having the larger and then having the smaller storage capacity K4,1 are to be inserted into the insertion regions EB1..4, beginning with the first insertion region EB1. In the exemplary embodiment, the  
20 current configuration, which is co-ordinated with an application, is determined by a memory module SM having the large storage capacity K4 inserted in the first and third insertion regions EB1,3 and by a memory module SM having the small storage capacity K1 inserted into the  
25 fourth insertion region EB4, no memory module SM being inserted into the second insertion region EB2.

FIG 2 shows the device EBK for forming conversion information items, having a first shifting stage VS1, to which are passed the capacity information items ki  
30 indicating the storage capacity K1,4 and configuration information items (koi) indicating the presence of memory modules (SM) inserted into the respective insertion regions EB1..4. Logical capacity information items lki that have been determined are communicated via a first  
35 output A1 of the first shifting stage VS1 and logical configuration information items lkoi via a second output A2 to a capacity correction stage KKS arranged in a conversion device KVE. The corrected capacity information items klki pass via an output A of the capacity correc-

tion stage KKS to a second input E2 of a module selection unit MAE, which is likewise arranged in the conversion device KVE and to whose first input E1 are passed those n address lines AD0..1 by means of which the memory modules SM inserted into insertion regions EB1..4 are addressed. In the exemplary embodiment, the four most significant address lines ADL0..3 are passed to the module selection unit MAE. The logical memory selection signals lsas formed in the module selection unit MAE pass via an output A of the latter to a first input E1 of a second shifting stage VS2, which is likewise arranged in the conversion device KVE and at whose output A the memory selection signal sas is present, by means of which the respective relevant insertion region EB1..4 is addressed as a function of the currently present memory area address AD0..m.

FIG 3 shows, in a block diagram, the first shifting stage VS1, four capacity information items ki, which in each case indicate the small or large storage capacity K1,4 for each insertion region EB1..4, being passed to a multiplexer MUX via four capacity lines SZ0..3 and four configuration information items koi, which indicate the presence of memory modules SM in the insertion regions EB1..4, being passed to the said multiplexer MUX via four presence lines VL0..3. The multiplexer MUX has three shift stages S1..3, the third shift stage S3 containing two times two (1..4) multiplex elements MX, the second shift stage S2 in each case containing three (5..10) multiplex elements MX and the first shift stage S1 in each case containing four (11..18) multiplex elements MX. In each case half of the multiplex elements MX are assigned to the capacity lines SZ0..3 and the other half are assigned to the presence lines VL0..3. A multiplex element MX has two inputs - indicated by arrows -, one output and a control input - indicated by the designation ST -, it being the case that when a binary 0 information item is applied to the control input ST, the signals present at the upper input are switched to the output and when a binary 1 informa-

tion item is applied to the control input ST, the signals present at the lower input are switched to the output.

In the third shift stage S3, the fourth presence line VL3 is connected to respectively one input of a first multiplex element MX(1), the second input of which  
5 is connected to 0 potential, and to one input of a second multiplex element MX(2), the second input of which is connected to the third presence line VL2. In the third shift stage S3, furthermore, the fourth capacity line SZ3  
10 is connected to a third multiplex element MX(3), the second input of which is connected to 0 potential, and to a fourth multiplex element MX(4), the second input of which is connected to the third capacity line SZ2. In the second shift stage S2, the output of the first multiplex  
15 element MX(1) is connected to the upper input of the fifth and to the lower input of the sixth multiplex element MX(5,6), 0 potential being connected to the lower input of the fifth multiplex element MX(5). The output of the second multiplex element MX(2) is connected to the  
20 upper input of the sixth and to the lower input of the seventh multiplex element MX(6,7), the upper input of which is connected to the second presence line VL1. The inputs of the eighth to tenth multiplex elements MX(8..10) are connected to the outputs of the third and  
25 fourth multiplex elements MX(3,4) in the same way as described above.

In the third shift stage S3 [sic], the output of the fifth multiplex element MX(5) is connected to the upper input of the eleventh and to the lower input of the  
30 twelfth multiplex element MX(11,12), the lower input of the eleventh multiplex element MX(11) being connected to 0 potential. The output of the sixth multiplex element MX(6) is passed to the upper input of the twelfth and to the lower input of the thirteenth multiplex element  
35 MX(12,13), and the output of the seventh multiplex element MX(7) is passed to the upper input of the thirteenth and to the lower input of the fourteenth multiplex element MX(13,14), the upper input of the fourteenth multiplex element MX(14) being connected to the first

presence line VL0. In an analogous manner, the outputs of the eighth to tenth multiplex elements MX(8..10) and the first capacity line SZ0 are connected to the upper and lower inputs of the fifteenth to eighteenth multiplex elements MX(15..18).

An inverter IN1 is connected to the first presence line VL0, the output of which inverter is passed to all the control inputs ST of the multiplex elements MX(11..18) arranged in the first shift stage S1. In a manner analogous to this, the control inputs ST of the second shift stage S2 are connected via a second inverter IN2 to the second presence line VL1 and the control inputs ST of the third shift stage S3 are connected via a third inverter IN3 to the third presence line DL2.

The outputs of the fourteenth to eleventh multiplex elements MX(14..11) represent the logical presence lines LVL0..3, on which the logical configuration information items lkoi are available. The outputs of the eighteenth to fifteenth multiplex elements MX(18..15) represent the logical capacity lines LSZ0..3, on which the logical capacity information items lki are present.

Under the assumption that in the case of the capacity information item ki a binary 1 information item represents a storage capacity of 4 Mbytes and a 0 information item represents a storage capacity of 1 Mbyte, in the exemplary embodiment a 1 information item is present on the first capacity line SZ0, a 0 information item is present on the second capacity line SZ1, a 1 information item is present on the third capacity line SZ2 and a 0 information item is present on the fourth capacity line SZ4. Under the further assumption that in the case of the configuration information item koi a 0 information item indicates the absence and a 1 information item the presence of an inserted memory module SM, referring to the exemplary embodiment a binary 1 information item is present on the first presence line VL0, a binary 0 information item is present on the second presence line VL1, a binary 1 information item is present on the third presence line VL2 and a binary 1 information item is

present on the fourth presence line VL3. This means that, in the second shift stage S2, the information that is present is shifted in the direction addresses less significant direction, since no memory module SM is  
5 inserted or plugged into the second insertion region EB2.

Consequently, a logical capacity information item lki formed by binary information items is present on the logical capacity lines LSZ(0..3) - a binary 1100 bit combination. The logical configuration information item  
10 lkoi is likewise present in binary form on the logical presence lines LVL0..3 - a binary 1110 bit combination.

FIG 4 shows, in a block diagram, the capacity correction stage KKS. In this, each of the logical capacity lines LSZ0..3 is connected to a first to fourth  
15 AND gate &(1..4). The four logical presence lines LV0..3 are respectively connected to a further input of the first to fourth AND gates &(1..4) and respectively connected to an input of a fifth to eighth AND gate &(5-8). The output of the first AND gate &(1) is passed  
20 to a further input of the second and to a further inverting input of the fifth AND gate &(2,5). The output of the second AND gate &(2) is connected to a further input of the third and to a further inverting input of the sixth AND gate &(3,6). In a manner analogous to this, the  
25 output of the third AND gate &(3) is connected to a further input of the fourth and to a further inverting input of the seventh AND gate &(4,7). The output of the fourth AND gate &(4) is passed to a further inverting input of the eighth AND gate &(8). The four outputs  
30 K4(0..3) of the four AND gates &(1..4) constitute capacity lines on which logical capacity information items klki referring to the large storage capacity K4 are indicated. These capacity lines are subsequently designated as K4 lines. The outputs of the fifth to eighth AND  
35 gates &(5..8) represent capacity lines K1(0..3) which refer to the small storage capacity K1 and on which logical capacity information items klki referring to the small storage capacity are present. The information items present at the eight outputs of the eight AND gates

&(1..8) usually represent the corrected logical capacity information klki, only the logical capacity information items klki referring to the large memory area being required in the exemplary embodiment. Referring to the  
5 exemplary embodiment, a binary 1100 bit combination is present on the K4 lines K4(0..3) provided for this. In this correction stage KKS, furthermore, correction is effected to the extent that as regards the population conditions - insertion of memory modules SM beginning  
10 with the addresses most significant insertion region EB1..4 - erroneous population is corrected. If, for example, a memory module SM having the low storage capacity K1 is inserted into the second insertion region EB2, then inserted memory modules SM only having the low  
15 storage capacity K1 are taken into account for the third and fourth insertion regions EB3,4, although memory modules SM having the large storage capacity K4 are possibly inserted. This means a storage capacity correction from actual to logically present storage capacity  
20 K1,4.

The components illustrated in Figure 5 and Figure 6 together show the module selection unit MAE - see Figure 2. In Figure 5, the two least significant address lines ADL2,3 of the n+k most significant address  
25 lines ADL0-3 are passed to a first decoding unit DK-1, and the two more significant address lines ADL0,1 are passed to a second decoding unit DK-4. In these decoding units DK-1, DK-4, the two address lines ADL0,1, ADL2,3 are in each case decoded on four output lines A1..4  
30 respectively assigned to an insertion region EB1..4. This means that one of the output lines A1..4 is actively connected, that is to say has a binary 1 information item, in accordance with the binary address information items AD0..3 - binary 0 or 1 information items - present  
35 on the address lines ADL0,1, ADL2,3.

The output lines A1..4 of the second decoding unit DK-4 are respectively connected to one input of four AND gates &(1..4). The second to fourth output lines A2..4 are additionally respectively connected to one

input of fifth to seventh AND gates &(5..7). The four output lines A1..4 of the first decoding unit DK-1 are passed to a first shift stage S1 and in this are connected in each case to one input of two multiplex elements MX. The remaining free input of the fourth multiplex element MX is coupled to zero potential 0. The output of the least significant multiplex element MX is connected to an input of an eighth AND gate &(8) and the outputs of the three further multiplex elements MX are connected to in each case one input of multiplex elements MX of a second shift stage S2. The output of the least significant multiplex element MX is passed to a ninth AND gate &(9) and the outputs of the two remaining multiplex elements MX are in each case guided to one input of two further multiplex elements MX, which form a third shift stage S3. The output of the less significant multiplex element MX is connected to the input of a tenth AND gate &(10) and the output of the remaining multiplex element MX is connected to an input of an eleventh AND gate &(11).

The further input of the fourth AND gate &(4) is connected to the fourth K4 line K4(3) and a further input of the third AND gate &(3) is connected to the further input of the seventh AND gate &(7), the third K4 line K4(2) and to the control input ST of the third shift stage S3. In a manner analogous to this, a further input of the second AND gate &(2) is passed to a further input of the sixth AND gate &(6), to the second K4 line K4(1) and to the control input ST of the second shift stage S2. A further input of the first AND gate &(1) has a connection to a further input of the fifth AND gate &(5), the first K4 line K4(0) and a control input ST of the first shift stage S1. Furthermore, the outputs of the fifth to seventh AND gates &(5..7) are combined in a first OR gate OD1, the output of which is connected to an enable input EN of the first decoding unit DK-1. The outputs of the first to fourth AND gates &(1..4) are coupled to a second OR gate OD2, the inverting output of which are [sic] connected to in each case one further input of the eighth

to eleventh AND gates &(8..11).

At the outputs EN4(0..3) of the four AND gates &(1..4), a binary information item is present which indicates whether, for the address information items  
5 AD0,1 currently appearing on the address lines ADL0,1, a memory module SM having the capacity K4 is available at one of the four insertion regions EB1..4. At the outputs EN1(0..3) of the eighth to eleventh AND gates &(8..11), logical information items are likewise present regarding  
10 whether, for the address information items AD2,3 currently present on the address lines ADL2,3, a memory module SM having the small capacity K1 is available at one of the four insertion regions EP1..4.

Figure 6 shows four OR gates OD(1..4), to one  
15 input of which the respective output EN4(0..3) of the first to fourth AND gates &(1..4) - see Figure 5 - is passed and to the further input of which a respective output EN1(0..3) of the eighth to eleventh AND gates &(8..11) is passed. The outputs of the four OR gates  
20 OD1(1..4) are respectively connected to one input of four AND gates &(1..4). One of the four logical presence lines LVL0..3 is respectively passed to the further inputs of the four AND gates &(1..4). The logical memory selection signal lsas is now present at the outputs LEN0..3 of the  
25 four AND gates &(1..4). This logical memory selection signal lsas indicates in binary form which insertion region EB1..4 is to be logically selected.

The conversion of the logical memory selection signal lsas into the physical memory selection signal sas  
30 is illustrated in Figure 7. For this purpose, the four presence lines VL0..3 - see Figure 3 - are passed to a third decoding unit DK-3. The four outputs A1..A4 of the third decoding unit DK-3 are respectively connected to a control input ST of four shift stages S1..4.

35 The outputs LEN0..3 of the four AND gates &(1..4) - see Figure 6 - are connected as follows to the four shift stages S1..4:

- output LEN0 to one input of the fourth shift stage S4,

- output LEN1 to one input of the fourth and third shift stages S3, S4,
- the output LEN2 to one input of the second, third and fourth shift stages S2..4, and
- 5 - LEN3 to in each case one input of all four shift stages S1..4.

The remaining inputs of the respective four inputs of the four shift stages S1..4 are connected to 0 potential.

10       The shift stages S1..4 are realized in the same way as illustrated in Figure 3 or 5. A decoding table (not illustrated) is stored in the third decoding unit DK-3 and is used to drive the shift stages S1..4 in such a way that the memory selection signal sas is present in  
15 binary form at the four outputs EN0..3 of the four shift stages S1..4, in each case one output EN0..3 being connected separately to an insertion region EB1..4. This means that one of the four outputs EN0..3 has a binary 1 information item by means of which the memory module SM  
20 inserted into the relevant insertion region EB1..4 is selected, that is to say enabled. Together with the address information items AD2-m of the remaining address lines ADL2-m, the sub-memory area in the enabled memory module SM is selected and data communicated from the  
25 microprocessor MP are stored or data are read and communicated to the microprocessor MP. Referring to the exemplary embodiment, the memory module SM inserted in the third insertion region EB3 is enabled, that is to say addressed.



## Patent Claims

1. Method for forming conversion information items  
5 (lki,lkoi) for converting memory area addresses (AD0..m) formed by a processor-controlled device into memory selection signals (sas) which are co-ordinated with a structure and storage capacity of a memory (SP),  
- in which the memory (SP) is formed by memory modules  
10 (SM) which have uniform and/or different storage capacities (Kl,4) and are each inserted into a physical insertion region (EB1..4) of the memory (SP), the memory (SP) comprising at least two insertion regions (EP1..4),  
15 - in which the capacity information items (ki), assigned to each inserted memory module (SM) and one indicating the storage capacity (Kl,4) of the respective inserted memory modules (SM), and configuration information items (koi), indicating the presence of inserted memory  
20 modules (SM), of all the insertion regions (EB1..4) are acquired in each case, and  
- in which logical capacity information items (lki) indicating the address space as a function of the acquired configuration information item [sic] (koi) and  
25 logical configuration information items (lkoi) indicating the virtual configuration of the memory (SP) are derived from the acquired capacity information items (ki) and the configuration information items (koi),  
- the logical capacity together with the configuration  
30 information items (lki,lkoi) representing the conversion information items.
2. Method according to Claim 1, characterized  
- in that, in the case of an m-digit, binary memory area  
35 address (AD0..m), n most significant digits are provided for the configuration of  $2^n$  insertion regions (EB1..4),  
- it being possible to insert memory modules (SM) having a total storage capacity of  $2^{m-n}$  addressable memory areas into each of the  $2^n$  insertion region [sic]



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(EB1..4), and

- in that one capacity and one configuration information item (ki,koi) is acquired for each insertion region (EB1..4).

5 3. Method according to Claim 2, characterized

- in that it is possible to insert memory modules (SM) having two different storage capacities (K1,4), the larger storage capacity (K4) comprising  $2^{m-n}$  addressable memory areas and the smaller storage capacity (k1) comprising  $2^{m-n-k}$  [sic] (k,m,n = 1,2..) addressable memory areas,
- in that the memory modules (SM) having the larger storage capacity (K4) are, beginning with the insertion region (EB1..4) with the smallest assigned memory area addresses (AD0..3), progressively inserted into the insertion regions (EB1..4) with the next more significant assigned memory area addresses (AD0..3),
- in that the acquired capacity information items (ki) are represented by a binary information item indicating the small or large storage capacity (K1,4),
- and the configuration information item (koi) is represented by a binary information item indicating the presence or absence of an inserted memory module (SM).

20 4. Method according to Claim 3, characterized

- 25 - in that following the insertion of memory modules (SM) into the insertion regions (EB1..4), the logical capacity information items (lki) are formed in such a way
- that, starting from the insertion regions (EB1..4) having an inserted memory module (SM) and with the assigned lowest memory area addresses (AD0..3), given the presence of a configuration information item (koi) indicating an inserted memory module (SM), the respectively acquired binary capacity information items (ki)
- 30 are subjected to binary addition and represent a binary number which indicates the usable address space of the memory (SP) by the binary sum of the large storage capacities (K4).

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5. Method according to Claim 4, characterized



- in that, in the case of insertion regions (EB1..4) without any inserted memory modules (SM), the logical capacity information (lki) and the logical configuration information (lkoi) as a function of the presence of inserted memory modules (SM) is effected [sic] by shifting the binary capacity and configuration information items (ki,koi), indicating the storage capacity (K1,4) of memory modules (SM), in the direction of less significant digits of the multi-digit binary capacity and configuration information items (ki,koi).
6. Arrangement for forming conversion information items (lki,lkoi) for converting memory area addresses (AD0..m) formed by a processor-controlled device into memory selection signals (sas) which are co-ordinated with a structure and storage capacity of a memory (SP),
- in which the memory (SP) is formed by memory modules (SM) which have uniform and/or different storage capacities (K1,4) and are each inserted into a physical insertion region (EB1..4) of the memory (SP), the memory (SP) comprising at least two insertion regions (EB1..4),
- in which capacity and presence lines (SZ,VL), via [lacuna] the capacity information items (ki), assigned to each introduced memory module (SM) and one indicating the storage capacity (K1,4) of the respective inserted memory modules (SM), and configuration information items (koi), indicating the presence of inserted memory modules (SM), of all the insertion regions (EB1..4) are communicated in each case, are connected to a shifting stage (VS1), and
- in which the shifting stage (VS1) is configured in such a way that logical capacity information items (lki) indicating the address space as a function of the acquired configuration information item [sic] (koi) and logical configuration information items (lkoi) indicating the virtual configuration of the memory (SP) are derived from the acquired capacity information items (ki) and the configuration information items (koi),
- the conversion information items representing [lacuna]



logical capacity together with the configuration information items (lki,lkoi) being present at in each case at [sic] one output (A1,2) of the shifting stage (VS1).

- 5     7.        Method for converting memory area addresses (AD0..m) formed by a processor-controlled device into memory selection signals (sas) which are co-ordinated with a structure and storage capacity (K1,4) of a memory (SP),
- 10   - in which the memory (SP) is formed by memory modules (SM) which have uniform and/or different storage capacities (K1,4) and are each inserted into a physical insertion region (EB1..4),
- 15   - in which a logical memory selection signal (lsas) is derived in an insertion region-related manner from n digits, referring to the configuration of the memory, of a currently present m-digit memory area address (AD0..m) with the aid of logical capacity information items (lkio) derived from capacity information items (ki) which indicate the storage capacity (K1,4) and
- 20   with the aid from [sic] logical configuration information items (lkoi) derived from configuration information items (koi) which indicate the virtual memory configuration, and
- 25   - in which, with the aid of the configuration information items (koi), a physical memory selection signal (sas) is derived from the insertion region-related logical memory selection signal (lsas) for the relevant insertion region.
- 30   8.        Method according to Claim 7, characterized
- in that it is possible to insert memory modules (SM) having a total storage capacity of  $2^{m-n}$  addressable memory areas into each of  $2^n$  insertion regions 1..4) [sic],
- 35   - in that logical memory selection signals (lsas1,lsas4) are derived from the n-digit memory area address (AD0..3) with the aid of storage capacity-specific capacity information items (klki), derived from the logical capacity and configuration items (lki,lkoi),



- for each storage capacity (K1,4) provided, and also a logical memory selection signal (lsas) is subsequently formed with the aid of the logical configuration information items (lkoi), and
- 5 - in that a physical memory selection signal (sas) is formed from the logical memory selection signal (lsas), with the aid of the configuration information items ((koi)) for the insertion region (EB1..4) determined and is forwarded to the memory module (SM) of the
- 10 relevant insertion region (EB1..4).
9. Method according to Claim 8, characterized in that, from the logical capacity and configuration information items (lki,lkoi) for every possible storage capacity (K1,4), logical capacity information items
- 15 (klki) specific to the storage capacity and one respectively indicating the logical total storage capacity thereof are formed.
10. Method according to Claim 8 or 9, characterized in that logical memory selection signals (lsas1,4) derived from the currently present address information
- 20 items of the m-digit memory area address (AD0..m) for every storage capacity (K1,4) provided are mapped onto the logical configuration information items (lkoi), thereby forming a logical memory selection signal (lsas).
- 25 11. Method according to one of Claims 8 to 10, characterized in that the configuration information items (koi) control, after having been decoded, the logical memory selection signal (lsas) on the relevant insertion region
- 30 (EB1..4), the controlled logical memory selection signal (lsas) representing the physical memory selection signal (sas).
12. Arrangement for converting memory area addresses (AD0..m) formed by a processor-controlled device into
- 35 memory selection signals (sas) which are co-ordinated with a structure and storage capacity of a memory (SP),
- in which the memory (SP) is formed by memory modules (SM) which have uniform and/or different storage capacities (K1,4) and are each inserted into a physical



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- insertion region (EB1..4),
- in which capacity and configuration lines (LSZ,LVL) communicating logical capacity information items (lki), which indicate the virtual storage capacity, and  
5 logical configuration information items (lkoi), which indicate the virtual memory configuration, are connected to a conversion device (KVE), and
  - in which the conversion device (KVE) is configured in such a way that an insertion region-related logical  
10 memory selection (msas) is derived from n digits, referring to the configuration of the memory, of a currently present m-digit memory area address (AD0..m) with the aid of from [sic] logical capacity information items (lkio) indicating the storage capacity (K1,4) and  
15 with the aid from of [sic] logical configuration information items (lkoi) indicating the virtual memory configuration, and
  - with the aid of the configuration information items (koi), a physical memory selection signal (sas) is  
20 derived from the insertion region-related logical memory selection signal (lsas) for the relevant insertion region (EB1..4), and
  - in which an output (EN0..3), which communicates the memory selection signal (sas), of the conversion device  
25 (KVE) is connected to each insertion region (EB1..4).