ESD PROTECTION CIRCUIT AND SEMICONDUCTOR DEVICE

CROSS-REFERENCE TO RELATED APPLICATION

[0001] This application is a national stage of International Patent Application No. PCT/CN2021/106499, filed on July 15, 2021, which claims priority to Chinese Patent Application No. 202110260635.5 filed on March 10, 2021, and entitled "ESD PROTECTION CIRCUIT AND SEMICONDUCTOR DEVICE", ". The entire contents of International Patent Application No. PCT/CN2021/106499 and Chinese Patent Application 202110260635.5 are the disclosure of which is hereby incorporated by reference in its entirety.

TECHNICAL FIELD

[0002] The present application relates to the technical field of integrated circuits, and in particular to but is not limited to, an ESD protection circuit and a semiconductor device.

BACKGROUND

[0003] In recent years, with the rapid development of integrated circuit technology, a line width of a metal oxide semiconductor (MOS) transistor has become narrower and narrower, a junction depth has become shallower and shallower, and a thickness of a gate oxide layer has become less and less. These have increased a need of a circuit design for electro-static discharge (ESD) protection. When the line width is 1 μm, an ESD event has little impact on a circuit, when the line width is 0.18 μm or 0.13 μm, especially when the line width is less than 90 nm, ESD has become an urgent problem.

[0004] FIG. 1A is a schematic structural diagram of an existing circuit. Referring to FIG. 1A, an internal circuit 10 is electrically connected to a first pad VDD and a second pad VSS, respectively. When static electricity is generated on one of the pads (such as the first pad VDD), the static electricity will flow through the internal circuit 10, thereby causing the internal circuit 10 to be damaged by the static electricity.

[0005] In order to prevent the internal circuit from being damaged by the static electricity, a clamp circuit including a clamp transistor is usually used as a protection