CLAIMS

1. A data receiving circuit, comprising:

a first amplification module, configured to: receive an enable signal, a feedback signal, a data signal, a first reference signal, and a second reference signal; when the enable signal is at a first level, in response to a sampling clock signal and on the basis of the feedback signal, select the data signal and the first reference signal for first comparison and output a first signal pair as a result of the first comparison, or select the data signal and the second reference signal for second comparison and output a second signal pair as a result of the second comparison; and when the enable signal is at a second level, perform the first comparison in response to the sampling clock signal, and output the first signal pair; wherein, the first signal pair comprises a first signal and a second signal, and the second signal pair comprises a third signal and a fourth signal; and

a second amplification module, configured to receive output signals of the first amplification module as an input signal pair, perform amplification processing on a voltage difference of the input signal pair, and output a first output signal and a second output signal as a result of the amplification processing.

2. The data receiving circuit according to claim 1, wherein the first amplification module comprises:

an amplification unit, provided with a first node, a second node, a third node, and a fourth node respectively configured to output the first signal, the second signal, the third signal, and the fourth signal in response to the sampling clock signal, wherein the amplification unit is configured to receive the data signal, the first reference signal, and the second reference signal; and

a decision equalization enable unit, connected between the first node and the second node as well as between the third node and the fourth node, and configured to: receive the enable signal and the feedback signal; when the enable signal is at the first level, on the basis of the feedback signal, turn on a connection path between the first node and the second node, or turn on a connection path between the third node and the fourth node; and when the enable signal is at the second level, turn off the connection path between the

first node and the second node, and turn off the connection path between the third node and the fourth node.

3. The data receiving circuit according to claim 2, wherein the sampling clock signal comprises a first sampling clock signal and a second sampling clock signal; and the amplification unit comprises:

a first comparison circuit, provided with the first node and the second node, and configured to receive the data signal and the first reference signal and perform the first comparison in response to the first sampling clock signal;

a clock generation circuit, configured to receive the enable signal and an original sampling clock signal and output the second sampling clock signal, wherein when the enable signal is at the first level, a phase of the second sampling clock signal is opposite to a phase of the original sampling clock signal, and when the enable signal is at the second level, the second sampling clock signal is a logic high-level signal; and

a second comparison circuit, provided with the third node and the fourth node, and configured to: receive the data signal and the second reference signal; when the enable signal is at the first level, perform the second comparison in response to the second sampling clock signal; and when the enable signal is at the second level, turn on a connection path between the third node and a ground terminal, and turn on a connection path between the fourth node and a ground terminal.

4. The data receiving circuit according to claim 2, wherein the feedback signal comprises a first feedback signal and a second feedback signal differential to each other; and the decision equalization enable unit comprises:

a first enable unit, configured to be turned on in response to the enable signal and the first feedback signal, so as to connect the first node and the second node; and

a second enable unit, configured to be turned on in response to the enable signal and the second feedback signal, so as to connect the third node and the fourth node;

wherein, when the enable signal is at the first level, the first enable unit or the second enable unit is turned on, and when the enable signal is at the second level, the first enable

unit and the second enable unit are both turned off.

5. The data receiving circuit according to claim 4, wherein the first enable unit comprises:

a ninth P-channel metal oxide semiconductor (PMOS) transistor and a tenth PMOS transistor, the ninth PMOS transistor being provided with one end connected to the first node, a gate for receiving a complementary enable signal, and the other end connected to one end of the tenth PMOS transistor, the tenth PMOS transistor being provided with the other end connected to the second node and a gate for receiving the first feedback signal, and a level of the complementary enable signal being opposite to a level of the enable signal.

6. The data receiving circuit according to claim 5, wherein the first enable unit further comprises:

a ninth N-channel metal oxide semiconductor (NMOS) transistor and a tenth NMOS transistor, the ninth NMOS transistor being provided with one end connected to the first node, a gate for receiving the enable signal, and the other end connected to one end of the tenth NMOS transistor, the tenth NMOS transistor being provided with the other end connected to the second node and a gate for receiving a first complementary feedback signal, and a level of the first complementary feedback signal being opposite to a level of the first feedback signal.

7. The data receiving circuit according to claim 4, wherein the second enable unit comprises:

an eleventh PMOS transistor and a twelfth PMOS transistor, the eleventh PMOS transistor being provided with one end connected to the third node, a gate for receiving a complementary enable signal, and the other end connected to one end of the twelfth PMOS transistor, the twelfth PMOS transistor being provided with the other end connected to the fourth node and a gate for receiving the second feedback signal, and a level of the complementary enable signal being opposite to a level of the enable signal.

8. The data receiving circuit according to claim 7, wherein the second enable unit further comprises:

an eleventh NMOS transistor and a twelfth NMOS transistor, the eleventh NMOS transistor being provided with one end connected to the third node, a gate for receiving the enable signal, and the other end connected to one end of the twelfth NMOS transistor, the twelfth NMOS transistor being provided with the other end connected to the fourth node and a gate for receiving a second complementary feedback signal, and a level of the second complementary feedback signal being opposite to a level of the second feedback signal.

9. The data receiving circuit according to claim 3, wherein the first comparison circuit comprises:

a first current source, connected between a power supply node and a fifth node and configured to provide a current to the fifth node in response to a first sampling clock signal;

a first comparison unit, connected to the first node, the second node, and the fifth node, and configured to receive the data signal and the first reference signal, perform the first comparison when the first current source provides the current to the fifth node, and output the first signal and the second signal; and

a first reset unit, connected to the first node and the second node and configured to reset the first node and the second node in response to the first sampling clock signal; and the second comparison circuit comprises:

a second current source, connected between the power supply node and a sixth node and configured to provide a current to the sixth node in response to a second sampling clock signal;

a second comparison unit, connected to the third node, the fourth node, and the sixth node, and configured to receive the data signal and the second reference signal, perform the second comparison when the second current source provides the current to the sixth node, and output the third signal and the fourth signal; and

a second reset unit, connected between the third node and the fourth node and

configured to reset the third node and the fourth node in response to the second sampling clock signal.

10. The data receiving circuit according to claim 9, wherein the first current source comprises:

a first PMOS transistor, connected between the power supply node and the fifth node and provided with a gate for receiving the first sampling clock signal; and

the second current source comprises:

a second PMOS transistor, connected between the power supply node and the sixth node and provided with a gate for receiving the second sampling clock signal.

11. The data receiving circuit according to claim 9, wherein the first comparison unit comprises:

a third PMOS transistor, connected between the first node and the fifth node and provided with a gate for receiving the data signal; and

a fourth PMOS transistor, connected between the second node and the fifth node and provided with a gate for receiving the first reference signal; and

the second comparison unit comprises:

a fifth PMOS transistor, connected between the third node and the sixth node and provided with a gate for receiving the data signal; and

a sixth PMOS transistor, connected between the fourth node and the sixth node and provided with a gate for receiving the second reference signal.

12. The data receiving circuit according to claim 9, wherein the first reset unit comprises:

a first NMOS transistor, connected between the first node and the ground terminal and provided with a gate for receiving the first sampling clock signal; and

a second NMOS transistor, connected between the second node and the ground terminal and provided with a gate for receiving the first sampling clock signal; and

the second reset unit comprises:

a third NMOS transistor, connected between the third node and the ground terminal and provided with a gate for receiving the second sampling clock signal; and

a fourth NMOS transistor, connected between the fourth node and the ground terminal and provided with a gate for receiving the second sampling clock signal.

13. The data receiving circuit according to claim 3, wherein the clock generation circuit comprises:

a first NAND gate circuit, provided with one input terminal for receiving the original sampling clock signal, the other input terminal connected to a power supply node, and an output terminal for outputting the first sampling clock signal~~.~~; and

~~14. The data receiving circuit according to claim 3, wherein the clock generation circuit comprises:~~

a second NAND gate circuit, provided with one input terminal for receiving the original sampling clock signal, the other input terminal for receiving the enable signal, and an output terminal for outputting the second sampling clock signal.

~~15~~14. The data receiving circuit according to claim 1, wherein the second amplification module comprises:

a first input unit, connected to a seventh node and an eighth node, and configured to receive the first signal pair for third comparison and provide signals to the seventh node and the eighth node, respectively, as a result of the third comparison;

a second input unit, connected to the seventh node and the eighth node, and configured to receive the second signal pair for fourth comparison and provide signals to the seventh node and the eighth node, respectively, as a result of the fourth comparison; and

a latch unit, connected to the seventh node and the eighth node, and configured to amplify and latch a signal of the seventh node and a signal of the eighth node, and output the first output signal and the second output signal respectively through a first output node and a second output node.

~~16~~15. The data receiving circuit according to claim ~~15~~14, wherein the first input unit comprises:

a fifth NMOS transistor, provided with a drain connected to the seventh node, a source connected to a ground terminal, and a gate for receiving the first signal; and

a sixth NMOS transistor, provided with a drain connected to the eighth node, a source connected to the ground terminal, and a gate for receiving the second signal; and

the second input unit comprises:

a seventh NMOS transistor, provided with a drain connected to the seventh node, a source connected to the ground terminal, and a gate for receiving the third signal; and

an eighth NMOS transistor, provided with a drain connected to the eighth node, a source connected to the ground terminal, and a gate for receiving the fourth signal.

~~17~~16. The data receiving circuit according to claim ~~15~~14, wherein the latch unit comprises:

a thirteenth NMOS transistor and a seventh PMOS transistor, a gate of the thirteenth NMOS transistor and a gate of the seventh PMOS transistor being both connected to the second output node, a source of the thirteenth NMOS transistor being connected to the seventh node, a drain of the thirteenth NMOS transistor and a drain of the seventh PMOS transistor being both connected to the first output node, and a source of the seventh PMOS transistor being connected to a power supply node; and

a fourteenth NMOS transistor and an eighth PMOS transistor, a gate of the fourteenth NMOS transistor and a gate of the eighth PMOS transistor being both connected to the first output node, a source of the fourteenth NMOS transistor being connected to the eighth node, a drain of the fourteenth NMOS transistor and a drain of the eighth PMOS transistor being both connected to the second output node, and a source of the eighth PMOS transistor being connected to the power supply node.

~~18~~17. The data receiving circuit according to claim ~~17~~16, wherein the second amplification module further comprises:

a third reset unit, connected between the power supply node and an output terminal of the latch unit and configured to reset the output terminal of the latch unit~~.~~;

~~19. The data receiving circuit according to claim 18,~~ wherein the third reset unit comprises:

a thirteenth PMOS transistor, connected between the first output node and the power supply node and provided with a gate for receiving the original sampling clock signal; and

a fourteenth PMOS transistor, connected between the second output node and the power supply node and provided with a gate for receiving the original sampling clock signal.

~~20~~18. A data receiving system, comprising:

a plurality of cascaded data transmission circuits, wherein each of the data transmission circuits comprises the data receiving circuit according to any one of claims 1-19, and a latch circuit connected to the data receiving circuit;

an output signal of a previous stage data transmission circuit is used as the feedback signal of a next stage data transmission circuit; and

an output signal of a last stage data transmission circuit is used as the feedback signal of a first stage data transmission circuit.

~~21~~19. The data receiving system according to claim ~~20~~18, wherein the data receiving circuit receives data in response to a sampling clock signal; and the data receiving system comprises four cascaded data transmission circuits, and the sampling clock signals of the data receiving circuits of adjacent stages have a phase difference of 90 degrees~~.~~;

~~22. The data receiving system according to claim 20,~~ wherein the first output signal and the second output signal outputted by the second amplification module of a previous stage data receiving circuit are used as the feedback signal of a next stage data receiving circuit; or, a signal outputted by a previous stage of the latch circuit is used as the feedback signal of a next stage data receiving circuit.

~~23~~20. A memory device, comprising:

a plurality of data ports; and

a plurality of data receiving systems according to any one of claims ~~20~~18-~~22~~19, each of the data receiving systems corresponding to one of the data ports.