CLAIMS

1. A method for forming a memory, comprising:

providing a substrate, in which at least word line structures and active regions are comprised, as well as a bottom dielectric layer and bit line contact layers that are on a top surface of the substrate, bit line contact openings being provided in the bottom dielectric layer, the bit line contact openings exposing the active regions in the substrate, and the bit line contact layers covering the bottom dielectric layer and filling the bit line contact openings;

etching part of the bit line contact layers to form bit line contact layers at different heights;

forming conducting layers on top surfaces of the bit line contact layers, top surfaces of the conducting layers being at different heights in a direction perpendicular to an extension direction of the word line structure, and the top surfaces of the conducting layers being at different heights in the extension direction of the word line structure;

forming top dielectric layers on the top surfaces of the conducting layers; and

sequentially etching part of the top dielectric layers, the conducting layers and the bit line contact layers to form separate bit line structures;

wherein etching part of the bit line contact layers to form the bit line contact layers at different heights comprises:

forming first photolithographic mask layers on the top surfaces of the bit line contact layers;

patterning the first photolithographic mask layers to form spaced patterns in a preset direction,

the preset direction forming an included angle α with the extension direction of the word line structure, and a range of α being $0<\alpha<90°$;

etching part of the bit line contact layers based on the spaced patterns to form the bit line contact layers at different heights; and

removing the spaced patterns.

2. The method for forming a memory of claim 1, wherein the spaced patterns comprise spaced and extending strips, or separate ellipses or rectangles.

3. The method for forming a memory of claim 1, wherein forming the conducting layers on the top surfaces of the bit line contact layers comprises:

forming conducting films on the top surfaces of the bit line contact layers; and

etching the conducting films to form the conducting layers with a same thickness on the top surfaces of the bit line contact layers at different heights.

4. The method for forming a memory of claim 1, wherein forming the top dielectric layers on the top surfaces of the conducting layers comprises:

forming top dielectric films on the top surfaces of the conducting layers; and

planarizing top surfaces of the top dielectric films to form the top dielectric layers, top surfaces of the top dielectric layers being at a same height.

5. The method for forming a memory of any one of claims 1-4, wherein the bit line contact layer filling the bit line contact opening and covering the bottom dielectric layer comprises:

forming a first bit line contact layer filling the bit line contact opening, the first bit line contact layer covering the bottom dielectric layer;

forming a barrier layer on a top surface of the first bit line contact layer at a top of the bottom dielectric layer; and

forming a second bit line contact layer on a top surface of the barrier layer and the top surface of the first bit line contact layer, the second bit line contact layer covering the first bit line contact layer and the barrier layer.

6. A memory, comprising:

a substrate, at least word line structures and active regions being comprised in the substrate;

a bottom dielectric layer, the bottom dielectric layer being at a top of the substrate, bit line contact openings being provided in the bottom dielectric layer, and the bit line contact openings exposing the active regions in the substrate; and

separate bit line structures, top surfaces of the bit line structures being at the same height, and the bit line structure comprising a bit line contact layer at a top of the bottom dielectric layer and in the bit line contact opening, a conducting layer at a top of the bit line contact layer, and a top dielectric layer at a top of the conducting layer,

wherein the conducting layers in the same bit line structure are at different heights in an extension direction of the bit line structure, and the conducting layers in adjacent bit line structures are at different heights in an extension direction of the word line structure.

7. The memory of claim 6, wherein a connecting line of the conducting layers is waved in the extension direction of the bit line structure.

8. The memory of claim 6, wherein the conducting layers in different bit line structures are at the same height in a preset direction, the preset direction forming an included angle α with the extension direction of the word line structure, and a range of α being $0<\alpha<90°$.