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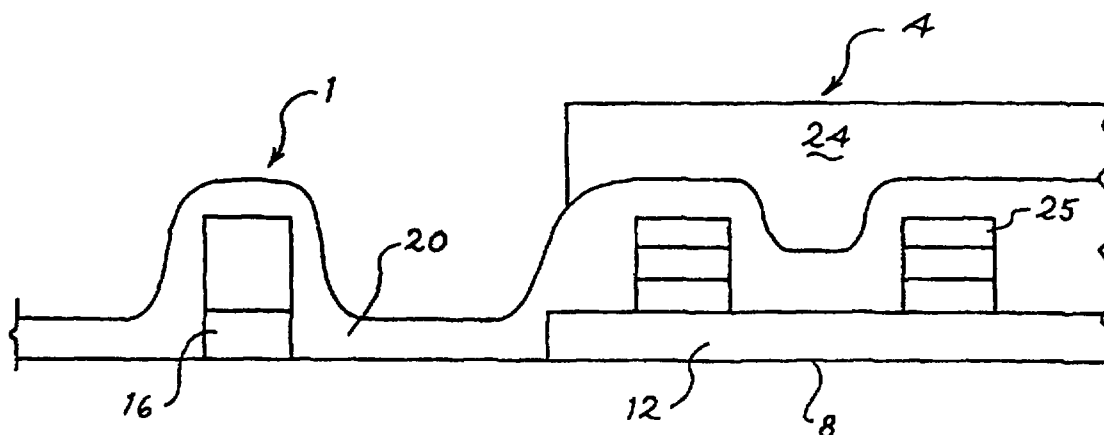
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(57) Abstract: The present invention includes a method for preventing damage to the ONO structure and silicon wafer by applying a mask to cover the core area of an integrated circuit during periphery spacer etching. A further method of the present invention to prevent damage to the ONO structure and silicon wafer comprises applying an exceptionally thick oxide layer above the uppermost layer of the wafer prior to periphery spacer etching. An even further method of the present invention includes a combination of applying an exceptionally thick oxide layer over the uppermost surface of the wafer and further applying a mask over the core area prior to periphery spacer etching.