

CLAIMS

1. A system-on-chip comprising:
 - a processor; and
 - a peripheral device,
- 5 the processor (PROC) being configured to communicate with the peripheral device through a first physical interface module associated with the processor and through a second physical interface module associated with the peripheral device,
 - the first physical interface module having a physical layer comprising a first number of pins and a protocol layer configured to operate according to a standard
 - 10 communications protocol,
 - the second physical interface module having a physical layer comprising a second number of pins and a protocol layer configured to operate according to either the standard communications protocol or a proprietary communications protocol different from the standard communications protocol,
- 15 wherein the first physical interface module comprises a controller configured to
 - select between the standard communications protocol and the proprietary communications protocol based on a protocol selection signal, and
 - whenever the proprietary communications protocol is selected,
 - reconfiguring one or more of the first number of pins to operate according to the
 - 20 proprietary communications protocol,
 - the first physical interface module further comprising a detector configured to monitor the pins of the first physical interface module and to provide the protocol selection signal based on at least one predetermined parameter associated with one or more pins of the first physical interface module.
- 25 2. The system-on-chip according to claim 1, wherein the standard communications protocol is one selected from the group USB 2, USB 3, Ethernet, HDMI, or eSATA.
3. The system-on-chip according to claim 1, wherein the first number is greater than or equal to the second number.
- 30 4. The system-on-chip according to claim 1, wherein the proprietary communications protocol is arranged to provide faster communication in a

communication bus linking the processor and the peripheral device than the standard communication protocol.

5. The system-on-chip according to claim 1 wherein the detector is configured to determine the parameter associated with one or more pins of the first set by measuring an electrical characteristic on at least one of the first number of pins and to provide the protocol selection signal based on the measured electrical characteristic.

6. The system-on-chip according to claim 5 wherein the electrical characteristic is one from the ordered group of current, voltage, impedance, frequency or logical level, the protocol selection signal being based on a comparison of the measured electrical characteristic with a reference electrical characteristic chosen from the ordered group of threshold current, threshold voltage, threshold impedance, reference frequency or reference logical level, respectively.

7. The system-on-chip according to claim 5 wherein the detector is an open circuit detector configured to detect at least one from the first number of pins as being open-circuited, the protocol selection signal depending on whether or not an open circuit is detected.

8. The system-on-chip according to claim 5 wherein the detector comprises a register for receiving a sequence of one or more bits via one or more of the first number of pins, the protocol selection signal being based on a match between a predetermined sequence of one or more bits and the detected sequence of one or more bits.

9. A method for managing communication between a processor and a peripheral device of a system-on-chip, the processor communicating with the peripheral device through a first physical interface module associated with the processor and through a second physical interface module associated with the peripheral device, the first physical interface module having a physical layer comprising a first number of pins and a protocol layer configured to operate according to a standard communications protocol, the second physical interface module having a physical layer comprising a second number of pins and a protocol layer configured to operate according to either the standard communications protocol or a proprietary communications protocol

different from the standard communications protocol, the method comprising:
monitoring, by a detector included in the first physical interface module, the
physical layer of the first physical interface module and providing a protocol selection
signal based on at least one predetermined parameter associated with one or more

5 pins of the first physical interface module,

selecting, by a controller included in the first physical interface module,
between the standard communications protocol and the proprietary communications
protocol based on the protocol selection signal, and

whenever the proprietary communications protocol is selected, reconfiguring
10 one or more of the first number of pins to operate according to the proprietary
communications protocol.

10. The method according to claim 9 wherein the standard communications
protocol is one selected from the group USB 2, USB 3, Ethernet, HDMI, or eSATA.

11. The method according to claim 9 wherein the first number is greater than or
15 equal to the second number.

12. The method according to claim 9 further comprising providing by the
proprietary communications protocol faster communication than the standard
communication protocol in a communication bus linking the processor and the
peripheral device.

20 13. The method according to claim 9 further comprising determining, by the
detector, the parameter associated with one or more pins of the first set by
measuring an electrical characteristic on at least one of the first set of pins and
provides the protocol selection signal, the measured electrical characteristic being
one from the ordered group of current, voltage, impedance, frequency or logical level,
25 the protocol selection signal being based on a comparison of the measured electrical
characteristic with a reference electrical characteristic chosen from the ordered group
of threshold current, threshold voltage, threshold impedance, reference frequency or
reference logical level, respectively

14. The method according to claim 9 further comprising detecting, by the detector, at least one from the first number of pins as being open-circuited, the protocol selection signal depending on whether or not an open circuit is detected.

- 5 15. The method according to claim 9 further comprising receiving by a register of the detector a sequence of one or more bits via one or more of the first number of pins, the protocol selection signal being based on a match between a predetermined sequence of one or more bits and the detected sequence of one or more bits.