

Method for Substantially Uniform Copper Deposition onto Semiconductor Wafer

Cross-reference to related applications

This application is a continuation-in-part of U.S. Application Ser. No. 09/232,864, filed on Jan 15 1999 now U.S. Patent No. 6391166; which claims the benefit of earlier filed U.S. Provisional Application Ser. No. 60/074,466, filed on Feb. 12, 1998, and U.S Provisional Application Ser. No. 60/094,215, filed on Jul. 27, 1998; and this application claims the benefit of PCT. International Patent Application No. PCT/CN2007/071008, filed on Nov. 2, 2007; the entire contents of which are incorporated herein by reference.

Field of Invention

The present invention generally relates to an electrochemical deposition method for electrochemically preparing a uniform copper film on semiconductor substrate bearing a thin resistive seed layer as part of interconnect formation in ULSI (Ultra large scale integrated) circuit fabrication.

Background

Semiconductor devices are manufactured or fabricated on semiconductor wafers using a number of different processing steps to create transistor and interconnection elements. In forming the device elements the semiconductor wafer may undergo, for example, masking, etching, and deposition processes to form the semiconductor transistors and desired electronic circuitry to connect those transistor terminals. In particular, multiple masking, ion implantation, annealing, and plasma etching, and chemical and physical vapor deposition steps can be performed to form shallow trench, transistor well, gate, poly-silicon line, and interconnection line structures such as vias and trenches.

After vias and trenches are formed, conductive materials are deposited into these structures to electrically connect the transistors underneath. Excess conductive materials are then removed to transform the conductive structures into desired circuitry. In forming conductive lines during ULSI (Ultra large scale integrated) circuit fabrication, electrochemical deposition of a metallic layer, usually copper, onto a substrate bearing a thin resistive seed layer is implemented. Such a deposition process can be used to fill via structures, trench structures, or combined structures of both. When these structures are filled, copper is continuously deposited to form a film covering the surface of the semiconductor wafer. A uniform final copper film is critical because the subsequent process step, commonly a planarization step (CMP), to remove the excess conductive copper requires a high degree of uniformity in order to achieve the equal electrical performance from device to device at the end of production line. The within film non-uniformity (WFNU), which is the ratio of the standard deviation of film thickness over the mean film thickness, is generally controlled under 2.5% in advanced process technology.

Large WFNU has a negative effect on the following CMP process step by causing either regional Cu remaining or excessive dielectric materials loss at the end of Cu polishing. If the same amount of Cu is removed evenly across the wafer during polishing, the initial thicker Cu film around the periphery of the wafer leads to Cu or barrier residue to be left there, and this incomplete removal process causes electrical short of the device. If a large amount of over-polishing is enforced to clear Cu and barrier materials on wafer periphery, the regions near wafer center suffer excessive loss of dielectric materials, thereby reducing the height of trenches and vias, which leads to different electrical resistance among the interconnection lines across the wafer.

Both effects can impact device yield substantially.

As wafer size migrates to from 200mm to 300 mm, and seed layer thickness continuously to decrease for every generation of manufacture technology that advances, ohmic resistance of the seed layer on the surface of the semiconductor wafer increases significantly. In conventional electrochemical deposition process, often referred as plating, a power source supplies electrical current or potential to a single working electrode and the wafer substrate bearing a seed layer. The wafer substrate, working electrode, power supply, and the electrolyte form an electrolytic cell. Current density across the thin resistive seed layer is non-uniform, higher at substrate periphery due to a phenomenon called "terminal effect". This current non-uniformity results in higher plating rate at the edge of semiconductor wafer and lower plating rate at the center of semiconductor wafer, which leads to non-uniform thickness of deposited copper film on the surface of semiconductor wafer. Terminal effect is more profound with less seed layer thickness and larger wafer size. In most severe embodiments, deposition only occurs at wafer periphery.

The terminal effect can be reduced by employing an electrolyte solution with relative lower acid content, as shown in FIGURES 3a-3d. However, as technology advances, low acid electrolyte alone fails to solve the non-uniform plating as a result of terminal effect. Often, this non-uniformity can be improved by implementing a film with higher thickness, as shown in FIGURES 3c-3d; however, this will severely limit the productivity of the processing equipment and greatly increase the cost to remove the excessive materials in the subsequent planarization step.

In the earlier patents, sophisticated designs have been

incorporated into processing apparatus to resolve the non-uniformity problem caused by terminal effect. Patent, U.S. Patent 6,391,166 (January. 15, 1999) disclosed plating apparatus and methods that utilized an independent power control for a system of electrodes to overcome the non-uniform plating rate on semiconductor wafer with very thin seed layer. Patent US Patent 6755954 (June 29, 2004) disclosed an apparatus and a method for electroplating of copper film with relatively small thickness variation. It showed an example, to form a 0.6 μ m (6000Å) copper film with 394Å thickness variation on 300mm wafer bearing a 400Å thick seed layer.

Summary

The present invention discloses methods applied to an electrochemical deposition apparatus with multiple electrodes and a system of electrical power controls. Such an apparatus is referred as "said apparatus" throughout the text and figures in this invention. An example of such an apparatus is described in earlier US. Patent No. 6391166 and PCT Patent Application No. PCT/CN2007/071008.

The disclosed methods apply to plating wafers bearing a seed layer with a thickness from 50Å to 900Å in a copper sulfate based electrolyte with conductivity ranging from 0.02 to 0.8 S/cm.

The disclosed methods produced electrochemically plated copper film with a within film non-uniformity as small as 0.33% (a variation of 42 Å) on 350Å seed layer, several times less than what was disclosed in previous patents.

Brief Description of Drawings

FIG. 1 illustrates a schematic view of said apparatus in the earlier invention on which present methods are practiced;

FIG. 2 illustrates a schematic view of part of a single-electrode plating apparatus.

FIGS. 3a - 3d show deposition profiles from a single-electrode plating apparatus.

FIG. 4 illustrates a schematic view of part of a plating apparatus with two electrodes disclosed in earlier invention;

FIGS. 5a and 5b illustrate waveform diagrams applied to a two-electrode plating apparatus.

FIGS. 6a and 6b show deposition profiles from a two-electrode apparatus;

FIG. 7 illustrates a schematic view of part of a plating apparatus with three electrodes disclosed in earlier invention;

FIGS. 8a and 8b illustrate waveform diagrams applied to a three-electrode plating apparatus.

FIGS. 9a and 9b show deposition profiles from a three-electrode apparatus;

FIG. 10 illustrates a schematic view of part of a plating apparatus with four electrodes disclosed in earlier invention;

FIGS. 11a and 11b illustrate waveform diagrams applied to a four-electrode plating apparatus.

FIGS. 12a and 12b show deposition profiles from a four-electrode apparatus;

FIGS. 13 show deposition profiles from a ten-electrode apparatus;

FIGS. 14 show estimated deposition profiles.

Detailed Description of Embodiments

The present invention discloses methods applied to an electrochemical deposition apparatus with multiple electrodes and a system of electrical power controls. The disclosed methods apply to plating wafers bearing a seed layer with a thickness from 50Å to 900Å in a copper sulfate based electrolyte with conductivity ranging from 0.02 to

0.8 S/cm. The disclosed method is to be practiced on apparatus disclosed in US Patent No. 6391166.

The methods in present invention include the following steps:

introducing a copper sulfate based electrolyte with a flow rate in the range of 1 to 20 LPM into said apparatus;

transferring a semiconductor wafer to a semiconductor wafer holder with electrical conduction path to wafer;

applying a small bias voltage to wafer;

bringing wafer into electrolyte, and the front surface of the wafer being in full contact with the electrolyte;

applying electrical current to each electrode; the power supplying connected to electrodes switch from constant voltage mode to constant current mode at desired times;

applying current or potential at a relative small value on each of electrodes, preferably the combined current being from 2A to 10A, and the ratio of the current densities of between electrodes being from 0.5:1 to 300:1;

applying current or potential at a relative large value on each of electrodes, preferably the combined current being from 10A to 40A, and the ratio of the current densities between electrodes being from 0.5:1 to 300:1;

switching power supply to a small bias voltage mode and apply it on said semiconductor wafer;

bringing wafer out of the electrolyte.

stopping power supply and clean off the residue electrolyte on wafer surface.

The current distribution on each electrode and the ratio of current densities between electrodes in steps 6 and 7 above vary in narrower ranges depending on the number of electrodes used and the

conductivity of the electrolyte. In the following embodiments, these ranges are specified for an apparatus with a particular number of electrodes and a particular electrolyte conductivity.

In one embodiment a method applied to said apparatus comprising two electrodes with electrolyte conductivity of 0.02-0.2S/cm is disclosed.

In one embodiment, a method applied to said apparatus comprising two electrodes with electrolyte conductivity of 0.2-0.8S/cm is disclosed.

In one embodiment, a method applied to said apparatus comprising three electrodes with electrolyte conductivity of 0.02-0.2S/cm is disclosed.

In one embodiment, a method applied to said apparatus comprising three electrodes with electrolyte conductivity of 0.2-0.8S/cm is disclosed.

In one embodiment, a method applied to said apparatus comprising four electrodes with electrolyte conductivity of 0.02-0.2S/cm is disclosed.

In one embodiment, a method applied to said apparatus comprising four electrodes with electrolyte conductivity of 0.2-0.8S/cm is disclosed.

In one embodiment, a method applied to said apparatus comprising ten electrodes with electrolyte conductivity of 0.02-0.2S/cm is disclosed.

In one embodiment, a method applied to said apparatus comprising ten electrodes with electrolyte conductivity of 0.2-0.8S/cm is disclosed.

A conventional plating apparatus with single electrode 201 is illustrated in Fig 2. Figs 3a – 3d are deposition profiles on the surface of a 300mm semiconductor wafer with said single electrode electroplating apparatus. More specifically, Figs 3a and 3b illustrate the deposition profiles of 3000Å thick film on said semiconductor with seed layer thicknesses varying from 350Å to 900Å in low and high conductive electrolytes, respectively, while Fig 3c and 3d illustrate the deposition profiles with thicknesses varying from 3000Å to 6000Å on said

semiconductor with 350Å thick seed layer in low and high conductive electrolytes, respectively.

WFNU values calculated from the thickness profiles in Figs 3a-3b are listed in Table 1. WFNU values increase as the thickness of seed layers decrease, indicating significant difficulty to deposit a uniform Cu film on the surface of semiconductor wafer when the seed layer is thin. And when the thickness of seed layer is less than 700Å, a WFNU value of less than 2.5% can no longer be achieved by conventional electroplating with a single electrode. The situation becomes worse when the conductivity of electrolyte increases.

Table 1

Seed layer thickness	Low conductive electrolyte - WFNU	High conductive electrolyte- WFNU
350Å	3.72%	13.91%
550Å	2.95%	11.45%
700Å	2.58%	10.19%
900Å	2.21%	8.94%

On the same 350Å-thick seed layer, the WFNU improves when the plating thickness increases, as illustrated in Fig 3c-3d. The corresponding values are listed in Table 2, and this effect is due to fact that the reduced the ohmic resistance of thicker film lessens the terminal effect during the deposition process. WFNU values are greater than 2.5% for plating thickness less than 5000Å, and they are far greater than 2.5% in the embodiment of high conductivity electrolytes. Although increasing plating thickness further can improve WFNU, the high cost associated to remove these excessive plated Cu in the following CMP step in the IC process flow prohibits depositing a very thick film.

Table 2

Deposition thickness	Low conductive electrolyte - WFNU	High conductive electrolyte- WFNU
3000Å	3.72%	13.91%
4000Å	2.98%	11.25%
5000Å	2.48%	9.93%
6000Å	2.12%	8.83%

In this invention, thinner seed (350Å) and plating thickness (3000Å) are used for all analysis forward. This combination gives the high sensitivity of the methods disclosed.

Embodiment 1

In one embodiment of the invention, a method for uniform deposition of Cu film on the surface of semiconductor wafer practiced in the apparatus illustrated in FIG 4 is disclosed is an embodiment of the invention illustrated in FIG 1; wherein the apparatus consists of the first electrode 401a and the second electrode 401b which can be positioned at the same or different vertical height, the area of the first electrode is 50%-90% of the total area of all electrodes, and the ratio of the total area of all electrodes over the area of the semiconductor wafer is greater than 0.85. The method consists of the following set of steps:

Step 1: open flow controllers 423a and 423b to control the flow rate in the working area for each electrode respectively; the flow rate in the working area of 401a is in the range 5 to 20 LPM and that of 401b is in the range 1 to 15 LPM. In one embodiment of the invention, the flow controllers 423a and 423b are turned on at the same time. In another embodiment of the invention, the flow controllers 423a and 423b are turned on at different times.

Step 2: transfer the semiconductor wafer bearing a seed layer to the wafer holder 421 in the apparatus; the wafer holder has an electrical

conducting passage that is in contact with the seed layer of the semiconductor wafer.

Step 3: apply small bias voltage in the range of 0.01 to 10 V to said semiconductor wafer.

Step 4: bring the semiconductor wafer, held by the wafer holder, into contact with the electrolyte, until the wafer front surface is fully immersed in the electrolyte.

Step 5: apply currents to electrodes 401a and 401b and maintain a positive potential on electrode 401a and a positive or negative potential on electrode 401b (The sign of the potential on each electrode is defined relatively to wafer through the text); the working current of electrode 401a is from 5 to 20A, and that of electrode 401b is from 0.01 to 10A. The ratio of the current densities on electrode 401a to that on electrode 201b is from 1:1 to 300:1. This step lasts for 5 to 30 seconds to fill the vias and trenches on the surface of semiconductor wafer 422. In one embodiment of the invention, the power supplies connected to the electrodes 401a and 401b switch from constant voltage mode to constant current mode at the same time. In another embodiment of the invention, the power supplies connected to the electrodes 401a and 401b switch from constant voltage mode to constant current mode at different times.

Step 6: power supplies connected to electrodes 401a and 401b control a positive potential on electrode 401a and a positive or negative potential on electrode 401b; the working current on electrode 401a is from 15 to 40A, and that on electrode 401b is from 0.01 to 20A. The ratio of the current densities on electrode 401a to that on electrode 401b is from 1:1 to 300:1. This step increases the efficiency of the electrochemical deposition by applying relative large electrical currents on the electrodes 401a and 401b. This step terminates when a desired deposition thickness is achieved.

Step 7: apply a small bias voltage on said semiconductor wafer. In

one embodiment of the invention, the electrodes 401a and 401b are switched from constant current mode to constant voltage mode at the same time. In another embodiment of the invention, the electrodes 401a and 401b are switched from constant current mode to constant voltage mode at different times.

Step 8: bring the semiconductor wafer out of the electrolyte and spin off the residue electrolyte left on the wafer surface.

In above step 5 and step 6, the sign of potential on electrode 401b is determined to be positive or negative based on the electrochemical deposition conditions. For example, if the conductivity of electrolyte is low and conductive layer on semiconductor wafer is thick, positive potential will be applied to both electrodes 401a and 401b as illustrated in Fig 5a; if the conductivity of electrolyte is high and conductive layer on wafer is thin, a positive potential will be applied to electrode 401a and a negative potential to electrode 401b as illustrated in Fig 5b.

The detailed sets of current density ratio and the signs of potential on individual electrode used in step 5 for plating uniform copper film on a 300mm semiconductor wafer bearing 200-2000Å thick seed layer in electrolyte with conductivity from 0.02 to 0.2S/cm and conductivity from 0.2 to 0.8S/cm are listed in Table 3:

Table 3

	Sign of Electrode 201a	Sign of Electrode 201b	Current density ratio (201a : 201b)
Conductivity 0.02-0.2S/cm	+	+	1:1-30:1
	+	-	15:1-30:1
Conductivity 0.2-0.8S/cm	+	-	2:1-15:1

Step 6 begins when the plated thickness of Cu film reaches 1500Å. The detailed sets current density ratio and the signs of potential on individual electrode used in step 6 for plating uniform copper film on a 300mm semiconductor wafer bearing 200-2000Å thick seed layer in

electrolyte with conductivity from 0.02 to 0.2S/cm and conductivity from 0.2 to 0.8S/cm are listed in Table 4.

Table 4

	Sign of Electrode 201a	Sign of Electrode 201b	Current density ratio (201a : 201b)
Conductivity 0.02-0.2S/cm	+	+	1:1-30:1
	+	-	15:1-30:1
Conductivity 0.2-0.8S/cm	+	-	10:1-20:1

FIGS 6a and 6b show the deposition profiles of 3000Å thick film deposited on 350Å seed layer in low and high conductive electrolyte respectively; wherein the profiles of method 1 are obtained with the process parameters detailed in Table 3 and 4, while those of method 2 are obtained with the process parameters out of the range defined in Table 3 and 4. The WFNU values are listed in the Table 5. As shown in Figs 6a-6b and Table 5, the disclosed method greatly improves WFNU of deposited 3000Å films in both low and high conductive electrolyte. WFNU values of said profiles on the surface of a 300mm semiconductor wafer are obtained excluding 2.3mm from the edge, which is more aggressive compared to the common industry practice of excluding 3.0 to 6.5 mm from the edge of the wafer.

Table 5

	Method 1 (Disclosed)- WFNU	Method 2 (Conventional)- WFNU
Low conductive electrolyte	2.35%	3.65%
High conductive electrolyte	7.44%	12.94%

Disclosed method (method 1) significantly improved WFNU, compared to conventional method (method 2) in both low and high conductivity electrolytes. In the embodiment of low conductivity electrolyte, a WFNU less than 2.5% is obtained.

Embodiment 2

In one embodiment of the invention, a method for uniform deposition of Cu film on the surface of semiconductor wafer practiced in the apparatus illustrated in FIG 7 is disclosed is an embodiment of the invention illustrated in FIG 1; wherein the apparatus consists of the first electrode 701a, the second electrode 701b and the third electrode 701c which can be positioned at the same or different vertical height, the area of the first electrode is 40%-60% of the total area of all electrodes, and the ratio of the total area of all electrodes over the area of the semiconductor wafer is greater than 0.85. The method consists of the following set of steps:

Step 1: open flow controllers 723a, 723b and 723c to control the flow rate in the working area for each electrode respectively; the flow rate in the working area of 701a is in the range 5 to 20 LPM, that of 701b is in the range 5 to 20 LPM, and that of 701c is 1 to 15 LPM. In one embodiment of the invention, the flow controllers 723a, 723b and 723c are turned on at the same time. In another embodiment of the invention, the flow controllers 723a, 723b and 723c are turned on at different times.

Step 2: transfer the semiconductor wafer bearing a seed layer to the wafer holder 721 in the apparatus; the wafer holder has an electrical conducting passage that is in contact with the seed layer of the semiconductor wafer.

Step 3: apply small bias voltage in the range of 0.01 to 10V to said semiconductor wafer;

Step 4: bring the semiconductor wafer, held by the wafer holder, into contact with the electrolyte, until the wafer front surface is fully immersed in the electrolyte;

Step 5: apply currents to electrodes 701a, 701b and 701c and maintain a positive potential on electrodes 701a, 701b and a positive or negative potential on electrode 701c; the working current of electrode 701a is from 2 to 20A, that of electrode 701b is from 0.01 to 20A, and that of electrode 701c is from 0.01 to 20A. The ratio of the current densities on electrode 701a to that on electrode 701b is from 1:1 to 50:1 and ratio of the current densities on electrode 701a to that on electrode 701c is from 1:1 to 300:1. This step lasts for 5 to 30 seconds to fill the vias and trenches on the surface of semiconductor wafer 722. In one embodiment of the invention, the power supplies connected to the electrodes 701a, 701b and 701c switch from constant voltage mode to constant current mode at the same time. In another embodiment of the invention, the power supplied connected to the electrodes 701a, 701b and 701c switch from constant voltage mode to constant current mode at different times.

Step 6: power supplies connected to electrodes 701a, 701b and 701c control a positive potential on electrodes 701a, 701b and a positive or negative potential on electrode 701c; the working current on electrode 701a is from 4 to 30A, that on electrode 701b is from 4 to 30A and that of electrode 701c is from 0.1 to 20A. The ratio of the current densities on electrode 701a to that on electrode 701b is from 1:1 to 50:1 and ratio of the current densities on electrode 701a to that on electrode 701c is from 1:1 to 300:1. This step increases the efficiency of the electrochemical deposition by applying relative large electrical currents on the electrodes 701a, 701b and 701c. This step terminates when desired deposition thickness is achieved.

Step 7: apply a small a bias voltage on said semiconductor wafer. In one embodiment of the invention, the electrodes 701a, 701b and

701c are switched from constant current mode to constant voltage mode at the same time. In another embodiment of the invention, the electrodes 701a, 701b and 701c are switched from constant current mode to constant voltage mode at different times.

Step 8: bring the semiconductor wafer out of the electrolyte and spin off the residue electrolyte left on the wafer surface.

In the above step 5 and step 6, the sign of potential on electrode 701c is determined to be positive or negative based on the electrochemical deposition conditions. For example, if the conductivity of electrolyte is low and conductive layer on semiconductor wafer is thick, positive potentials will be applied to all electrodes 701a, 701b and 701c as illustrated in Fig 8a; if the conductivity of electrolyte is high and conductive layer on wafer is thin, positive potentials will be applied to electrode 701a and 701b, and a negative potential to electrode 701c as illustrated in Fig 8b.

The detailed sets of current density ratio and the signs of potential on individual electrode used in step 5 for plating uniform copper film on a 300mm semiconductor wafer bearing 150-2000Å thick seed layer in electrolyte with conductivity from 0.02 to 0.2S/cm and conductivity from 0.2 to 0.8S/cm are listed in Table 6:

Table 6

	Sign of Electrode 301a	Sign of Electrode 301b	Sign of Electrode 301c	Current density ratio	
				(301a : 301b)	(301a : 301c)
Conductivity 0.02-0.2S/cm	+	+	+	1:1-2:1	1:1-300:1
	+	+	-	1:1-2:1	10:1-40:1
Conductivity 0.2-0.8S/cm	+	+	-	5:1-20:1	2:1-10:1

Step 6 begins when the plated thickness of Cu film reaches 1500Å. The detailed sets current density ratio and the signs of potential on individual electrode used in step 6 for plating uniform copper film on a 300mm semiconductor wafer bearing 150-2000Å thick seed layer in electrolyte with conductivity from 0.02 to 0.2S/cm and conductivity from 0.2 to 0.8S/cm are listed in Table 7:

Table 7

	Sign of Electrode 301a	Sign of Electrode 301b	Sign of Electrode 301c	Current density ratio	
				(301a : 301b)	(301a : 301c)
Conductivity 0.02-0.2S/cm	+	+	+	1:1-2:1	1:1-300:1
	+	+	-	1:1-2:1	50:1-300:1
Conductivity 0.2-0.8S/cm	+	+	-	1:1-2:1	20:1-80:1

FIGS 9a and 9b show the deposition profiles of 3000Å thick film deposited on 350Å seed layer in low and high conductive electrolyte respectively; wherein the profiles of method 1 are obtained with the process parameters detailed in Table 6 and 7, while those of method 2 are obtained with the process parameters out of the range defined in Table 6 and 7. The WFNU values are listed in the Table 8. As shown in Figs 9a-9b and Table 8, the disclosed method greatly improves WFNU of deposited 3000Å films in both low and high conductive electrolyte. WFNU values of said profiles on the surface of a 300mm semiconductor wafer are obtained excluding 2.3mm from the edge, which is more aggressive compared to the common industry practice of excluding 3.0 to 6.5mm from the edge of the wafer.

Table 8

	Method 1(Disclosed)- WFNU	Method 2(Conventional)- WFNU
Low conductive electrolyte	0.54%	2.81%
High conductive electrolyte	1.52%	8.55%

Disclosed method (method 1) significantly improved WFNU, compared to conventional method (method 2) in both low and high conductivity electrolytes. In the embodiment of low conductivity electrolyte, a WFNU less than 2.5% is obtained.

Embodiment 3

In one embodiment of the invention, a method for uniform deposition of Cu film on the surface of semiconductor wafer practiced in the apparatus illustrated in FIG 10 is disclosed is an embodiment of the invention illustrated in FIG 1; wherein the apparatus consists of the first electrode 1001a, the second electrode 1001b, the third electrode 1001c and the fourth electrode 1001d which can be positioned at the same or different vertical height, the area of the first electrode is 30%-50% of the total area of all electrodes, and the ratio of the total area of all electrodes over the area of the semiconductor wafer is greater than 0.85. The method consists of the following set of steps:

Step 1: open flow controllers 1023a, 1023b, 1023c and 1023d to control the flow rate in the working area for each electrode respectively; the flow rate in the working area of 1001a, 1001b and 1001c are in the range 5 to 20 LPM and that of 1001d is in the range 1 to 15 LPM. In one embodiment of the invention, the flow controllers 1023a, 1023b, 1023b and 1023c are turned on at the same time. In another embodiment of the invention, the flow controllers 1023a, 1023b, 1023b and 1023c are turned on at different times.

Step 2: transfer the semiconductor wafer bearing a seed layer to the wafer holder 1021 in the apparatus; the wafer holder has an electrical conducting passage that is in contact with the seed layer of the semiconductor wafer.

Step 3: apply small bias voltage in the range of 0.01 to 10V to said semiconductor wafer;

Step 4: bring the semiconductor wafer, held by the wafer holder, into contact with the electrolyte, until the wafer front surface is fully immersed in the electrolyte.

Step 5: apply currents to electrodes 1001a, 1001b and 1001c and maintain a positive potential on electrodes 1001a, 1001b, 1001c and a positive or negative potential on electrode 1001d; the working current of electrode 1001a is from 1 to 15 A, that of electrode 1001b from 0.5 to 10A, and that of electrode 1001c and 1001d from 0.01 to 10A. The ratio of the current densities on electrode 1001a to that on electrode 1001b is from 0.5:1 to 10:1, that of electrode 1001a to 1010c from 0.5:1 to 50:1 and that of 1001a to 1001d from 1:1 to 300:1. This step lasts for 5 to 30 seconds to fill the vias and trenches on the surface of semiconductor wafer 1022. In one embodiment of the invention, the power supplies connected to the electrodes 1001a, 1001b, 1001b and 1001c switch from constant voltage mode to constant current mode at the same time. In another embodiment of the invention, the power supplies connected to the electrodes 1001a, 1001b, 1001b and 1001c switch from constant voltage mode to constant current mode at different times.

Step 6: power supplies connected to electrodes 1001a, 1001b and 1001c control a positive potential on electrodes 1001a, 1001b, 1001c and a positive or negative potential on electrode 1001d; the working current on electrode 1001a is from 2 to 30A, that on electrode 1001b and 1001c from 1 to 30A, and that of electrode 1001d from 0.01 to 20A. The ratio of the current densities on electrode 1001a to that on electrode 1001b is from 0.5:1 to 10:1, that of electrode 1001a to 1010c

from 0.5:1 to 50:1 and that of 1001a to 1001d from 1:1 to 300:1. This step increases the efficiency of the electrochemical deposition by applying relative large electrical currents on the electrodes 1001a, 1001b, 1001c and 1001d. This step terminates when desired deposition thickness is achieved.

Step 7: Apply a small bias voltage on said semiconductor wafer. In one embodiment of the invention, the electrodes 1001a, 1001b, 1001b and 1001c are switched from constant current mode to constant voltage mode at the same time. In another embodiment of the invention, the electrodes 1001a, 1001b, 1001b and 1001c are switched from constant current mode to constant voltage mode at different times.

Step 8: bring the semiconductor wafer out of the electrolyte and spin off the residue electrolyte left on the wafer surface.

In above step 5 and step 6, the sign of potential on electrode 1001d is determined to be positive or negative based on the electrochemical deposition conditions. For example, if the conductivity of electrolyte is low and conductive layer on semiconductor wafer is thick, positive potentials will be applied to all electrodes 1001a, 1001b, 1001c and 1001d as illustrated in Fig 11a; if the conductivity of electrolyte is high and conductive layer on wafer is thin, positive potentials will be applied to electrode 1001a, 1001b and 1001c, and a negative potential to electrode 1001d as illustrated in Fig 11b.

The detailed sets of current density ratio and the signs of potential on individual electrode used in step 5 for plating uniform copper film on a 300mm semiconductor wafer bearing 50-2000Å thick seed layer in electrolyte with conductivity from 0.02 to 0.2S/cm and conductivity from 0.2 to 0.8S/cm are listed in Table 9:

Table 9

	Sign of Electrode 401a	Sign of Electrode 401b	Sign of Electrode 401c	Sign of Electrode 401d	Current density ratio		
					(401a : 401b)	(401a : 401c)	(401a : 401d)
Conductivity 0.02-0.2S/cm	+	+	+	+	0.5:1-2:1	0.5:1-10: 1	1:1-300:1
	+	+	+	-	0.5:1-2:1	0.5:1-3:1	10:1-100: 1
Conductivity 0.2-0.8S/cm	+	+	+	-	1:1-2:1	4:1-30:1	2:1-20:1

Step 6 begins when the plated thickness of Cu film reaches 1500Å. The detailed sets current density ratio and the signs of potential on individual electrode used in step 6 for plating uniform copper film on a 300mm semiconductor wafer bearing 50-2000Å thick seed layer in electrolyte with conductivity from 0.02 to 0.2S/cm and conductivity from 0.2 to 0.8S/cm are listed in Table 10:

Table 10

	Sign of Electrode 401a	Sign of Electrode 401b	Sign of Electrode 401c	Sign of Electrode 401d	Current density ratio		
					(401a : 401b)	(401a : 401c)	(401a : 401d)
Conductivity 0.02-0.2S/cm	+	+	+	+	1:1-2:1	1:1-10:1	1:1-300:1
	+	+	+	-	0.5:1-2:1	0.5:1-10: 1	10:1-300: 1
Conductivity 0.2-0.8S/cm	+	+	+	-	1:1-2:1	1:1-2:1	1:1-250:1

FIGS 12a and 12b show the deposition profiles of 3000Å thick film deposited on 350Å seed layer in low and high conductive electrolyte respectively; wherein the profiles of method 1 are obtained with the process parameters in Table 9 and 10, while those of method 2 are obtained with the process parameters out of the range defined in Table 9 and 10. The WFNU values are listed in the following Table 11. As shown in Figs 12a-12b and Table 11, the disclosed method greatly improves WFNU of deposited 3000Å films in both low and high

conductive electrolyte. WFNU values of said profiles on the surface of a 300mm semiconductor wafer are obtained excluding 2.3mm from the edge, which is more aggressive compared to the common industry practice of excluding 3.0 to 6.5mm from the edge of the wafer.

Table 11

	Method 1 (Disclosed)- WFNU	Method 2 (Conventional)- WFNU
Low conductive electrolyte	0.33%	2.69%
High conductive electrolyte	0.66%	5.47%

Disclosed method (method 1) significantly improved WFNU, compared to conventional method (method 2) in both low and high conductivity electrolytes. In the embodiment of low conductivity electrolyte, a WFNU less than 2.5% is obtained.

Embodiment 4

The above methods of present invention are practiced on simple electrode configurations of the apparatus disclosed in U.S patent No. 6391166. Other applications of the method of the present invention practiced in those electrode configurations with more than four electrodes can be devised in similar way; wherein the area of the first electrode being 5%-30% of total electrodes area, and the ratio of the total area of all electrodes over the area of the semiconductor wafer is greater than 0.85.

The detailed sets of current density ratio and the signs of potential on individual electrode used for plating first 100Å to 1500Å copper film on a 300mm semiconductor wafer bearing 50-2000Å thick seed layer in

electrolyte with conductivity from 0.02 to 0.2S/cm and conductivity from 0.2 to 0.8S/cm are listed in Table 12. In this embodiment, the plating apparatus consists of N electrodes, where N is between 5 and 15.

Table 12

	Sign of 1 st Electrode	Sign of 2 nd ... (n-2) th Electrodes	Sign of (n-1) th Electrode	Sign of n th Electrode	Current density ratio		
					E1 : E2... En-2	(E1 : En-1)	(E1 : En)
Conductivity 0.02-0.2S/cm	+	+	+	+	0.8:1-2:1	0.5:1-10: 1	1:1-300:1
	+	+	+	-	0.5:1-2:1	0.5:1-3:1	10:1-100: 1
Conductivity 0.2-0.8S/cm	+	+	+	-	1:1-2:1	4:1-40:1	2:1-100:1

The detailed sets of current density ratio and the signs of potential on individual electrode used for plating the remaining portion of copper film on a 300mm semiconductor wafer bearing 50-2000Å thick seed layer in electrolyte with conductivity from 0.02 to 0.2S/cm and conductivity from 0.2 to 0.8S/cm are listed in Table 13.

Table 13

	Sign of 1 st Electrode	Sign of 2 nd ... (n-2) th Electrodes	Sign of (n-1) th Electrode	Sign of n th Electrode	Current density ratio		
					E1 : E2... En-2	(E1 : En-1)	(E1 : En)
Conductivity 0.02-0.2S/cm	+	+	+	+	1:1-2:1	1:1-10:1	1:1-300:1
	+	+	+	-	0.5:1-2:1	0.5:1-10: 1	10:1-300: 1
Conductivity 0.2-0.8S/cm	+	+	+	-	1:1-2:1	1:1-2:1	1:1-300:1

FIGS 13 shows the deposition profiles of 3000Å thick Cu film deposited on a 350Å seed layer with said apparatus in electrolyte 1 with low conductivity and electrolyte 2 with high conductivity, respectively; wherein the apparatus of said embodiment comprises ten electrodes

with independent control. WFNU values obtained using the method of present invention are well below 2.5%: 0.26% in electrolyte 1 and 0.59% in electrolyte 2, respectively.

WFNU improves as the number of electrodes, N, increases with methods disclosed in the present invention. The methods, when applied to an apparatus with more than one electrode, produces WFNU less than 2.5% on 300mm wafer with a seed layer as thin as 350Å. When N is increased to four, the WFNU improves to 0.33% on the same wafer and same seed layer.

The method disclosed in the present invention is compared to a method disclosed previously in US Patent 6755954. All conditions are held to be exactly the same: (1) multiple electrodes configuration (2) electrolyte conductivity = 0.5 S/cm, (3) seed layer thickness = 400Å, (4) total plating thickness = 6000Å, and (5) excluding 2.7mm of Cu film from wafer edge. To make direct comparison, thickness uniformity range values are used, instead of WFNU values. Fig 14 shows the deposition profile estimated with the method disclosed in the present invention, and the thickness uniformity range values are compared in Table 14:

Table 14

Thickness uniformity range in US 675594	Thickness uniformity range here
240Å	138.4Å

The method of present invention produces a deposited film with WFNU = 0.72% and thickness uniformity range = 138.4Å, nearly 2X improvement compared to the disclosed method in US Patent 6755954.

What is claimed is:

1. A method for electrochemical deposition of uniform Cu film in an apparatus consisting of two electrodes, wherein an area of a first electrode is between 50% to 90% of the total area of all electrodes, the method comprises:

flowing a copper sulfate based electrolyte into a plating apparatus, wherein the flow rate is from 1 to 20 LPM;

transferring a semiconductor wafer to a wafer holder that is electrically in contact with conductive layer on the semiconductor wafer;

turning on power supplies to apply a bias voltage up to 10V to the semiconductor wafer;

bringing the semiconductor wafer into contact with the electrolyte;

maintaining a positive potential relative to the semiconductor wafer on the first electrode;

providing, in a first plating step, a combined current from 2A to 10A to all electrodes, a ratio of the current density on the first electrode over that on the second electrode is between 1:1-30:1 when the potential on the second electrode is positive relative to the semiconductor wafer; and the ratio of the current density on the first electrode over that on the second electrode is between 2:1-30:1 when the potential on the second electrode is negative relative to the semiconductor wafer;

providing, in a second plating step, a combined current from 10A to 40A to all electrodes; a ratio of the current density on the first electrode over that on the second electrode is between 1:1-30:1 when the potential on the second electrode is positive relative to the semiconductor wafer; and the ratio of the current density on the first electrode over that on the second electrode is between 10:1-30:1 when the potential on the second electrode is negative relative to the semiconductor wafer;

providing, by switch power supplies, a bias voltage up to 1V on the

semiconductor wafer;

bringing the semiconductor wafer out of the electrolyte.

2. The method of claim 1, where in the ratio of the total area of all electrodes over the area of the semiconductor wafer is greater than 0.85.

3. The method of claim 1, wherein the ratio of the current densities on the first electrode over that on the second electrode is between 15:1-30:1 in the electrolyte with conductivity from 0.02 to 0.2S/cm when the potential on the second electrode is negative relative to said semiconductor wafer in the first plating step.

4. The method of claim 1, wherein the ratio of the current densities on the first electrode over that on the second electrode is between 2:1-15:1 in the electrolyte with conductivity from 0.2 to 0.8S/cm when the potential on the second electrode is negative relative to said semiconductor wafer in the first plating step.

5. The method of claim 1, wherein the ratio of the current densities on the first electrode over that on the second electrode is between 15:1-30:1 in the electrolyte with conductivity from 0.02 to 0.2S/cm when the potential on the second electrode is negative relative to said semiconductor wafer in the second plating step.

6. The method of claim 1, wherein the ratio of the current densities on the first electrode over that on the second electrode is between 10:1-20:1 in the electrolyte with conductivity from 0.2 to 0.8S/cm when the potential on the second electrode is negative relative to said semiconductor wafer in the second plating step.

7. The method of claim 1, wherein the thickness of the conductive layer on the semiconductor wafer is from 50 to 900Å.

8. The method of claim 1, wherein the WFNU of the Cu film deposited on the semiconductor wafer surface is adjustable from 0.2% to 2.5%.

9. The method of claim 1, wherein the electrodes are positioned at the same vertical height.

10. The method of claim 1, wherein the electrodes are positioned at different vertical heights.

11. A method for electrochemical deposition of uniform Cu film in an apparatus consisting of three electrodes, wherein an area of the first electrode is between 40% to 60% of the total area of all electrodes, the method comprises:

flowing a copper sulfate based electrolyte into a plating apparatus, wherein the flow rate is from 1 to 20 LPM.

transferring a semiconductor wafer to a wafer holder that is electrically in contact with conductive layer on the wafer;

turning on power supplies to apply a bias voltage up to 10V to the semiconductor wafer;

bringing the semiconductor wafer into contact with the electrolyte;

maintaining a positive potential relative to the semiconductor wafer on the first electrode;

providing, in a first plating step, a combined current from 2A to 10A to all electrodes; a ratio of the current density on the first electrode over that on the second electrode is between 1:1-2:1, and that on the first electrode over that on the third electrode is between 1:1-300:1 when the

potential on the third electrode is positive relative to said semiconductor wafer; and the ratio of the current density on the first electrode over that on the second electrode is between 1:1-20:1, and that on the first electrode over that on the third electrode is between 2:1-40:1 when the potential on the third electrode is negative relative to said semiconductor wafer;

providing, in a second plating step, a combined current from 10A to 40A to all electrodes; a ratio of the current density on the first electrode over that on the second electrode is between 1:1-2:1, and that on the first electrode over that on the third electrode is between 1:1-300:1 when the potential on the third electrode is positive relative to said semiconductor wafer; and the ratio of the current density on the first electrode over that on the second electrode is between 1:1-2:1, and that on the first electrode over that on the third electrode is between 20:1-300:1 when the potential on the third electrode is negative relative to said semiconductor wafer;

providing, by switch power supplies, a bias voltage up to 1V on said semiconductor wafer;

bringing the semiconductor wafer out of the electrolyte.

12. The method of claim 11, where in the ratio of the total area of all electrodes over the area of the semiconductor wafer is greater than 0.85.

13. The method of claim 11, wherein the ratio of the current densities on the first electrode over that on the second electrode is between 1:1-2:1, and that on the first electrode over that on the third electrode is between 10:1-40:1 in the electrolyte with conductivity from 0.02 to 0.2S/cm when the potential on the third electrode is negative relative to the semiconductor wafer in the first plating step.

14. The method of claim 11, wherein the ratio of the current densities on the first electrode over that on the second electrode is between 5:1-20:1, and that on the first electrode over that on the third electrode is between 2:1-10:1 in the electrolyte with conductivity from 0.2 to 0.8S/cm when the potential on the third electrode is negative relative to the semiconductor wafer in the first plating step.

15. The method of claim 11, wherein the ratio of the current densities on the first electrode over that on the second electrode is between 1:1-2:1, and that on the first electrode over that on the third electrode is between 50:1-300:1 in the electrolyte with conductivity from 0.02 to 0.2S/cm when the potential on the third electrode is negative relative to the semiconductor wafer in the second plating step.

16. The method of claim 11, wherein the ratio of the current densities on the first electrode over that on the second electrode is between 1:1-2:1, and that on the first electrode over that on the third electrode is between 20:1-80:1 in the electrolyte with conductivity from 0.2 to 0.8S/cm when the potential on the third electrode is negative relative to the semiconductor wafer in the second plating step.

17. The method of claim 11, wherein the thickness of the conductive layer is from 50 to 900Å.

18. The method of claim 11, wherein the WFNU of the Cu film deposited on the semiconductor wafer surface is adjustable from 0.2% to 2.5%.

19. The method of claim 11, wherein the electrodes are positioned at the same vertical height

20. The method of claim 11, wherein the electrodes are positioned at different vertical heights.

21. A method for electrochemical deposition of uniform Cu film in an apparatus consisting of four or more electrodes, wherein an area of the first electrode is between 5% to 50% of the total area of all electrodes, the method comprises:

flowing a copper sulfate based electrolyte into a plating apparatus, wherein the flow rate is from 1 to 20 LPM.

transferring a semiconductor wafer to a wafer holder that is electrically in contact with conductive layer on the wafer;

turning on power supplies to apply a bias voltage up to 10V to the semiconductor wafer;

bringing the semiconductor wafer into contact with the electrolyte;

maintaining a positive potential relative to the semiconductor wafer on the first electrode;

providing, in a first plating step, a combined current from 2A to 10A to all electrodes; a ratio of the current density on the first electrode over that on the second last electrode is between 0.5:1-10:1, that on the first electrode over that on the last electrode is between 1:1-300:1 and that on the first electrode over that on the rest electrodes is between 0.5:1-2:1 when the potential on the last electrode is positive relative to the semiconductor wafer; and the ratio of the current density on the first electrode over that on the rest electrode is between 0.5:1-2:1, that on the first electrode over that on the second last electrode is between 0.5:1-30:1, and that on the first electrode over that on the last electrode is between 2:1-300:1 when the potential on the last electrode is negative relative to the semiconductor wafer;

providing, in a second plating step, a combined current from 10A to 40A to all electrodes; a ratio of the current density on the first electrode over that on the second last electrode is between 0.5:1-10:1, that on the

first electrode over that on the last electrode is between 1:1-300:1, and that on the first electrode over that on the rest electrodes is between 0.8:1-2:1 when the potential on the last electrode is positive relative to the semiconductor wafer; and the ratio of the current density on the first electrode over that on the rest electrode is between 0.5:1-2:1, that on the first electrode over that on the second last electrode is between 0.5:1-10:1, and that on the first electrode over that on the last electrode is between 1:1-300:1 when the potential on the last electrode is negative relative to the semiconductor wafer;

providing, by switch power supplies, a bias voltage up to 1V on said semiconductor wafer;

bringing the semiconductor wafer out of the electrolyte.

22. The method of claim 21, where in the ratio of the total area of all electrodes over the area of the semiconductor wafer is greater than 0.85.

23. The method of claim 21, wherein the ratio of the current densities on the first electrode over that on the second last electrode is between 0.5:1-3:1, that on the first electrode over that on the last electrode is between 10:1-100:1, and that on the first electrode over that on the rest electrodes is between 0.5:1-2:1 in the electrolyte with conductivity from 0.02 to 0.2S/cm when the potential on the last electrode is negative relative to said semiconductor wafer in the first plating step.

24. The method of claim 21, wherein the ratio of the current densities on the first electrode over that on the second last electrode is between 4:1-40:1, that on the first electrode over that on the last electrode is between 2:1-100:1, and that on the first electrode over that on the rest electrodes is between 1:1-2:1 in the electrolyte with

conductivity from 0.2 to 0.8S/cm when the potential on the third electrode is negative relative to said semiconductor wafer in the first plating step.

25. The method of claim 21, wherein the ratio of the current densities on the first electrode over that on the second last electrode is between 0.5:1-10:1, that on the first electrode over that on the last electrode is between 10:1-300:1, and that on the first electrode over that on the rest electrodes is between 0.5:1-2:1 in the electrolyte with conductivity from 0.02 to 0.2S/cm when the potential on the third electrode is negative relative to said semiconductor wafer in the second plating step.

26. The method of claim 21, wherein the ratio of the current densities on the first electrode over that on the second last electrode is between 1:1-2:1, that on the first electrode over that on the last electrode is between 1:1-300:1, and that on the first electrode over that on the rest electrodes is between 1:1-2:1 in the electrolyte with conductivity from 0.2 to 0.8S/cm when the potential on the third electrode is negative relative to said semiconductor wafer in the second plating step.

27. The method of claim 21, wherein the thickness of the conductive layer is from 50 to 900Å.

28. The method of claim 21, wherein the WFNU of said Cu film deposited on the semiconductor wafer surface is adjustable from 0.2% to 2.5%.

29. The method of claim 21, the electrodes are positioned at the same vertical height

30. The method of claim 21, the electrodes are positioned at different vertical heights.