ABSTRACT OF THE DISCLOSURE

A processor includes a constant register 36 for storing a constant, a format decoder 21 for decoding a format code located in the P0.0 field of an instruction stored in the instruction register 10, and a constant register control unit 32 which, when the format decoder 21 has decoded that the instruction includes a constant to be stored in the constant register 36, shifts the presently stored value in the constant register 36 and stores the constant into the constant register 36.

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