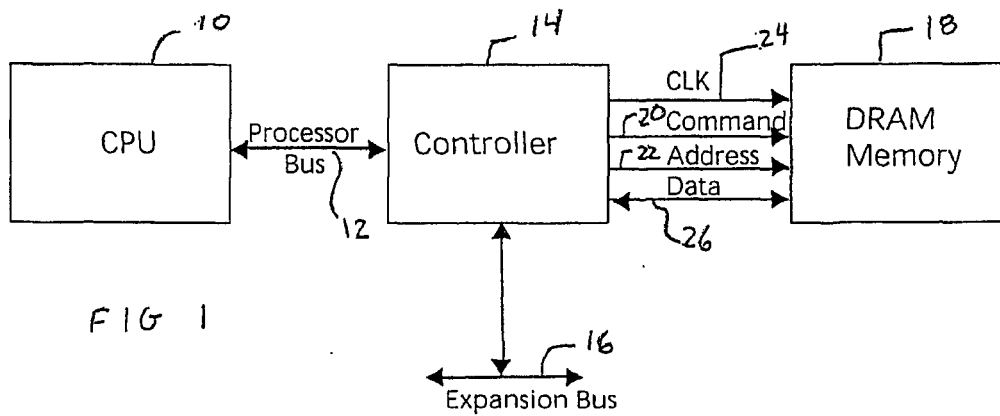




512M(x4) Addressing

Add Pin	ROW	COL
A13		
A12	ROW12	
A11	ROW11	
A10	ROW10	COL10
A9	ROW9	COL9
A8	ROW8	COL8
A7	ROW7	COL7
A6	ROW6	COL6
A5	ROW5	COL5
A4	ROW4	COL4
A3	ROW3	COL3
A2	ROW2	COL2
A1	ROW1	COL1
A0	ROW0	COL0

FIG 4A

512M(x8) Addressing

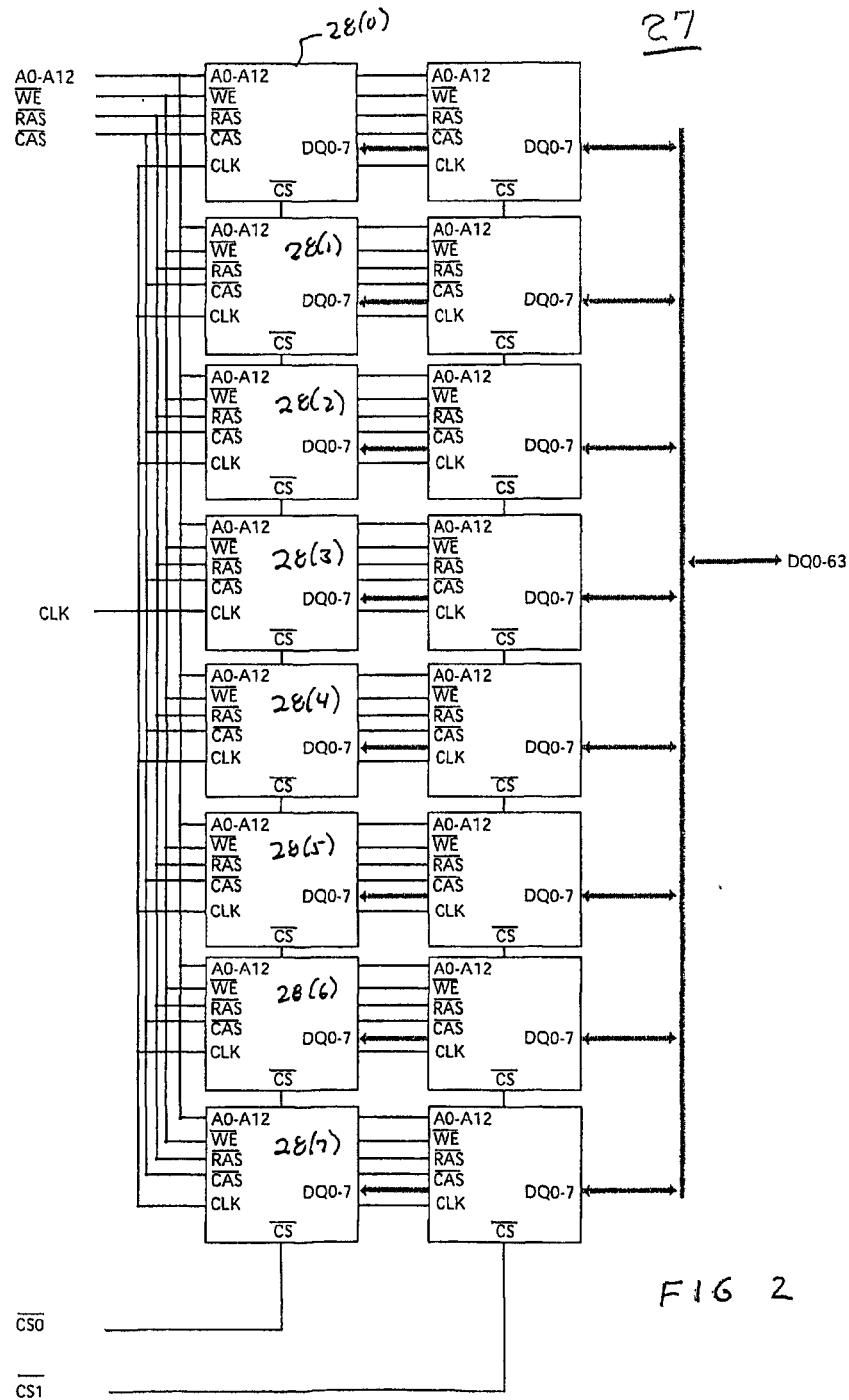
Add Pin	ROW	COL
A13		
A12	ROW12	
A11	ROW11	
A10	ROW10	
A9	ROW9	COL9
A8	ROW8	COL8
A7	ROW7	COL7
A6	ROW6	COL6
A5	ROW5	COL5
A4	ROW4	COL4
A3	ROW3	COL3
A2	ROW2	COL2
A1	ROW1	COL1
A0	ROW0	COL0

FIG 4B

512M(x16) Addressing

Add Pin	ROW	COL
A13		
A12		
A11	ROW11	
A10	ROW10	
A9	ROW9	COL9
A8	ROW8	COL8
A7	ROW7	COL7
A6	ROW6	COL6
A5	ROW5	COL5
A4	ROW4	COL4
A3	ROW3	COL3
A2	ROW2	COL2
A1	ROW1	COL1
A0	ROW0	COL0

FIG 4C



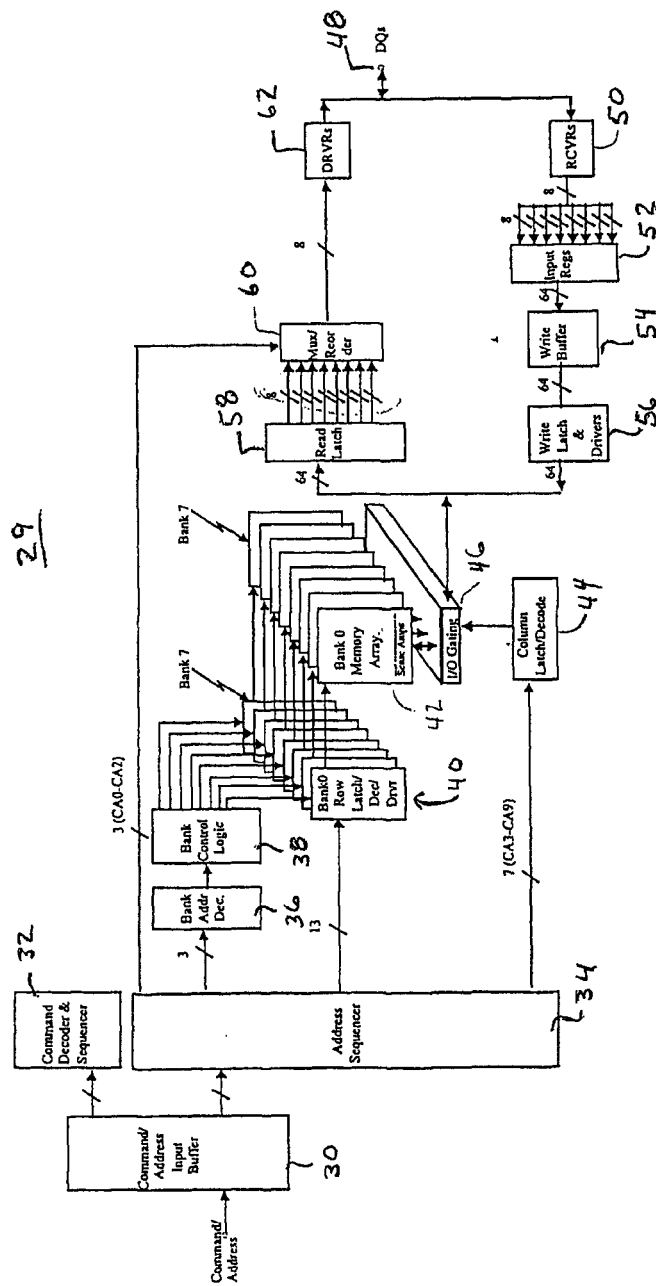


FIG 3

