

ABSTRACT

The present disclosure relates to a semiconductor memory device including a semiconductor substrate including a memory cell region and contact regions, a first stacked structure on the semiconductor substrate, a second stacked structure disposed between the semiconductor substrate and the first stacked structure, a plurality of cell plugs extending in a vertical direction crossing a top surface of the semiconductor substrate and arranged in the first stacked structure and the second stacked structure in the memory cell region, and a plurality of supports extending in the vertical direction and arranged in the first stacked structure in the contact region, wherein the second stacked structure is arranged in a different level from the plurality of supports.

FIG. 2B