Patent Claims

1. Method for the testing of optoelectronic chips (1) which are arranged on a wafer and have electrical interfaces in the form of contact pads (1.1) and optical interfaces which are arranged to be fixed relative thereto in the form of optical deflection elements (1.2) with a specific coupling angle (α), in which

- the wafer is received by a positioning table (3) which is adjustable relative to a contacting module (2) in X direction, Y direction and Z direction of a Cartesian coordinate system and which is rotatable around the Z axis, wherein the contacting module (2) has electrical interfaces in the form of needles (2.1) which are associated with the contact pads (1.1) and optical interfaces (2.2) which are associated with the optical deflection elements (1.2), and
- in a first adjustment step, the wafer is fed to the contacting module (2) in such a way that the needles (2.1) are disposed vertically above the centers of the contact pads (1.1) of a first one of the chips (1) in a first adjustment position, wherein the contacting module (2) has an adjustment distance (a) in Z direction from the first one of the chips (1) that is greater than a free length (l) of the needles (2.1),
- in further adjustment steps, the relative alignment of the optical deflection elements (1.2) with respect to the optical interfaces (2.2) provided on the contacting module (2) is carried out,
- the positioning table (3) is then fed to the contacting module (2) in Z direction by a feed displacement (Δz) in an optical working distance (b) in which the needles (2.1) contact the contact pads (1.1) with a predefined pressing force, and
- electrical signals and optical signals are subsequently routed via the interfaces which are associated with one another, wherein

- the relative alignment of the optical deflection elements (1.2) with respect to the optical interfaces (2.2) provided on the contacting module (2) is carried out in that,
- in a scanning field smaller than the size of the contact pads (1.1), the positioning table (3) is initially deflected into a second adjustment position in X direction and Y direction relative to the first adjustment position, while an optical signal is routed via at least one of the optical interfaces of the contacting module (2.2) and one of the optical deflection elements (1.2), wherein the second adjustment position is occupied when the optical signal is coupled in with a maximum intensity, and
- the first one of the chips (1) is subsequently deflected in X-Y direction by an adjustment displacement into a third adjustment position, wherein the adjustment displacement was calculated from the feed displacement (Δz) and the coupling angle (α) of the relevant optical deflection element (1.2) before the positioning table (3) is fed to the contacting module (2) in Z direction by the feed displacement (Δz) in the optical working distance (b), characterized in that
- a difference in position resulting from the first adjustment position and the second adjustment position of the first one of the chips (1) is stored as an offset and taken into account for the adjustment of further chips (1) after the latter have been positioned in a first adjustment position with respect to the contacting module (2).

2. Method for testing optoelectronic chips (1) arranged on a wafer, according to claim 1, characterized in that the optical working distance (b) in which the needles (2.1) contact the contact pads (1.1) with a predefined pressing force is monitored, and the third adjustment position is corrected when there are changes in the pressing force.

3. Method for testing optoelectronic chips (1) arranged on a wafer, according to one of claims 1 or 2, characterized in that the change in the optical working distance (b) is determined long-term over the useful life of the contacting module (2) and, for implementing the method, the needles (2.1) of the contacting module (2) are replaced by new needles (2.1) when the optical working distance (b) falls below a predetermined minimum distance.

4. Method for testing optoelectronic chips (1) arranged on a wafer, according to one of claims 1, characterized in that, when the optical signals routed via the interfaces which are respectively associated with one another are coupled into one of the interfaces, they over-radiate the latter.

5. Method for testing optoelectronic chips (1) arranged on a wafer, according to one of claims 1, characterized in that the optical signals routed via the interfaces which are respectively associated with one another have a tophead distribution of their radiation intensity when coupled into one of the interfaces.