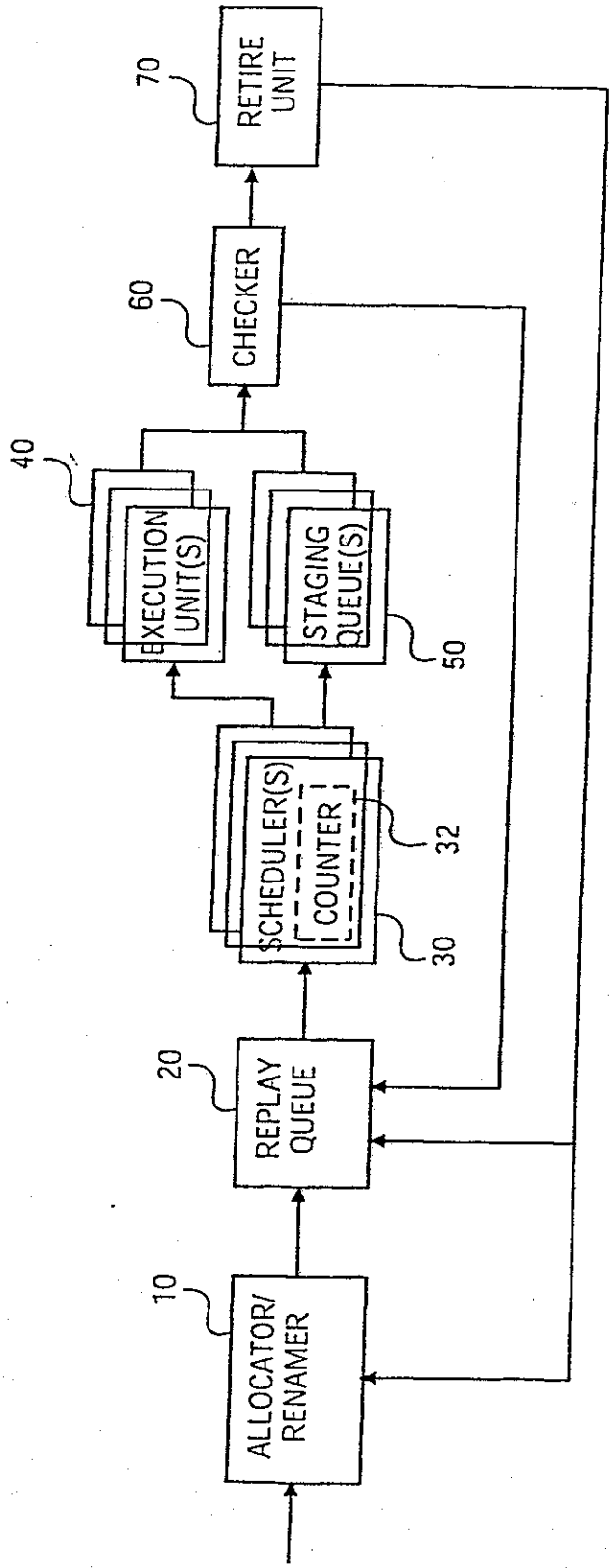

RETIRE UNIT
70
CHECKER
60
EXECUTION UNIT(S)
STAGING QUEUE(S)
40
50
SCHEDULER(S)
COUNTER
32
30
REPLAY QUEUE
20
ALLOCATOR/ RENAMER
10

FIG. 1

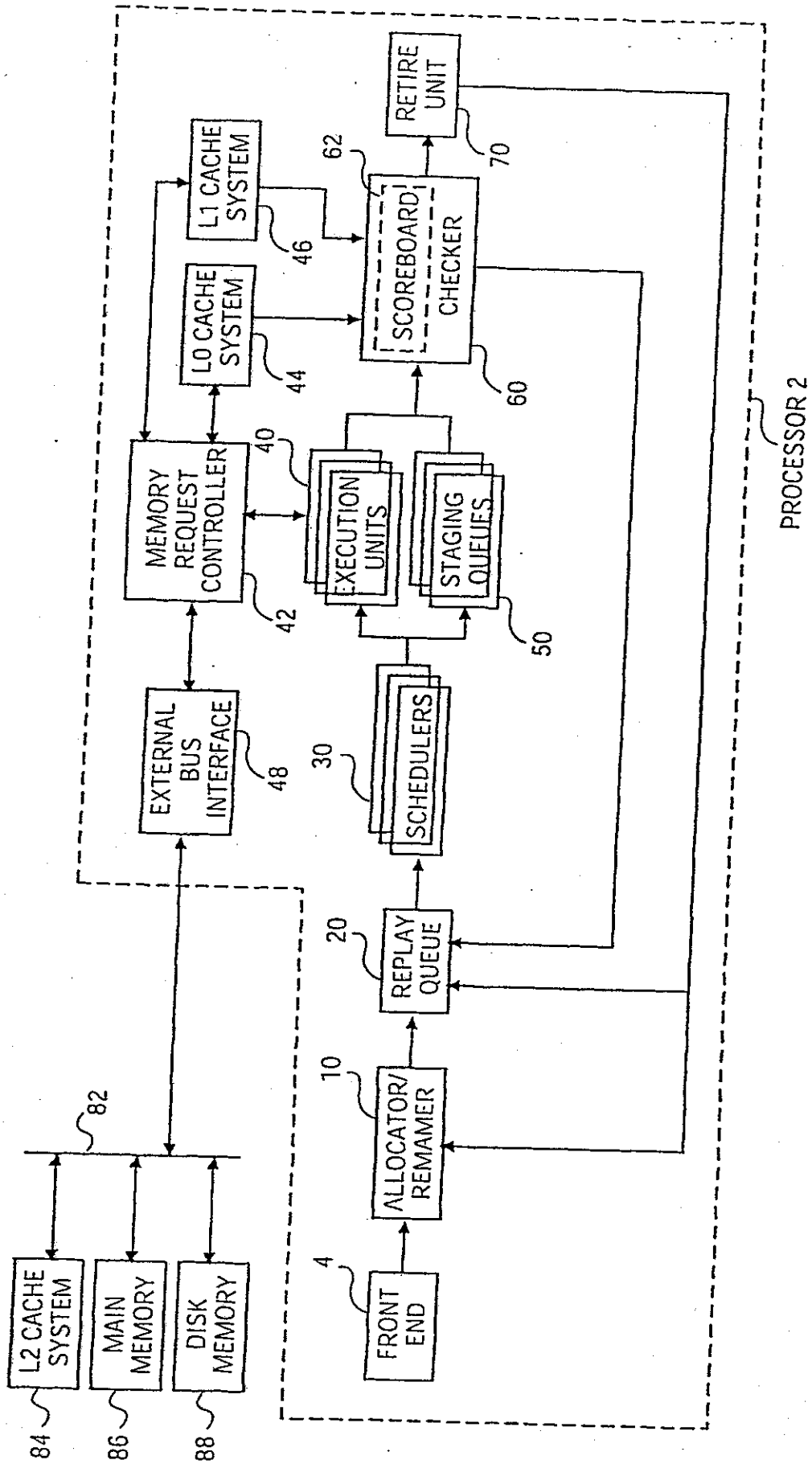

L2 CACHE SYSTEM
MAIN MEMORY
DISK MEMORY
84
86
88
82
EXTERNAL BUS INTERFACE
48
MEMORY REQUEST CONTROLLER
42
40
L1 CACHE SYSTEM
46
L0 CACHE SYSTEM
44
EXECUTION UNITS
STAGING QUEUES
50
SCOREBOARD/ CHECKER
60
62
RETIRE UNIT
70
PROCESSOR 2
SCHEDULERS
30
REPLAY QUEUE
20
ALLOCATOR/ REMAMER
10
FRONT END
4

FIG. 2

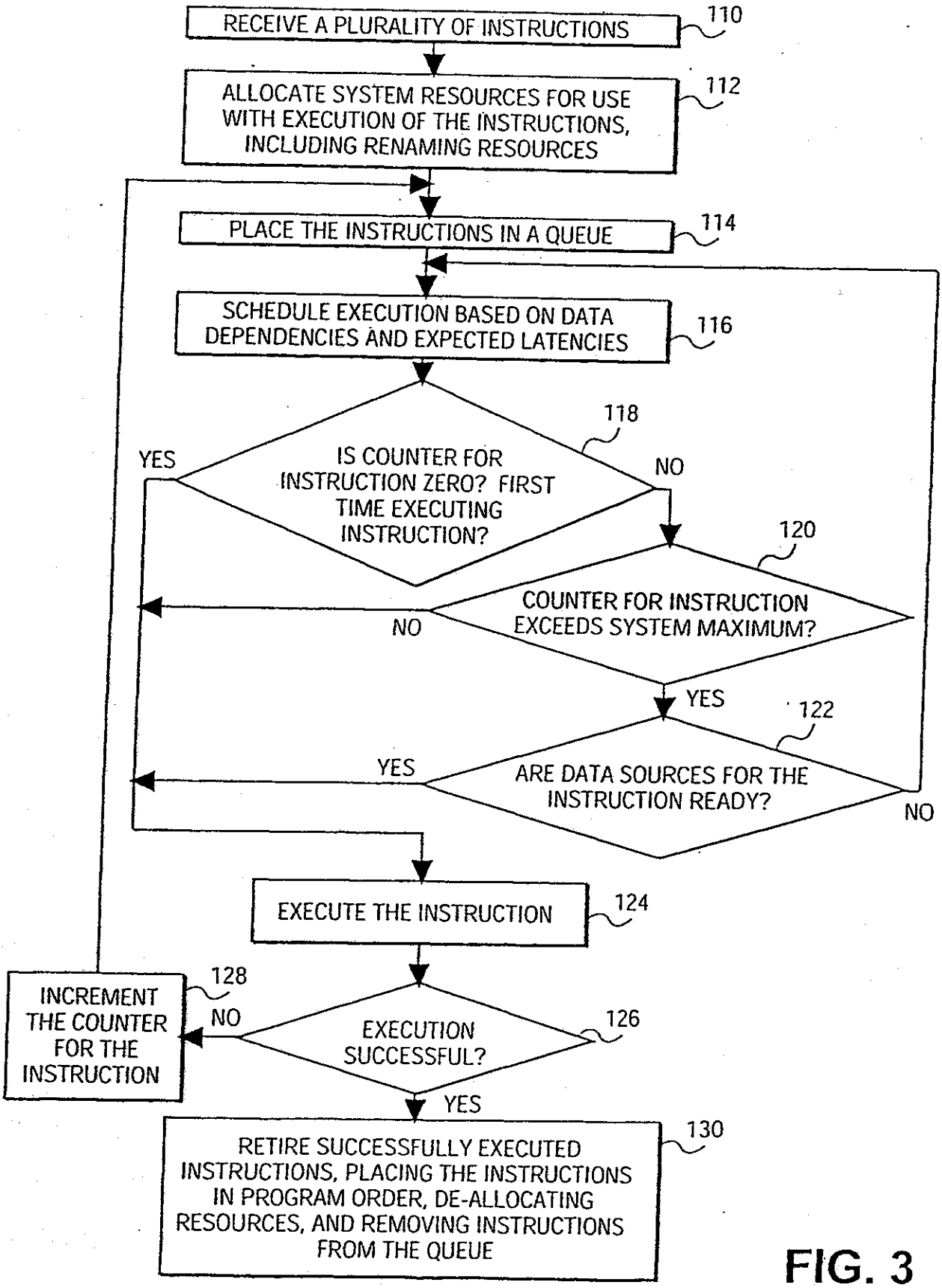

RECEIVE A PLURALITY OF INSTRUCTIONS
110
ALLOCATE SYSTEM RESOURCES FOR USE WITH EXECUTION OF THE INSTRUCTIONS, INCLUDING RENAMING RESOURCES
112
PLACE THE INSTRUCTIONS IN A QUEUE
114
SCHEDULE EXECUTION BASED ON DATA DEPENDENCIES AND EXPECTED LATENCIES
116
IS COUNTER FOR INSTRUCTION ZERO? FIRST TIME EXECUTING INSTRUCTION?
118
YES
NO
COUNTER FOR INSTRUCTION EXCEEDS SYSTEM MAXIMUM?
120
NO
YES
ARE DATA SOURCES FOR THE INSTRUCTION READY?
122
YES
NO
EXECUTE THE INSTRUCTION
124
EXECUTION SUCCESSFUL?
126
NO
YES
INCREMENT THE COUNTER FOR THE INSTRUCTION
128
RETIRE SUCCESSFULLY EXECUTED INSTRUCTIONS, PLACING THE INSTRUCTIONS IN PROGRAM ORDER, DE-ALLOCATING RESOURCES, AND REMOVING INSTRUCTIONS FROM THE QUEUE
130

FIG. 3