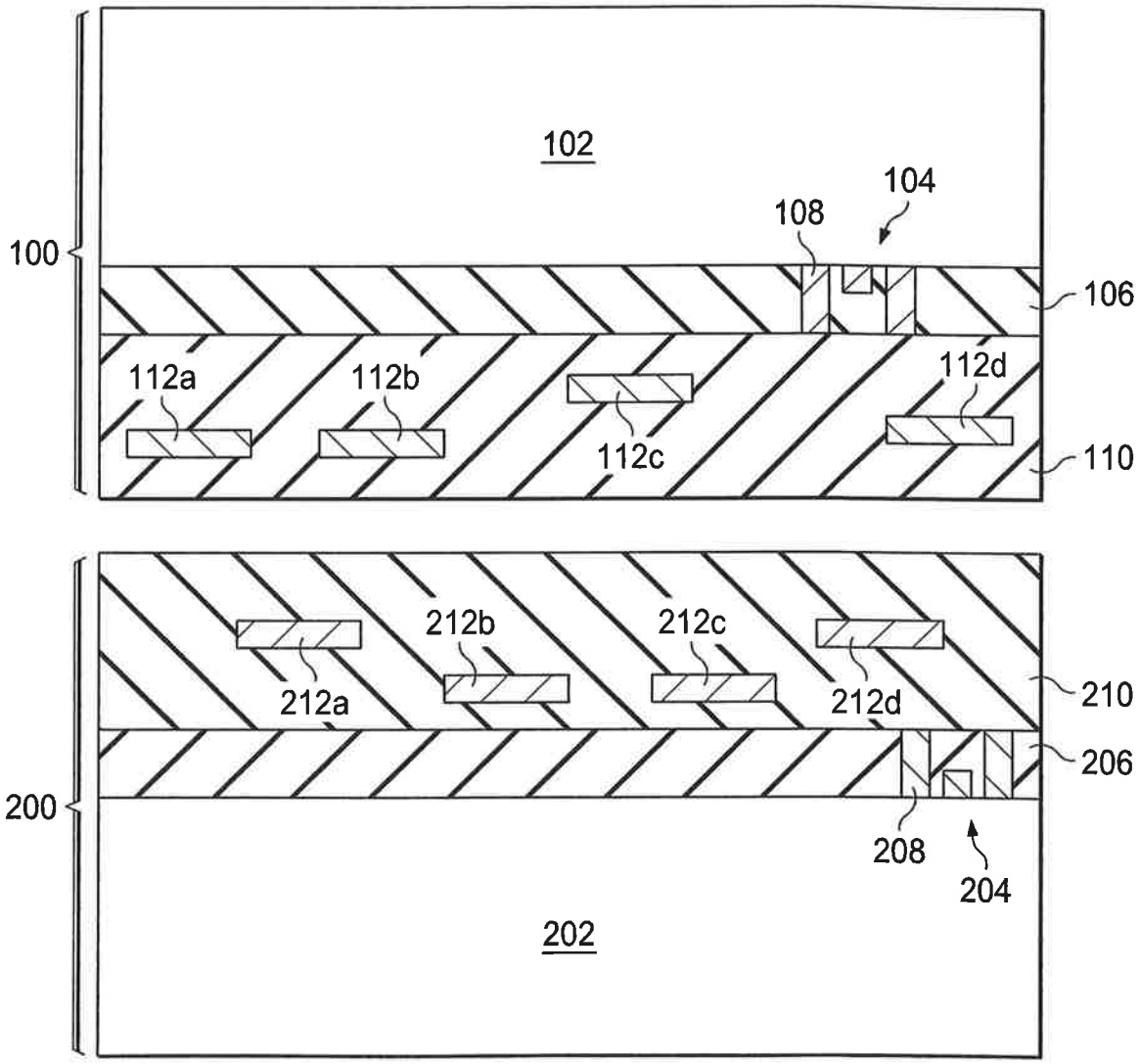

102
104
108
100
106
112a
112b
112c
112d
110
212b
212c
212a
212d
210
206
200
208
204
202

FIG. 1

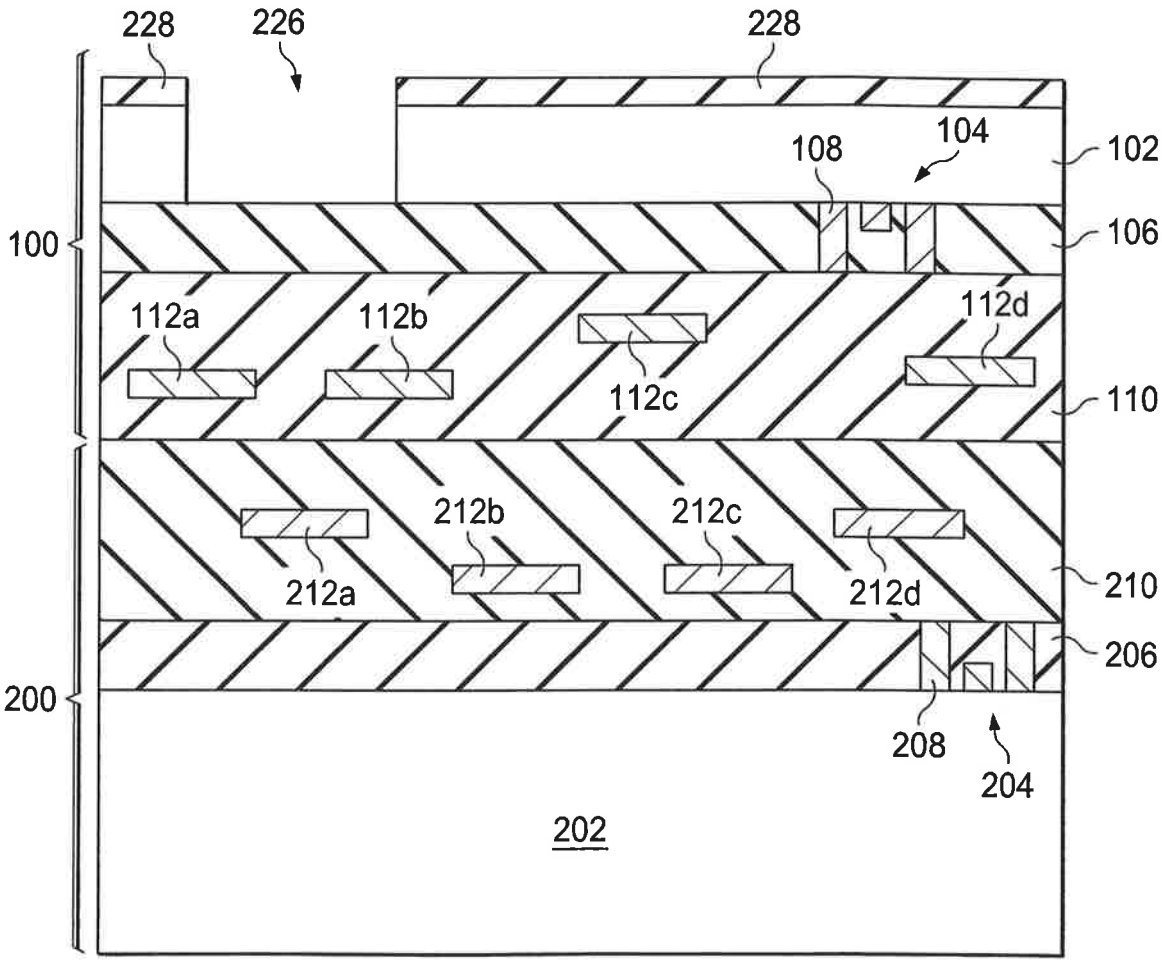

228
226
228
108
104
102
100
106
112a
112b
112c
112d
110
212b
212c
212a
212d
210
206
200
208
204
202

FIG. 2

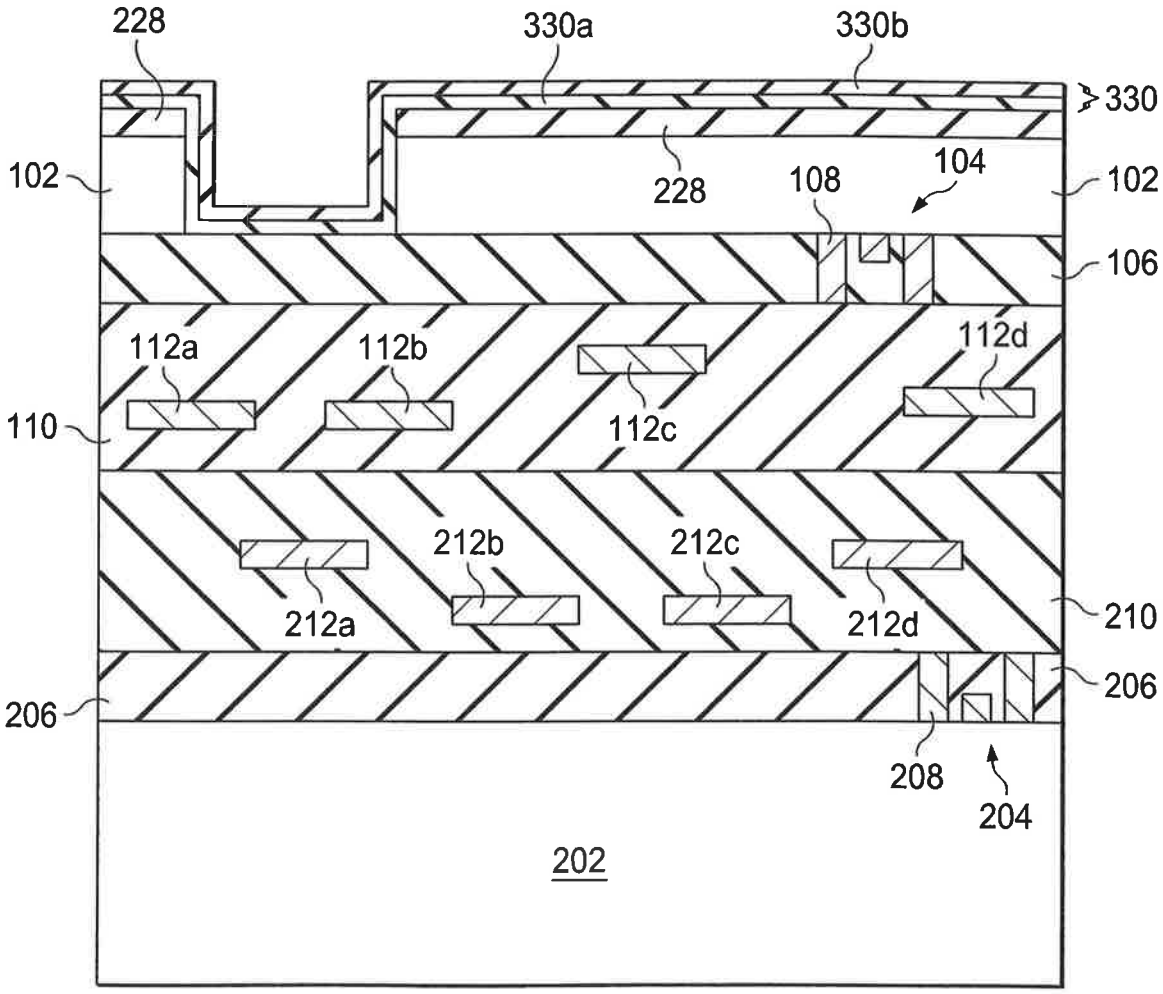

228
330a
330b
330
102
228
108
104
102
106
112a
112b
112c
112d
110
212b
212c
212a
212d
210
206
206
208
204
202

FIG. 3

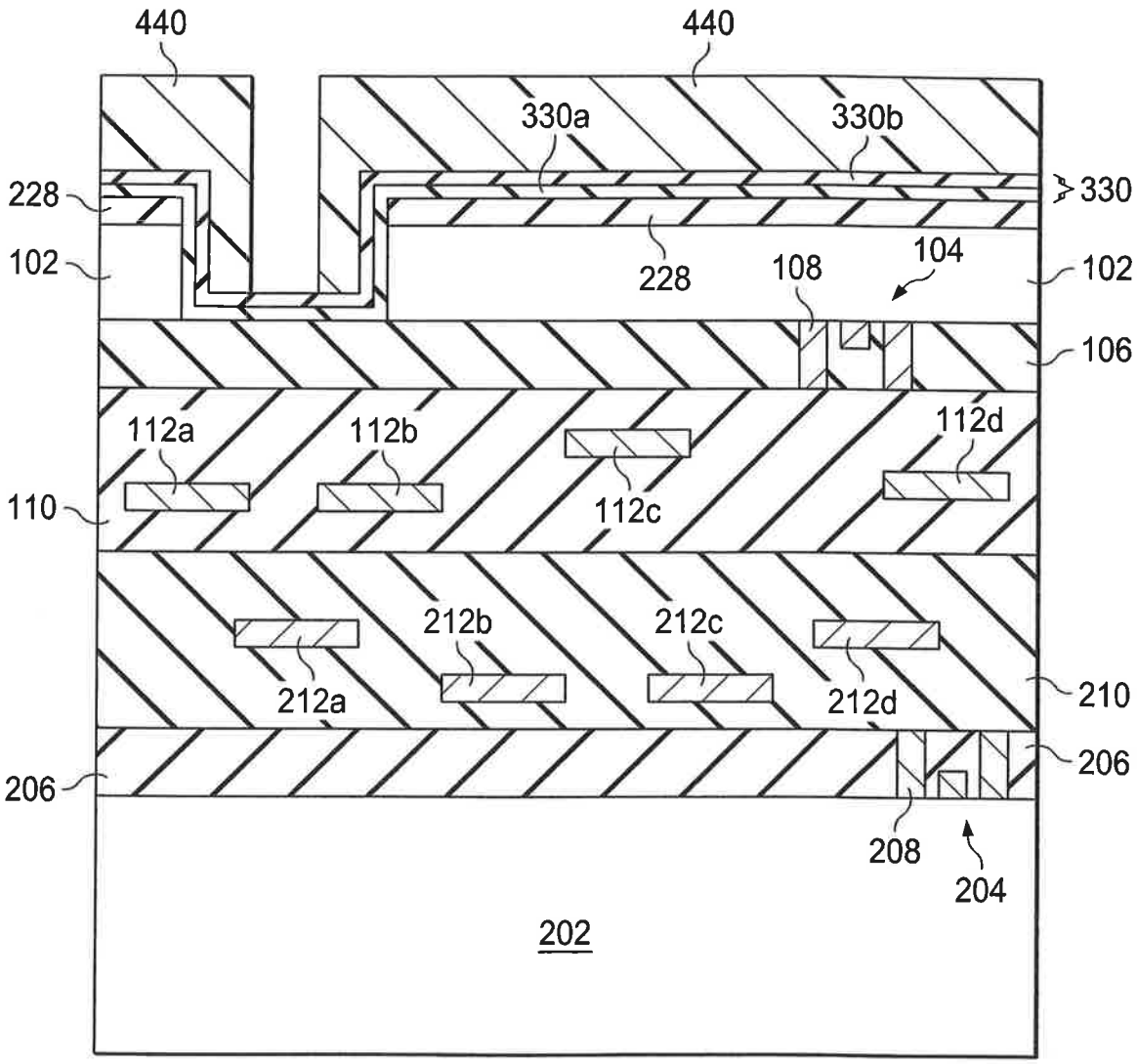

440
440
330a
330b
228
330
102
228
108
104
102
106
112a
112b
112c
112d
110
212b
212c
212a
212d
210
206
206
208
204
202

FIG. 4

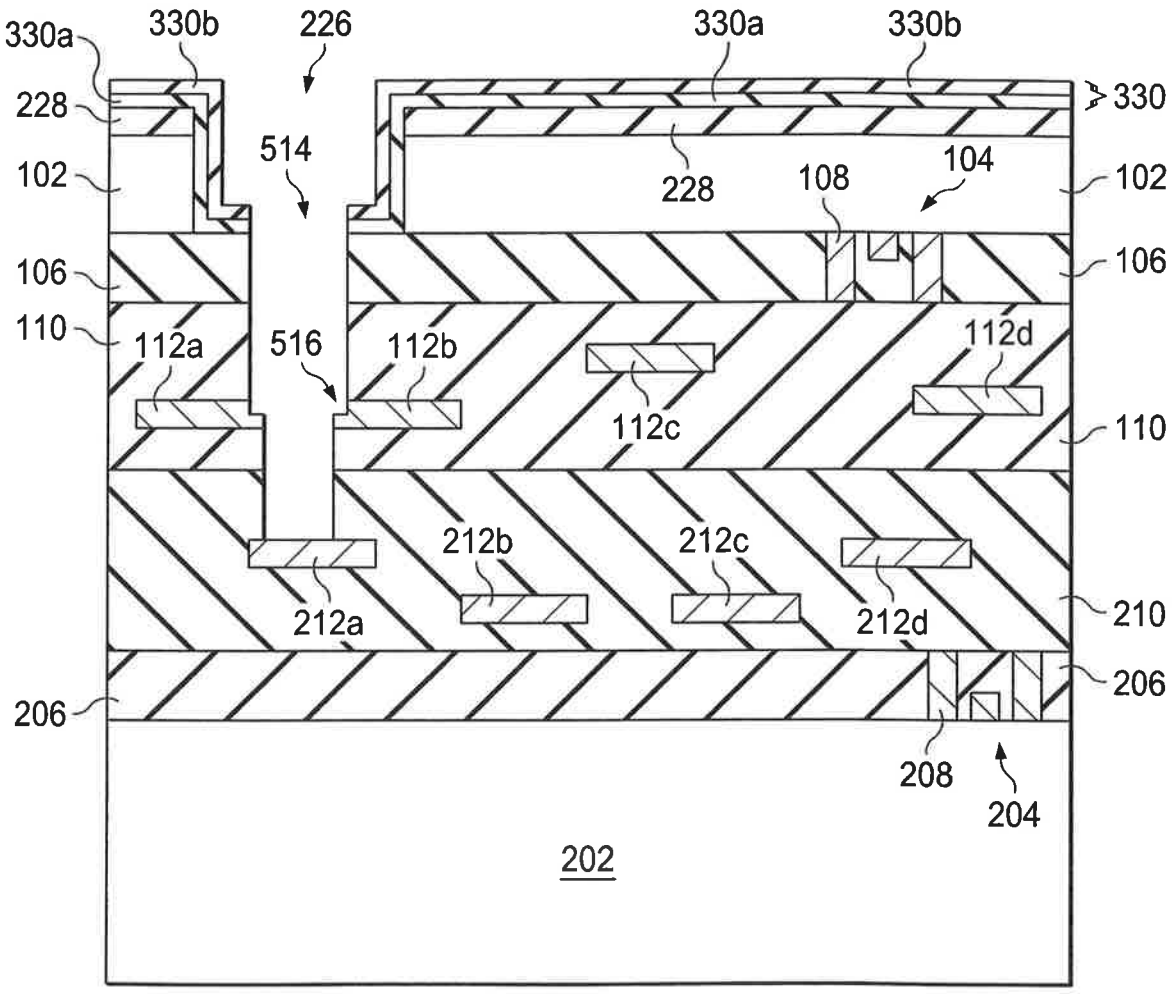

330a
330b
226
330a
330b
330
228
514
228
108
104
102
102
106
106
110
112a
516
112b
112d
112c
110
212b
212c
212a
212d
210
206
206
208
204
202

FIG. 5

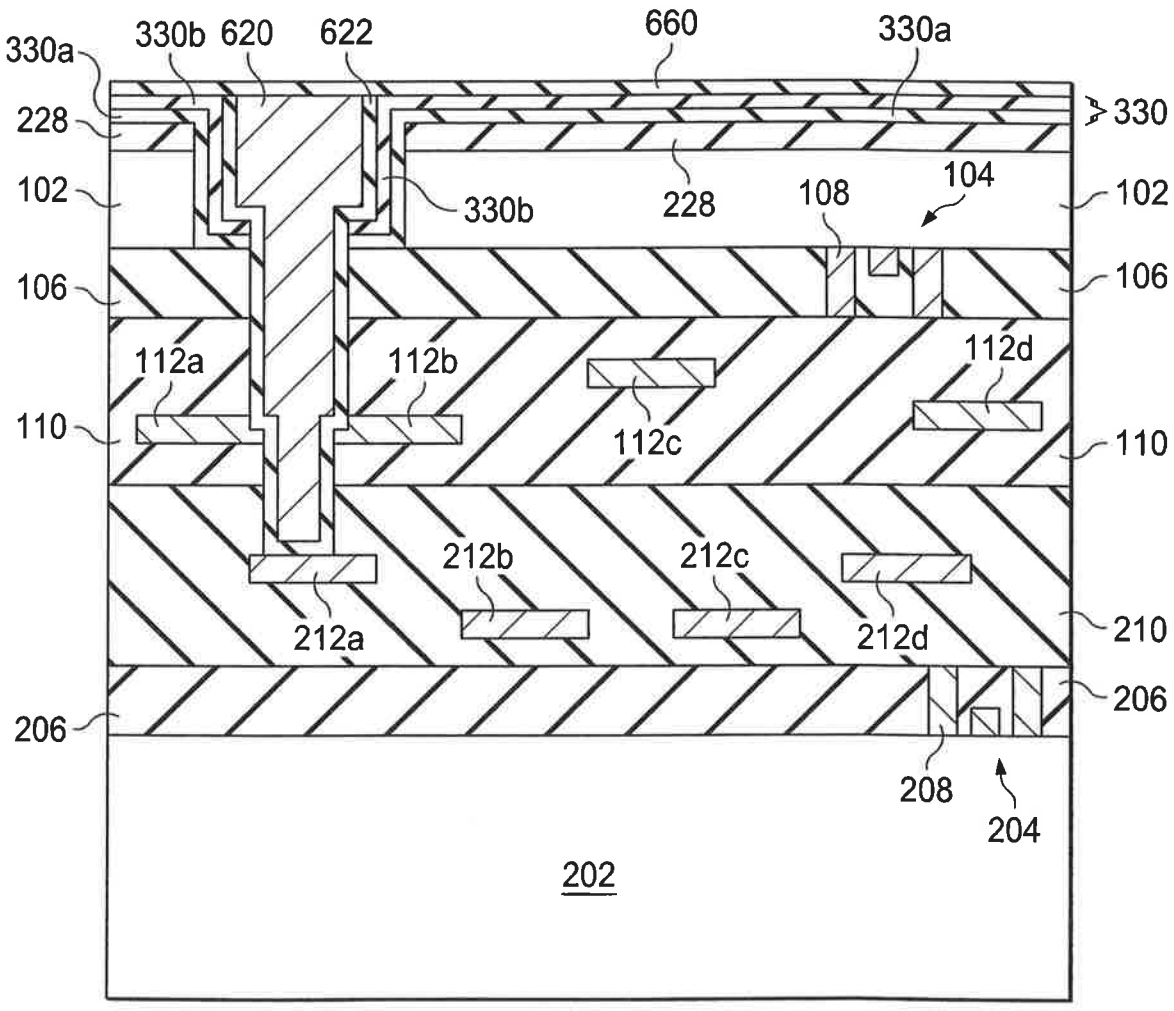

330a
330b
620
622
660
330a
228
330
102
330b
228
108
104
102
106
106
112a
112b
112d
110
112c
110
212b
212c
212a
212d
210
206
206
208
204
202

FIG. 6

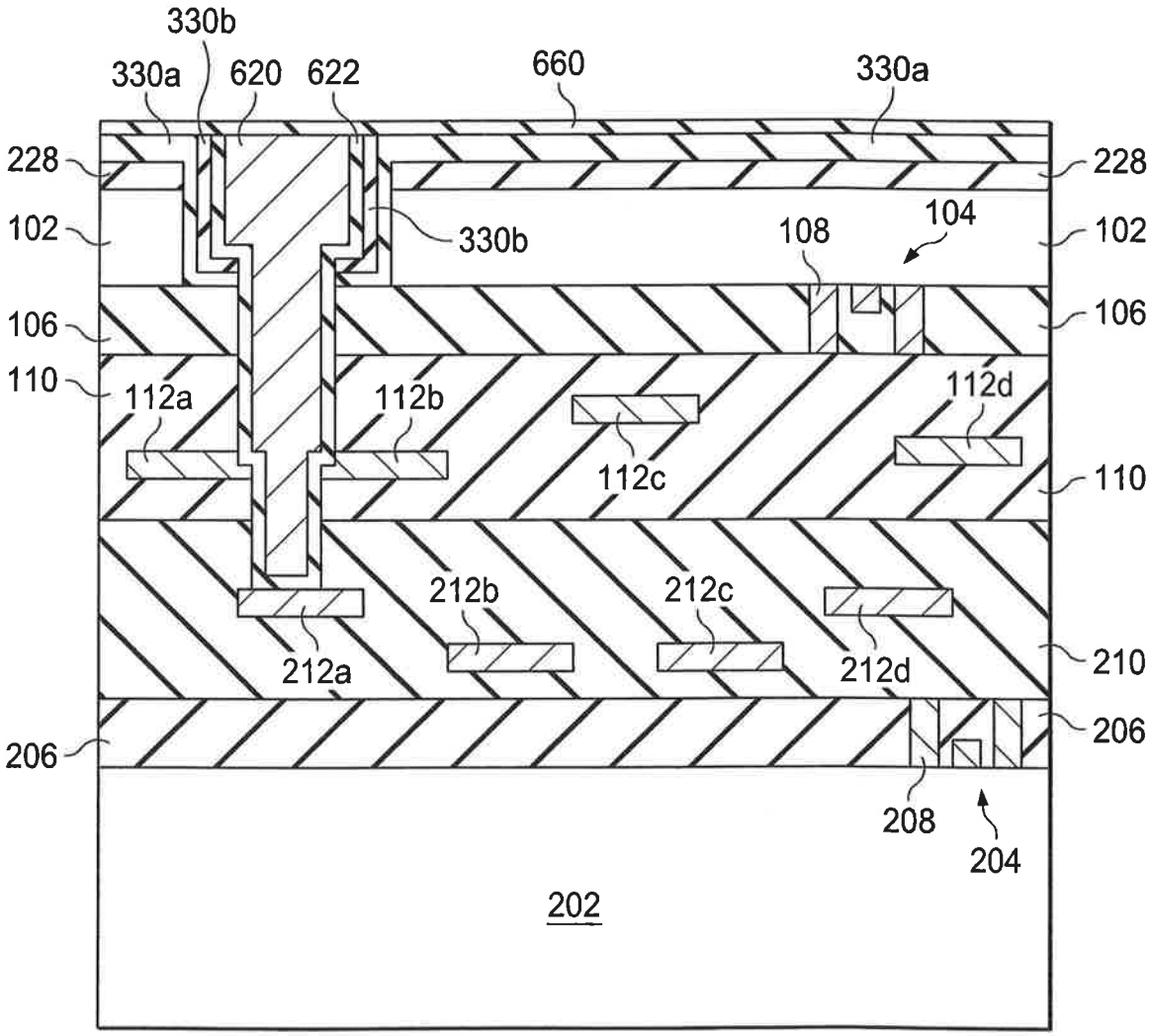

330b
330a
620
622
660
330a
228
228
102
330b
108
104
102
106
106
110
112a
112b
112c
112d
110
212b
212c
212a
212d
210
206
206
208
204
202

FIG. 7

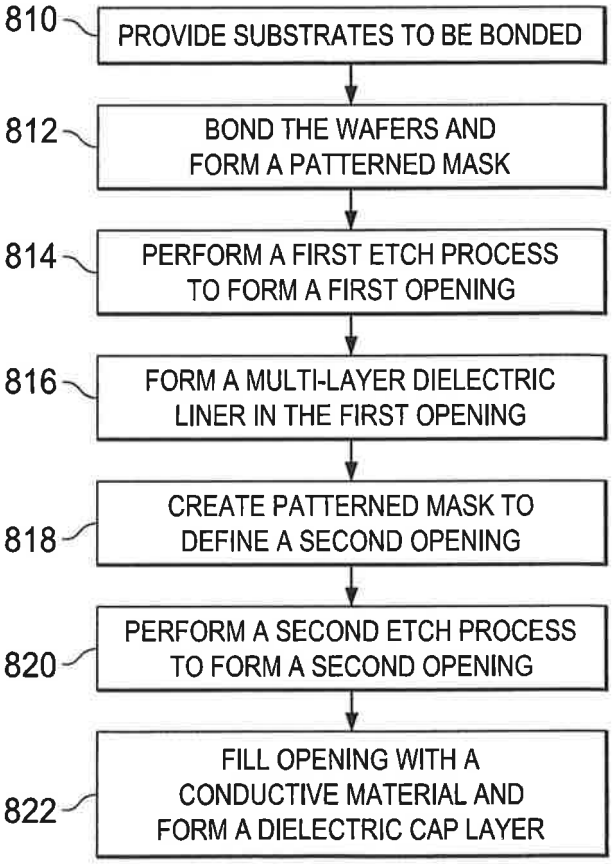

810
PROVIDE SUBSTRATES TO BE BONDED
812
BOND THE WAFERS AND FORM A PATTERNED MASK
814
PERFORM A FIRST ETCH PROCESS TO FORM A FIRST OPENING
816
FORM A MULTI-LAYER DIELECTRIC LINER IN THE FIRST OPENING
818
CREATE PATTERNED MASK TO DEFINE A SECOND OPENING
820
PERFORM A SECOND ETCH PROCESS TO FORM A SECOND OPENING
822
FILL OPENING WITH A CONDUCTIVE MATERIAL AND FORM A DIELECTRIC CAP LAYER

FIG. 8