ABSTRACT

METHOD TO REDUCE CAPACITANCE BETWEEN METAL LINES

A process for reducing device capacitance via inclusion of an air gap in a low dielectric constant (low k), layer, used to fill narrow spaces between metal lines, has been developed. The process features the formation of dual damascene metal lines, comprised with a narrow space between the top portions of the dual damascene metal structures, and a wider space between bottom portions of these same structures. Deposition of a low k layer, using a deposition procedure lacking acceptable conformality properties, results in the narrow space between top portions of the dual damascene metal structures being completely filled with low k layer, while the wider space located between bottom portions of the metal structures remains unfilled The unfilled portion of the low k layer now features an embedded air gap, resulting in decreased capacitance for the dielectric layer located between metal lines, thus reducing performance degrading RC delays

FIGURE 3

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