

The applicant has, however, observed that the production of a structure comprising a layer for trapping electric charges and a dielectric layer by means of a manufacturing method using only moderate heat treatments (that is to say not exposing the structure to temperatures above 1000°C) led to structures with radiofrequency (RF) performance levels that were much lower than expected.

As documented in the publication “White paper - RF SOI Characterisation” dated January 2015 and published by SOITEC, the RF performance of a substrate can be characterized by a second harmonic distortion measurement HD2. In the case of semiconductor structures comprising a charge trapping layer and implementing only moderate heat treatments, the applicant has observed that this HD2 characteristic could be between 55% and 75% of the expected value.

OBJECT OF THE INVENTION

Embodiments of the present invention seek to address this problem, at least in part. More particularly, embodiments of the present invention seek to provide a method for manufacturing a semiconductor structure comprising transferring a thin layer onto a support provided with a layer for trapping electric charges, with the method not employing heat treatment exposing the structure to a high temperature, but nonetheless resulting in a structure with compliant RF performance levels.

BRIEF DESCRIPTION OF THE INVENTION

An aspect of the present invention provides a method for manufacturing a structure comprising a thin layer which is composed of a piezoelectric and/or ferroelectric material and is transferred onto a support provided with a charge trapping layer, the method comprising the following steps:

- preparing the support comprising forming the trapping layer on a base substrate, the trapping layer having a hydrogen concentration of less than 10^{18} at/cm³;
- joining the support to a donor substrate by means of a dielectric layer comprising a silicon oxide having nitrogen in a nitrogen/oxygen ratio of between 0.01 and 0.25;

- removing part of the donor substrate to form the thin layer;

the manufacturing method exposing the structure to a temperature below a maximum temperature of 1000°C at least during and after the joining step.

Another aspect of the present invention provides a structure that cannot be exposed to high temperatures, for example higher than 600°C or 1000°C, the structure comprising:

- a base substrate;
- a trapping layer placed on the base substrate and having a hydrogen concentration of less than 10^{18} at/cm³;
- a dielectric layer arranged on the trapping layer, the dielectric layer comprising a silicon oxide having nitrogen in a nitrogen/oxygen ratio of between 0.01 and 0.25;
- a thin layer placed on the dielectric layer composed of a piezoelectric and/or ferroelectric material.

There is also disclosed a method for manufacturing a structure comprising a thin layer transferred onto a support provided with a charge trapping layer, the method comprising the following steps:

- preparing the support comprising forming the trapping layer on a base substrate, the trapping layer having a hydrogen concentration of less than 10^{18} at/cm³;
- joining the support to a donor substrate by means of a dielectric layer having a hydrogen concentration of less than 10^{20} at/cm³ or comprising a barrier preventing the diffusion of hydrogen toward the trapping layer or having low hydrogen diffusivity;

- removing part of the donor substrate to form the thin layer;

the manufacturing method exposing the structure to a temperature below a maximum temperature of 1000°C.

Forming a trapping layer having a low hydrogen concentration during the support preparation step avoids excessively neutralizing the electric charge traps of this layer. Forming a dielectric layer that also has a low hydrogen concentration or that prevents the diffusion of this hydrogen avoids or limits its diffusion toward the trapping layer, in particular during heat treatments to which this dielectric layer is exposed during the manufacturing method and after the joining step. Alternatively, a barrier may be provided in the dielectric layer preventing the diffusion of hydrogen from the dielectric layer toward the trapping layer.

According to other advantageous and non-limiting features of the invention, taken alone or in any technically feasible combination:

- the trapping layer is deposited at a deposition temperature between 600°C and 950°C, and the step of preparing the support comprises a first stage of annealing the trapping layer in a hydrogen depleted atmosphere and at a temperature between the deposition temperature and 1000°C;
- the deposition of the trapping layer implements an LPCVD technique;
- the trapping layer is formed by deposition at a temperature between 950°C and 1100°C;
- the deposition of the trapping layer is implemented in an epitaxy frame;
- the dielectric layer is produced by depositing a material having a hydrogen concentration of more than 10^{20} at/cm³ followed by the application of a second annealing stage in a hydrogen depleted atmosphere;
- the second annealing stage is between 800°C and 900°C for at least one hour in a neutral atmosphere;