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DOUBLE-LAYERED LOW DIELECTRIC CONSTANT DIELECTRIC DUAL DAMASCENE METHOD

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RELATED PATENT APPLICATION

U.S. Patent Application Serial # 09/726,657 (CS-00-024) to Q.S. Fong et al.

BACKGROUND OF THE INVENTION

(1) Field of the Invention

The invention relates to a method of metallization in the fabrication of integrated circuits, and more particularly, to a method of dual damascene metallization using low dielectric constant materials in the manufacture of integrated circuits.

(2) Description of the Prior Art

The damascene or dual damascene process has become a future trend in integrated circuit manufacturing, especially in the copper metallization process. These processes are discussed in ULSI Technology, by Chang and Sze, The McGraw Hill Companies, Inc., NY, NY, c. 1996, pp. 444-445. Low dielectric constant materials have been proposed as the dielectric materials in order to reduce capacitance. In

the conventional damascene scheme, one or more etch stop and/or barrier layers comprising high dielectric constant materials, such as silicon nitride, are required. This defeats the purpose of the low dielectric constant materials. It is desired to find a process which does not require a high dielectric constant etch stop/barrier layer.

U.S. Patent 6,004,883 to Yu et al shows a dual damascene method without an etch stop layer. U.S. Patent 6,083,822 to Lee shows a dual damascene method using a thin silicon nitride etch stop layer. U.S. Patent 6,025,259 to Yu et al discloses a dual damascene method with etch stop layers. U.S. Patent 6,071,809 to Zhao shows a method using an etch stop layer. U.S. Patent 5,635,423 to Huang et al teaches various methods of forming a dual damascene opening. An etch stop layer such as silicon nitride or polysilicon is used. U.S. Patents 5,935,762 to Dai et al and 5,877,076 to Dai show a double mask self-aligned process using a silicon nitride etch stop layer. U.S. Patent 5,741,626 to Jain et al discloses a dual damascene process using a tantalum nitride etch stop layer.

SUMMARY OF THE INVENTION

A principal object of the present invention is to provide an effective and very manufacturable method of metallization in the fabrication of integrated circuit devices.

Another object of the invention is to provide a dual damascene metallization process using low dielectric constant materials.

Yet another object of the invention is to provide a dual damascene metallization process using low dielectric constant materials without using a high dielectric constant etch stop material.

A further object of the invention is to provide a double layered low dielectric constant material dual damascene metallization process.

A still further object of the invention is to provide a double layered low dielectric constant material via first dual damascene metallization process.

Another object of the invention is to provide a double layered low dielectric constant material dual trench first damascene metallization process.

Yet another object of the invention is to provide a double layered low dielectric constant material self-aligned dual damascene metallization process.

In accordance with the objects of this invention a double layered low dielectric constant material dual damascene metallization process is achieved. Metal lines are provided covered by an insulating layer overlying a semiconductor substrate. A first organic dielectric layer is deposited overlying the insulating layer. A second inorganic dielectric layer is deposited overlying the first dielectric layer. In a first method, a via pattern is etched into the second dielectric layer. The via pattern is etched into the first dielectric layer using the patterned second dielectric layer as a mask. Thereafter, a trench pattern is etched into the second inorganic dielectric layer to complete dual damascene openings. In a second method, a trench pattern is etched into the second dielectric layer. Thereafter, a via pattern is etched through the second inorganic dielectric layer and the first organic dielectric layer to complete dual damascene openings. In a third method, a via pattern is

etched into the second dielectric layer. Then, simultaneously, the via pattern is etched into the first dielectric layer and a trench pattern is etched into the second inorganic dielectric layer to complete dual damascene openings in the fabrication of an integrated circuit device.

BRIEF DESCRIPTION OF THE DRAWINGS

In the accompanying drawings forming a material part of this description, there is shown:

Figs. 1 through 7 schematically illustrate in cross-sectional representation a first preferred embodiment of the dual damascene process of the present invention.

Figs. 8 through 13 schematically illustrate in cross-sectional representation a second preferred embodiment of the dual damascene process of the present invention.

Figs. 14 through 19 schematically illustrate in cross-sectional representation a third preferred embodiment of the dual damascene process of the present invention.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

The present invention provides a double-layered low dielectric constant material dual damascene process. A high dielectric constant material etch stop/barrier layer is not required in the process of the present invention. The present invention is described for three preferred embodiments. In the first preferred embodiment, a via first dual damascene process is described with reference to Figs. 1-7. In the second preferred embodiment, a trench first dual damascene process is described with reference to Figs. 8-13. In the third preferred embodiment, a self-aligned dual damascene process is described with reference to Figs. 14-19.

The first preferred embodiment, a via first dual damascene process, will now be described with reference to Figs. 1-7. Referring now more particularly to Fig. 1, there is illustrated a portion of a partially completed integrated circuit device. There is shown a semiconductor substrate 10, preferably composed of monocrystalline silicon. Semiconductor devices structures, such as gate electrodes, source and drain regions, and metal interconnects, not shown, are formed in and on the semiconductor substrate and covered with an insulating layer. Interconnection lines, such as

tungsten, copper or aluminum-copper lines 14, for example, are formed over the insulating layer and will contact some of the underlying semiconductor device structures through openings in the insulating layer, not shown.

Now, a passivation or barrier layer 16 is formed over the metal lines and planarized. Now, the key features of the present invention will be described. A first dielectric layer 18 is deposited over the barrier layer 16 to a thickness of between about 6000 and 20,000 Angstroms. This dielectric layer 18 comprises a low dielectric constant organic material, such as polyimides, HOSP, SILK, FLARE, BCB, methylsilsesquioxane (MSQ), or any organic polymers. The dielectric constant should be less than about 3.5.

Next, a second dielectric layer 20 is deposited to a thickness of between about 6000 and 20,000 Angstroms. The second dielectric layer 20 comprises a low dielectric constant inorganic material, such as fluorinated silicate glass (FSG), carbon-doped FSG, nitrogen-doped FSG, CORAL, BLACK Diamond, Z3MS, XLK (by Dow Corning), and hydrogen silsesqioxane (HSQ). The dielectric constant should be less than about 3.5. Alternatively, the first dielectric layer could be inorganic and the second layer could be organic.

Referring now to Fig. 2, a photoresist layer is coated over the second dielectric layer 20 and patterned to form a photoresist mask 25 for the via pattern. The second dielectric layer 20 is etched where it is not covered by the photoresist mask 25 to form the via pattern, as shown in Fig. 3. The photoresist mask 25 is removed. If the second dielectric layer is an organic layer, a hard mask must be used instead of the photoresist mask since subsequent removal of the photoresist will damage the organic material as well.

Now, the patterned second dielectric layer serves as a hard mask for etching the via pattern into the first dielectric layer 18, as shown in Fig. 4.

Referring now to Fig. 5, a second photoresist layer is coated over the second dielectric layer 20 and patterned to form the photoresist mask 29 having a trench pattern. Alternatively, a hard mask could be used instead of photoresist. The hard mask material must have sufficient etch selectivity compared to the inorganic dielectric material deposited to prevent etching of the inorganic material during patterning.

The trench pattern is etched into the second dielectric layer 20, as shown in Fig. 6. The etching recipe is chosen to etch the second dielectric layer with a high selectivity to the first dielectric material. In this way, the first dielectric material acts as an etch stop.

The photoresist mask 29 is removed, leaving the completed dual damascene openings 32, shown in Fig. 6. The process of the invention has formed the dual damascene openings using a double layer of low dielectric constant materials. No high dielectric constant material was used as an etch stop. Therefore, low capacitance is maintained.

Processing continues as is conventional in the art to fill the damascene openings 32. For example, a barrier metal layer, not shown, is typically deposited over the third dielectric layer and within the openings. A metal layer, such as copper, is formed within the openings, such as by sputtering, electroless plating, or electroplating, for example. The excess metal may be planarized to complete the metal fill 34, as shown in Fig. 7.

The second preferred embodiment, a trench first dual damascene process, will now be described with reference to Figs. 8-13. Referring now more particularly to

Fig. 8, there is illustrated a portion of a partially completed integrated circuit device. There is shown a semiconductor substrate 10, preferably composed of monocrystalline silicon. Semiconductor devices structures, such as gate electrodes, source and drain regions, and metal interconnects, not shown, are formed in and on the semiconductor substrate and covered with an insulating layer. Interconnection lines, such as tungsten, copper or aluminum-copper lines 14, for example, are formed over the insulating layer and will contact some of the underlying semiconductor device structures through openings in the insulating layer, not shown.

Now, a passivation or barrier layer 16 is formed over the metal lines and planarized. Now, the key features of the present invention will be described. A first dielectric layer 18 is deposited over the barrier layer 16 to a thickness of between about 6000 and 20,000 Angstroms. This dielectric layer 18 comprises a low dielectric constant organic material, such as polyimides, HOSP, SILK, FLARE, BCB, MSQ, or any organic polymers.

Next, a second low dielectric layer 20 is deposited to a thickness of between about 6000 and 20,000 Angstroms. The second dielectric layer 20 comprises a low

dielectric constant inorganic material, such as fluorinated silicate glass (FSG), carbon-doped FSG, nitrogen-doped FSG, CORAL, BLACK Diamond, Z3MS, XLK, and HSQ. The dielectric constant should be less than about 3.5. Alternatively, the first dielectric layer could be inorganic and the second layer could be organic.

Referring now to Fig. 9, a photoresist layer is coated over the second dielectric layer 20 and patterned to form a photoresist mask 29 for the trench pattern. The second dielectric layer 20 is etched where it is not covered by the photoresist mask 29 to form the trench pattern, as shown in Fig. 10. The photoresist mask 29 is removed. If the second dielectric layer is an organic layer, a hard mask must be used instead of the photoresist mask since subsequent removal of the photoresist will damage the organic material as well.

Referring now to Fig. 11, a second photoresist layer is coated over the patterned second dielectric layer 20 and patterned to form the photoresist mask 25 having a via pattern. Alternatively, a hard mask could be used instead of photoresist. The hard mask material must have sufficient etch selectivity compared to the inorganic dielectric material deposited to prevent etching of the inorganic

material during patterning.

The via pattern is etched into the first dielectric layer 18, as shown in Fig. 12. The photoresist mask 25 is removed, leaving the completed dual damascene openings 32, shown in Fig. 12. The process of the invention has formed the dual damascene openings using a double layer of low dielectric constant materials. No high dielectric constant material was used as an etch stop. Therefore, low capacitance is maintained.

Processing continues as is conventional in the art to fill the damascene openings 32. For example, a barrier metal layer, not shown, is typically deposited over the third dielectric layer and within the openings. A metal layer, such as copper, is formed within the openings, such as by sputtering, electroless plating, or electroplating, for example. The excess metal may be planarized to complete the metal fill 34, as shown in Fig. 13.

The third preferred embodiment, a self-aligned dual damascene process, will now be described with reference to Figs. 14-19. Referring now more particularly to Fig. 14, there is illustrated a portion of a partially completed integrated circuit device. There is shown a semiconductor

substrate 10, preferably composed of monocrystalline silicon. Semiconductor devices structures, such as gate electrodes, source and drain regions, and metal interconnects, not shown, are formed in and on the semiconductor substrate and covered with an insulating layer. Interconnection lines, such as tungsten, copper or aluminum-copper lines 14, for example, are formed over the insulating layer and will contact some of the underlying semiconductor device structures through openings in the insulating layer, not shown.

Now, a passivation or barrier layer 16 is formed over the metal lines and planarized. Now, the key features of the present invention will be described. A first dielectric layer 18 is deposited over the barrier layer 16 to a thickness of between about 6000 and 20,000 Angstroms. This dielectric layer 18 comprises a low dielectric constant organic material, such as polyimides, HOSP, SILK, FLARE, BCB, MSQ, or any organic polymers.

Next, a second low dielectric layer 20 is deposited to a thickness of between about 6000 and 20,000 Angstroms. The second dielectric layer 20 comprises a low dielectric constant inorganic material, such as fluorinated silicate glass (FSG), carbon-doped FSG, nitrogen-doped FSG, CORAL, BLACK Diamond, Z3MS, XLK, and HSQ. The dielectric

constant should be less than about 3.5. Alternatively, the first dielectric layer could be inorganic and the second layer could be organic.

Referring now to Fig. 15, a photoresist layer is coated over the second dielectric layer 20 and patterned to form a photoresist mask 25 for the via pattern. The second dielectric layer 20 is etched where it is not covered by the photoresist mask 25 to form the via pattern, as shown in Fig. 16. The photoresist mask 25 is removed. If the second dielectric layer is an organic layer, a hard mask must be used instead of the photoresist mask since subsequent removal of the photoresist will damage the organic material as well.

Referring now to Fig. 17, a second photoresist layer is coated over the second dielectric layer 20 and patterned to form the photoresist mask 29 having a trench pattern.

The trench and via patterns are etched simultaneously into the second dielectric layer 20 and the first dielectric layer 18, respectively, as shown in Fig. 18. Since the two dielectric layers comprise different materials, two etching recipes must be used, one for the organic

material and another for the inorganic material.

The photoresist mask 29 is removed, leaving the completed dual damascene openings 32, shown in Fig. 18. The process of the invention has formed the dual damascene openings using a double layer of low dielectric constant materials. No high dielectric constant material was used as an etch stop. Therefore, low capacitance is maintained.

Processing continues as is conventional in the art to fill the damascene openings 32. For example, a barrier metal layer, not shown, is typically deposited over the third dielectric layer and within the openings. A metal layer, such as copper, is formed within the openings, such as by sputtering, electroless plating, or electroplating, for example. The excess metal may be planarized to complete the metal fill 34, as shown in Fig. 19.

The process of the present invention provides three simple and manufacturable dual damascene processes where only low dielectric constant materials are used. No high dielectric constant materials are required as etch stops. The process of the invention uses a novel double layer of low dielectric constant materials to form dual damascene openings in the manufacture of integrated circuits.

While the invention has been particularly shown and described with reference to the preferred embodiments thereof, it will be understood by those skilled in the art that various changes in form and details may be made without departing from the spirit and scope of the invention.

CLAIMS:-

1. A method of forming dual damascene openings in the fabrication of an integrated circuit device comprising:

providing metal lines covered by an insulating layer overlying a semiconductor substrate;

depositing a first organic dielectric layer overlying said insulating layer;

depositing a second inorganic dielectric layer overlying said first dielectric layer;

etching a via pattern into said second dielectric layer;

etching said via pattern into said first dielectric layer using patterned said second dielectric layer as a mask; and

thereafter etching a trench pattern into said second inorganic dielectric layer to complete said forming of said dual damascene openings in the fabrication of said integrated circuit device.

2. The method according to Claim 1 further comprising forming semiconductor device structures including gate electrodes and source and drain regions in and on said semiconductor substrate wherein said metal lines overlie and contact said semiconductor device structures.

3. The method according to Claim 1 wherein said first organic dielectric layer comprises one of the group containing: polyimides, HOSP, SILK, FLARE, BCB, MSQ, and organic polymers.

4. The method according to Claim 1 wherein said second inorganic dielectric layer comprises one of the group containing: CORAL, BLACK DIAMOND, FSG, carbon-doped FSG, nitrogen-doped FSG, Z3MS, XLK, and HSQ.

5. The method according to Claim 1 further comprising filling said dual damascene openings with a metal layer.

6. A method of forming dual damascene openings in the fabrication of an integrated circuit device comprising:

providing metal lines covered by an insulating layer overlying a semiconductor substrate;

depositing a first organic dielectric layer overlying said insulating layer;

depositing a second inorganic dielectric layer overlying said first dielectric layer;

etching a trench pattern into said second dielectric layer; and

thereafter etching a via pattern through said second inorganic dielectric layer and said first organic

dielectric layer to complete said forming of said dual damascene openings in the fabrication of said integrated circuit device.

7. The method according to Claim 6 further comprising forming semiconductor device structures including gate electrodes and source and drain regions in and on said semiconductor substrate wherein said metal lines overlie and contact said semiconductor device structures.

8. The method according to Claim 6 wherein said first organic dielectric layer comprises one of the group containing: polyimides, HOSP, SILK, FLARE, BCB, MSQ, and organic polymers.

9. The method according to Claim 6 wherein said second inorganic dielectric layer comprises one of the group containing: CORAL, BLACK DIAMOND, FSG, carbon-doped FSG, nitrogen-doped FSG, Z3MS, XLK, and HSQ.

10. The method according to Claim 6 further comprising filling said dual damascene openings with a metal layer.

11. A method of forming dual damascene openings in the fabrication of an integrated circuit device comprising:

providing metal lines covered by an insulating layer overlying a semiconductor substrate;

depositing a first organic dielectric layer overlying said insulating layer;

depositing a second inorganic dielectric layer overlying said first dielectric layer;

etching a via pattern into said second dielectric layer; and

simultaneously etching said via pattern into said first dielectric layer and etching a trench pattern into said second inorganic dielectric layer to complete said forming of said dual damascene openings in the fabrication of said integrated circuit device.

12. The method according to Claim 11 further comprising forming semiconductor device structures including gate electrodes and source and drain regions in and on said semiconductor substrate wherein said metal lines overlie and contact said semiconductor device structures.

13. The method according to Claim 11 wherein said first organic dielectric layer comprises one of the group containing: polyimides, HOSP, SILK, FLARE, BCB, MSQ, and organic polymers.

14. The method according to Claim 11 wherein said second inorganic dielectric layer comprises one of the group containing: CORAL, BLACK DIAMOND, FSG, carbon-doped FSG, nitrogen-doped FSG, Z3MS, XLK, and HSQ.

15. The method according to Claim 11 further comprising filling said dual damascene openings with a metal layer.

16. A method of forming dual damascene openings in the fabrication of an integrated circuit device comprising:

providing metal lines covered by an insulating layer overlying a semiconductor substrate;

depositing a first inorganic dielectric layer overlying said insulating layer;

depositing a second organic dielectric layer overlying said first dielectric layer;

etching a via pattern into said second dielectric layer;

etching said via pattern into said first dielectric layer using patterned said second dielectric layer as a mask; and

thereafter etching a trench pattern into said second inorganic dielectric layer to complete said forming of said dual damascene openings in the fabrication of said integrated circuit device.

17. The method according to Claim 16 further comprising forming semiconductor device structures including gate electrodes and source and drain regions in and on said semiconductor substrate wherein said metal lines overlie and contact said semiconductor device structures.

18. The method according to Claim 16 wherein said first inorganic dielectric layer comprises one of the group containing: CORAL, BLACK DIAMOND, FSG, carbon-doped FSG, nitrogen-doped FSG, Z3MS, XLK, and HSQ.

19. The method according to Claim 16 wherein said second organic dielectric layer comprises one of the group containing: polyimides, HOSP, SILK, FLARE, BCB, MSQ, and organic polymers.

20. The method according to Claim 16 further comprising filling said dual damascene openings with a metal layer.

21. A method of forming dual damascene openings in the fabrication of an integrated circuit device comprising:

providing metal lines covered by an insulating layer overlying a semiconductor substrate;

depositing a first inorganic dielectric layer overlying said insulating layer;

depositing a second organic dielectric layer overlying said first dielectric layer;

etching a trench pattern into said second dielectric layer; and

thereafter etching a via pattern through said second inorganic dielectric layer and said first organic dielectric layer to complete said forming of said dual damascene openings in the fabrication of said integrated circuit device.

22. The method according to Claim 21 further comprising forming semiconductor device structures including gate electrodes and source and drain regions in and on said semiconductor substrate wherein said metal lines overlie and contact said semiconductor device structures.

23. The method according to Claim 21 wherein said first inorganic dielectric layer comprises one of the group containing: CORAL, BLACK DIAMOND, FSG, carbon-doped FSG, nitrogen-doped FSG, Z3MS, XLK, and HSQ.

24. The method according to Claim 21 wherein said second organic dielectric layer comprises one of the group containing: polyimides, HOSP, SILK, FLARE, BCB, MSQ, and organic polymers.

25. The method according to Claim 21 further comprising filling said dual damascene openings with a metal layer.

26. A method of forming dual damascene openings in the fabrication of an integrated circuit device comprising:

providing metal lines covered by an insulating layer overlying a semiconductor substrate;

depositing a first inorganic dielectric layer overlying said insulating layer;

depositing a second organic dielectric layer overlying said first dielectric layer;

etching a via pattern into said second dielectric layer; and

simultaneously etching said via pattern into said first dielectric layer and etching a trench pattern into said second inorganic dielectric layer to complete said forming of said dual damascene openings in the fabrication of said integrated circuit device.

27. The method according to Claim 26 further comprising forming semiconductor device structures including gate electrodes and source and drain regions in and on said semiconductor substrate wherein said metal lines overlie and contact said semiconductor device structures.

28. The method according to Claim 21 wherein said first inorganic dielectric layer comprises one of the group containing: CORAL, BLACK DIAMOND, FSG, carbon-doped FSG, nitrogen-doped FSG, Z3MS, XLK, and HSQ.

29. The method according to Claim 26 wherein said second organic dielectric layer comprises one of the group containing: polyimides, HOSP, SILK, FLARE, BCB, MSQ, and organic polymers.

30. The method according to Claim 21 further comprising filling said dual damascene openings with a metal layer.