DIFFERENTIAL PHASE TRACKING CIRCUIT

BACKGROUND OF THE INVENTION

1. FIELD OF THE INVENTION

This invention relates to improvements in dynamic information storage or retrieval systems and methods, and more particularly to improvements in such systems and methods for the storage or retrieval of arbitrarily variable information which is retained in a storage medium by variation of a optical characteristic thereof by sensing a variation of a physical characteristic of the storage medium by a transducer having relative motion along a continuous path, and still more particularly to improvements in such systems and methods involving optical servo systems for controlling the tracking of an optical data sensing transducer.

2. RELEVANT BACKGROUND

In typical optical disc apparatuses, data is arranged in a concentric or spiral fashion around the disk, and a laser beam is positioned such that its beam spot falls on and follows the center of the target track. A typical prior art optical disc data sensing apparatus or transducer for reading information from an optical disc is shown in Figure 1, to which reference is now made. Laser light is emitted from a laser diode 12 and passes through a beam splitter prism 14, a collimating lens 16, and a focusing lens 18. The focusing lens 18 focuses the laser light onto a particular track (not shown) of the optical disc 20.

Laser light is reflected from the surface of the disc 20 and passes through the focusing lens 18 and the collimating lens 16. The light then reflects from the surface of the beam splitter prism 14 through a cylindrical lens 22 to finally illuminate a photo-detector array 24. The photo-detector array 24 converts the

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received light energies into electric signals. The entire apparatus is known as the "pickup", which serves as the transducer element for the data pattern recorded on the optical disc 20.

The focusing lens 18 is typically held in a lens holder attached by a spring mechanism to a pickup body (not shown). The position of the lens is controlled by permanent magnets (now shown) mounted to the pickup body. Wire coils 19 attached to the lens holder carry electric currents that generate magnetic force that interacts with the magnets and moves the lens holder relative to the pickup body. Both a focusing coil and a radial coil may be used to control the focus and radial movements, respectively. The position of the focusing lens 18 is controlled with the lens holder being driven in accordance with the control signals flowing into the focusing and tracking coils 19.

The laser beam positioning is typically achieved by a feedback control system, which includes a feedback tracking error signal circuit 25, a linear feedback controller 26, and a lens actuator, which includes the focusing and tracking coils 19 and a power amplifier 27. A data recovery circuit 23 is provided to recover data from the photo-detector array 24, in known manner.

Figure 2 depicts a laser beam spot 30 after it has been reflected from an optical disc onto a photo-detector array 24 in the operation of the circuit of Figure 1. The example array 24 is a four-point tracker array in which the array is divided into four quadrants, denoted a, b, c, and d. Each quadrant has its own photodiode and photo-detector output (not shown). The laser beam spot 30 is shown at its peak, not being scattered by patterns that may exist in the optical groove of the disc. This shift in the reflection of the beam spot causes the divisions of the photo-detector array to be illuminated to different degrees. This varying degree of illumination of the photo-detector is used in the generation of a tracking error signal. More particularly, the

signal pairs a+c and b+d have a time delay difference that is linearly proportional to track position error. When the focusing lens is not properly positioned, data may not be read correctly from the desired track of the optical disc. Consequently, the presence of a tracking error indicates that the beam spot is not in the proper position to read data from the optical disc. Thus, ideally, each of the divisions of the photo-detector array should be illuminated equally.

The tracking error signal typically has a linear relationship with respect to the position error, such that its magnitude is directly proportional to the distance of the beam spot away from track center. In an ideal feedback control system, the laser beam is positioned exactly at the track center. However, due to noise injected at the tracking error signal generator, the beam spot could be positioned off the track center. It is therefore imperative to minimize noise in the process of generating a tracking error signal in response to position error.

For a dual-layer optical disk, a differential phase detection (DPD) method has become the preferred method for generating the tracking error. A typical DPD implementation is illustrated in Figure 3. A photo-detector 24, of construction similar to the photo-detector described above with reference to Figure 2, is divided into separate light receiving areas a, b, c, and d. The intersection of the dividing lines that form the four areas is aligned with the optical axis of a reflected laser beam from the surface of an optical disk 20, as described above. The outputs of the photo-detectors are paired diagonally and amplified by amplifiers 40 and 42 to produce the light signals 34 and 36 shown in Figure 4A. These analog signals are converted to digital signals by signal level comparators 44 and 46, after equalization of the waveform by equalizers 48 and 50. The equalizers typically have frequency response characteristics such that higher frequency

signals are given relatively higher gain, thus to ensure that narrower, and hence smaller, pulses are sufficiently amplified so that with a fixed gain level comparators the outputs reach full digital levels, as shown by the signals 52 and 54 in Figure 4A.

Figures 4B and 4C show the effects of an analog equalizer in the circuit. More particularly, as shown in Figure 4B, if no analog equalizer is employed, the circuit may miss the occurrence of a narrow pulse that is sandwiched between two wider pulses. On the other hand, using an equalizer, the narrow pulse is detected, as shown in Figure 4C. The analog equalizer may have a frequency response such that lower frequency signals receive less amplification than higher frequency signals. Since analog signals coming from the pickup have the characteristic that higher frequency signals (narrower pulses) have less amplitude, the analog equalizer serves to "pump" these weaker pulses up to similar amplitudes as the wider pulses. In Figure 4C, it is shown that the narrower pulses have similar amplitudes as the wider ones, as a consequence of using an analog equalizer.

With reference again to Figure 3, a phase comparator 56 compares the phases of the transitions of the digitized pulse signals 52 and 54, and produces time lag signals UP 60 and DN 62 indicating the delay difference between digitized signals B1 and B2. The UP 60 and DN 62 signals are received by a charge pump 64, which in turns outputs a positive or negative charge package of charge amount directly proportional to the duration of the UP or DN pulses into a parallel resistor-capacitor network. The capacitor voltage is further filtered by a low-pass filter 68 to produce an analog tracking error signal. Further details of the operation of this circuit can be found in the ECMA Standards document ECMA-272 (1998) 120mm DVD Rewritable disk (DVD-RAM), which is incorporated herein by reference.

The principle behind DPD systems is that delay difference between different photodetector signal pairs is directly proportional to laser beam spot position error with respect to track center. However, it is observed by the present inventors that the prior art DPD implementation results in a tracking error signal level that not only depends on this delay difference but also on the pulse patterns. Over time, given a certain pulse width of the UP (or DN) pulse trains corresponding to a certain tracking position error, the average current density pumped across the load resistor is a function of not only the pulse widths of UP (or DN) but also the frequency of occurrence of the UP (or DN) pulses. In a CD or DVD disk, data patterns vary from 3T to 11T (CD) or 14T (DVD), resulting in UP or DN pulse rate varying over a roughly 4 to 1 range. Such data dependency of the tracking error signal creates perturbation of the beam spot position.

Previous systems also require an array of analog equalizer circuits to amplify narrower, hence smaller, pulses corresponding to 3T or 4T data pulses. In the absence of such equalizer array, as discussed above, some narrow pulses (such as 3T) adjacent to much wider pulses (such as 10T) could fail to drive the comparators adequately to reach full digital levels thus resulting sometimes in missing pulses in both or, worse, one of the B1 and B2 signals. However, use of the analog equalizer array adds delay mismatch between B1 and B2 due to inherent limitation of precision of component matching. Furthermore, as is often the case, if this delay difference varies with different frequencies, the consequence is a varying delay difference error injected into signals B1 and B2 that is indistinguishable from noise being added to the tracking error signal. There is therefore a need to provide an alternative DPD implementation that does not require analog equalizers to relatively amplify the narrower pulses.

SUMMARY OF THE INVENTION

The present application discloses an improved circuit and method for generating differential phase detection tracking error in optical disc media. A photo-detector comprising four separate light receiving areas receives light reflected from the surface of an optical disc. The photodetector generates signals from the light received. The signals are converted into digital pulses that indicate a change of threshold, for example, between pits and land. A phase difference of the digital signals is measured, and discrete voltage signals are produced that indicate the phase difference between the signals. Valid phase difference measurements are stored in a ping-pong capacitor charge pump. The latest valid phase measurement is then selected and filtered to produce a tracking error signal.

An advantage of the disclosed methods and structures, in various embodiments is that the tracking error signal produced is free of noise introduced by input pulse density fluctuation.

Another advantage of the invention is it is inherently unsusceptible to missing pulses in the input signals to the phase comparator, thus eliminating the need for costly analog equalizers, and their attendant noise problems.

BRIEF DESCRIPTION OF THE DRAWINGS

The invention will be illustrated in the accompanying drawings, in which:

Figure 1 shows an arrangement of parts of the pickup assembly or optical sensor for detecting optical sensor data of a DVD structure, or the like, including feedback circuitry for positioning the pickup assembly, according to the prior art.

Figure 2 illustrates a typical optical disc sensor array for use in conjunction with the optical sensor of Figure 1, according to the prior art.

Figure 3 shows a differential phase detection tracking error circuit, according to the prior art.

Figure 4A shows various waveforms produced by the circuit of Figure 3.

Figure 4B shows the waveforms of the circuit of Figure 1, when it is operated without an equalizer circuit, in which a narrow pulse that is sandwiched between wide pulses can result in a missing pulse.

Figure 4C shows the waveforms of the circuit of Figure 1, when it is operated with an equalizer circuit, in which a narrow pulse that is sandwiched between wide pulses is detected.

Figure 5 shows the architecture of a differential phase detection tracking error circuit, according to a preferred embodiment of the invention.

Figures 6A and 6b show details of the phase comparator of the circuit of Figure 5.

Figure 7 shows details of the output switch logic circuit of Figure 5.

Figure 8 shows details of the ping-pong logic circuit of Figure 5.

Figure 9 shows details of the reset logic circuit of Figure 5.

Figure 10 shows details of the ping-pong charge pump of Figure 5.

Figure 11 shows details of the output switch circuit of Figure 5.

Figure 12 shows waveforms produced by the circuit of Figure 5 in operation.

In the various figures of the drawings, like reference numerals are used to denote like or similar parts.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Figure 5 shows a differential phase detection tracking error circuit (DPD-TE) 100, according to a presently preferred embodiment

of the invention. The outputs of a photo-detector 102 are paired diagonally and amplified by amplifiers 104 and 106 to produce signals A1 and A2. The signals A1 and A2 are digitized by level comparators 108 and 110 without equalization of the waveform, in contrast to methods of the prior art, to produce digital signals B1 and B2.

A phase comparator 112 produces time lag signals Up and Dn from the digitized signals B1 and B2. However, the phase comparator 112 also produces a validation flag, v. The Up and Dn signals are provided to a ping-pong logic circuit 114 and to an output switch logic circuit 116. The validation flag, v, is supplied to a reset logic circuit 118 and to the output switch logic circuit 116, along with the Up and Dn signals.

The output switch logic 116 produces an ANB signal, which is received by the reset logic 118, the ping-pong logic 114, and an output switch 120. The ping-pong logic 114 produces ping-pong signals: UPA, UPB, DNA, and DNB. Additionally, the reset logic 118 produces two signals: Ra and Rb. These six signals drive a ping-pong charge pump 122. The charge pump produces charges Va and Vb from its capacitors CA and CB (described below).

The output switch 120 receives the charge signals Va and Vb from the ping-pong charge pump 122, and directs a selected one of them to output, Cout, based on the ANB signal, which it receives from the output switch logic 116. Cout is filtered through a low pass filter 124 to produce a tracking error (TE) signal 126 which can be used to position an optical disc transducer element, such as that depicted in Figure 1.

The architecture of the phase comparator circuit and validation flag generator 112 of Figure 5 are shown in Figures 6A and 6B to which reference is now additionally made. The phase comparator circuit is shown in Figure 6A, and includes four D-type positive-edge-triggered flip-flops 130-133, each with active low

clear inputs. The Up and Dn signals are produced by separate, parallel configurations circuit blocks 136 and 138. The signal B1 for block 136 and signal B2 for block 138 act as clock signals respectively to flip-flops 130 and 131, and to flip-flops 132 and 133. The logic "1" state signal present at the D inputs of each of the flip-flops 130-133 is transferred to the respective Q outputs of the flip-flips, upon application of either the B1 or the B2 signals.

The Up signal generated by block 136 is created by a two-input OR gate 140, with B1R (from the Q output of D-type flip-flop 136) and B1F (from the Q output of D-type flip-flop 131) as its inputs. On the other hand, the Dn signal generated by block 138 is created by a two-input OR gate 142, with B2R (from the Q output of D-type flip-flop 132) and B2F (from the Q output of D-type flip-flop 133) as its inputs.

The low clear input, R(bar), is supplied by OR-type gates 146, 148, 150, 152, 156, 158, 160, and 162. More particularly, the R(bar) input for the D-type flip-flop 130 is created by a three input NOR gate 146, having as its inputs B2, B1F, and the output of a two-input OR gate 148, which has B1R, and the complement of B1 as its inputs. The R(bar) input for the D-type flip-flop 131 is created by a three input NOR gate 150, having as its inputs B1R, the complement of B2, and the output of a two-input OR gate 152, which has B1 and B1F as its inputs.

The R(bar) input for the D-type flip-flop 132 is created by a three input NOR gate 156, having as its inputs, B1, B2F, and the output of a two-input OR gate 158, which has B2R and the complement of B2 as its inputs. The R(bar) input for the D-type flip-flop 133 is created by a three input NOR gate 160, having as its inputs, B2R and the complement of B1, and the output of a two-input OR gate 432, which has B2 and B2F as its inputs.

In operation, if a rising edge from B1 arrives, B1R is asserted, thereby asserting the UP signal. However, when B2 already is high, that is, when the rising edge of B2 precedes B1, the B2 signal path resets the D-type flip-flop 130. Also, after B1R is asserted, it can be deasserted either by B1 becoming low, since the B1 signal path resets the B1R flip-flop 130, or by B2 becoming high. Finally, if a B1 falling edge has asserted B1F and no B2 falling edge has arrived to deassert B1F before B1 rises (i.e. B2 misses a pulse), then B1R is prevented from being >asserted. B1 being high also resets the B1F signal. The consideration for B1F flip-flop is similar to that of the B1R, except with the role of B1F signal in the reset of flip-flop replaced by the B1R signal. Finally, the DN signal generation is similar to that of the UP signal, except with the role of B1 and B2 and their derivatives interchanged.

The validation flag generator architecture 164 of the phase comparator 112 is shown in Figure 6B. The validation flag is generated on line 166, as the output of a D-type, positive-edged, flip-flop 168 with active low clear. The clock signal to the D-type flip-flop 168 is provided by the output of a two-input OR gate 170 having the Up and Dn signals generated by the phase comparator circuit, described above, as its inputs. The logic "1" signal present at the D input terminal is clocked to Q upon a low-to-high transition of either the Up or Dn signal, to provide the *v* output signal.

The low clear input, R(bar), is driven by a 4-input NOR gate 172, having at each of its inputs a two-input OR gate, 174, 176, 178, and 180, respectively. The OR gate 174 has inputs B1R and B1, the OR gate 176 has inputs B1F and B1, the OR gate 178 has inputs B2R and B2, and the OR gate 180 has inputs B2F and B2. The validation flag is used to assure that signals generated are consistent with the upper and lower comparator signals B1 and B2 in

order to validate or invalidate phase comparator pulses. At the end of each comparator pulse, the validation flag can be deasserted to declare the pulse invalid.

The validation flag, v, is asserted when the UP pulse begins. It remains asserted after UP pulse ends if and only if the UP pulse is valid. Any one of two conditions can cause the validation flag to be deasserted before the UP pulse ends: (1) B1 falls while B1R is still high (i.e. not deasserted by B2 rising, which might occur, for example, if B2 misses a +ve pulse); or (2) B1 rises while B1F is still high (i.e. not deasserted by B2 falling, which might occur, for example, if B2 misses a -ve pulse).

The validation flag, v, is also asserted when the DN pulse begins. It remains asserted after the DN pulse ends if and only if the DN pulse is valid. Any one of two conditions can cause the validation flag to be deasserted before the DN pulse ends: (1) B2 falls while B2R is still HIGH (i.e. not deasserted by B1 rising, which may occur, for example, if B1 misses a +ve pulse), or (2) B2 rises while B2F is still high (i.e. not deasserted by B1 falling, which may occur, for example, if B1 misses a -ve pulse).

The output switch logic circuit 116 of the presently preferred embodiment is shown in Figure 7 to which reference is now additionally made. The output switch logic circuit 116 receives the Up and Dn output signals and the validation flag, v, of the phase comparator 112. The Up and Dn signals are inputs to a two-input NOR gate 184 which drives the clock of a D positive-edge D-type flip-flop 186 with active low clear. The validation flag, v, provides an clock enable signal to the D-type flip-flop, so that if the validation flag goes low, indicating an invalid signal, the D-type flip-flop 186 resets to switch the Q(bar) output (the ANB signal) high. The output of the flip-flop, Q(bar), provides a signal ANB on line 188. The ANB signal also provides the D input to the flip-flop 186.

The EN input is an active HIGH clock-enable input to the flip-flop 186. When EN is high, the rising edge of the CLK input of the flip-flop is allowed to clock the flip-flop, making it toggle in the present configuration. When EN is low, rising edge of the CLK input is NOT allowed to clock the flip-flop, hence keeping the present flip-flop state.

In this circuit 116 of Figure 7, the UP (or DN) pulse (positive pulses) will toggle the flip-flop 186 if V is held high across the falling edge of UP (or DN). However, if the UP (or DN) pulse is declared invalid by V becoming low prior to the falling edge of UP (or DN), then the UP falling edge will not toggle flip-flop 186.

Thus, the ANB signal toggles each time an UP (or DN) pulse ends, if and only if the validation flag is high. In other words, the ANB signal toggles upon valid UP (or DN) pulses. The toggling of the ANB signal alternates the ping-pong capacitor so that the newly charged capacitor has its capacitor voltage propagated to the output. But if the UP (or DN) pulse is not valid, the alternation is skipped, and the same capacitor which has just been charged (or discharged) will go back to being reset and prepare for the next charge/discharge. The other capacitor, which held the previous valid voltage, continues to output its voltage to the circuit output.

It should be noted that the validation flag, v, arrives at the clock enable input of the ANB flip-flop 186 before the UP or DN signal propagates to its clock input. Normally when the UP (or DN) pulse is valid, the validation flag, v, continues to be HIGH when the UP (or DN) pulse is deasserted, and hence the ANB flip-flop is clocked and toggled since the validation flag input is high. However, when the UP (or DN) pulse is detected as being invalid, then the validation flag is deasserted before the UP (or DN) pulse

is completed and deasserted. Hence the falling edge of UP (or DN) Pulse does not cause the ANB flip-flop to be clocked and toggled.

The ping-pong logic circuit 114 is shown in Figure 8 to which reference is now additionally made. The ping-pong logic circuit 114 receives the Up, Dn, and ANB signals as its inputs. Four two-input AND gates 190, 192, 194, and 196 create outputs UPA, UPB, DNA, AND DNB, respectively. The outputs are used to drive the ping-pong charge pump 122, described below. The AND gate 190 receives as input the UP and ANB signals to produce the UPA signal on its output. The AND gate 192 receives as input the Up and the complement of ANB signals to produce the UPB signal on its output. The AND gate 194 receives as input the Dn and ANB signals to produce the DNA signal on its output. And the AND gate 196 receives as input Dn and the complement of ANB signals to produce the DNB signal on its output.

In operation, if ANB is high, the ping-pong logic circuit 114 converts the UP and DN pulses into UPA and DNA pulses, which operate on charge pump capacitor CA 130, described below. On the other hand, if ANB is low, UP and DN pulses are converted into UPB and DNB pulses which operate on charge pump capacitor CB 132, also described below.

The reset logic circuit 118 is shown in Figure 9 to which reference is now additionally made. The reset logic 118 receives the ANB signal from the output switch logic circuit 116 and the validation flag, V, from the phase comparator 112. An initial set of two two-input AND gates is used to generate one of the inputs needed for the reset logic output and a second signal which will be used for the other input. The AND gate 200 receives signal ANB, and the complement thereof which has been delayed by the delay circuit 202. The output of the AND gate 200, RA', is one of the inputs to a two-input OR gate 204.

On the other hand, the AND gate 206 receives as its inputs the ANB signal, which has been delayed by one cycle at by delay circuit 202, as well as the complement of the ANB signal. The output of the AND gate 206, RB', is one of the inputs to a two-input OR gate 208. Finally, the AND gate 210 is a two-input gate which receives the validation flag signal, v, delayed one cycle by delay circuit 212 and its complement as input. Two-input AND gates 214 and 216 receive the output of the AND gate 210 as one of their inputs. The AND gate 214 receives the ANB signal as its second input, and AND gate 216 receives the complement of ANB as its second input.

The output, RA", of the AND gate 214 is the second input to OR gate 204, and the output, RB", of the AND gate 216 is the second input to the OR gate 208. The outputs of OR gates 204 and 208 (RA and RB respectively) serve as inputs to the ping-pong charge pump 122 shown in detail in Figure 10 to which reference is now additionally made.

With reference additionally now to Figure 10, the architecture of the ping-pong charge pump 122 is shown. The charge pump 122 includes a pair of capacitors CA 130 and CB 132 that alternate between a "reset-and-charge" phase and a "hold" phase. The voltage of the capacitor in the hold phase is selected as output. More particularly, the ping-pong charge pump 122 receives the UPA, UPB, DNA, and DNB signals from the ping-pong logic circuit 114 and the RA and RB signals from the reset logic 118 as input. Assertion of the UPA, UPB, DNA and DNB signals controls the respective switches 124-127 of the ping-pong charge pump 122.

The capacitors CA 130 and CB 132 provide a charge of either node VA or VB, depending on the state of signals UPA, UPB, DNA, and DNB and magnitudes of the current sources 134 and 136. The charge pump output, VA or VB, is selected from the one of the two ping-pong capacitors, CA 130 or CB 132, that holds the last valid phase difference measurement voltage.

Thus, the charge pump 122 is provides an output that is independent of the time interval that elapses between successive input pulses. The charge pump uses the RA and RB signals from the reset logic circuit 118 to discharge or reset respective ones of the capacitors 130 or 132 that has been charged by an invalid pulse and return it to the reset state to be ready for the next phase comparator output result from the phase comparator circuit 112. Consequently, the two capacitors, CA 130 and CB 132, alternate between "hold" and "reset or charge/discharge" states. While one capacitor is in the hold state, the other is reset first (by RA, for CA, or by RB, for CB) and subsequently charged/discharged.

The architecture of the output switch circuit 120 of the presently preferred embodiment is shown in Figure 11 to which reference is now additionally made. The output switch circuit 120 receives as its inputs the charges on nodes VA and VB from capacitors CA 130 and CB 132 depicted in Figure 10, as well as the ANB signal from output switch logic 116 shown in Figure 7. The ANB signal controls switches 140 and 142. When the ANB signal is high, it switches the charge of capacitor CB 132 to Cout. On the other hand, when the ANB signal is low, it switches the charge of capacitor CA 130 to Cout. Thus, if ANB is high, the voltage on capacitor CB 132 is propagated to the Cout signal. Conversely, if ANB is low, the voltage on capacitor CA 130 is propagated to the Cout signal.

In operation, with reference additionally now to Figure 12, when the signal A2 146 from detectors B and D of the detector 102 lags the signal A1 148 from the detectors A and C, indicating that the beam needs to be moved in the "up" direction, signals B2 150 and B1 152 are generated at the outputs of level comparators 110 and 108. Since the beam needs to be moved in the "up" direction, there are no DN, DNA or DNB outputs, as shown, but there are a

series of UP pulses 154 generated, the width of which representing the magnitude of the location error of the sensor.

The ping-pong logic circuit generates the UPA 158 and UPB 156 signals from the UP, DN and ANB signals, as shown. At the same time, the ANB signal 160 is generated by the output switch logic circuit 116, and changes state upon the falling edge of the first UP signal 154, and again on the third falling edge of the UP signal. It is noted that since the validation signal is low during the falling edge of the second UP signal pulses, the ANB signal 160 remains in its high state until the falling edge of the third UP signal.

As a result, the charge 164 on the capacitor CB 132 is allowed to charge during the UP pulse 154, and the concomitant UPB pulse 156, which corresponds to the time that the A1 pulse is positive and A2 is negative, to a value determined by the width of the first UPB pulse. This value is maintained until it is reset to Vref by the falling edge of the ANB signal. Upon the occurrence of the next subsequent UPB pulse, the charge on capacitor CB 132 again charges to a value dependent upon the width of the UPB pulse. This process is repeated with each repetition of the UPB signal.

At the same time, the charge 166 on the capacitor CA 130 is first reset to Vref, but charges during the second UP pulse, and UPA pulse, which corresponds to the time that the A1 pulse is negative and A2 is positive, to a value determined by the width of the first UPA pulse. This process is repeated with each repetition of the UPA signal.

The values charged on both capacitors CB 132 and CA 130 are reset to the Vref value by the reset pulses 168 and 170, respectively. The reset logic 118, in response to the ANB 160 and validity 162 signals, generates the reset pulses 168 and 170.

The output signal 172, which is dependent upon the selection by the output switch 120 of the charge on one of the capacitors 130

or 132, presents on the output the voltage VA or VB, respectively. Since the ANB signal is inverted in the output circuit from the state of the ANB signal of the ping-pong logic circuit 114, the output signal 172 is produced only during the time that the capacitors produce relatively steady-state output signals, rather than during their respective charge and reset cycles. Consequently, the variations in voltage of the Cout signal 172 are relatively minor, and can be effectively removed by the low pass filter 124 to produce the tracking error signal 126.

Although the invention has been described and illustrated with a certain degree of particularity, it is understood that the present disclosure has been made only by way of example, and that numerous changes in the combination and arrangement of parts can be resorted to by those skilled in the art without departing from the spirit and scope of the invention, as hereinafter claimed.

CLAIMS

1. A method generating a tracking error signal representing a location of a data sensor of a digital versatile disc, comprising:

generating pulse signals of width proportional to a tracking error of said data sensor;

charging respective first and second capacitors to respective charge values proportional to said pulse signal widths;

and alternately switching said capacitor charge values to an output to produce a tracking error signal.

2. The method of claim 1 further comprising filtering said tracking error signal to produce a filtered tracking error signal.

3. The method of claim 1 wherein said step of charging respective first and second capacitors comprises storing charges on capacitors of a ping-pong charge pump.

4. The method of claim 3 further comprising selecting an output of said charge pump from a capacitor of said ping-pong charge pump holding a last valid phase difference measurement voltage.

5. The method of claim 1 further comprising producing a validation flag signal when said pulse signals have an improper configuration.

6. The method of claim 5 further comprising establishing a reference voltage on said capacitors when said validation flag signal is asserted.

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7. The method of claim 5 wherein a capacitor not holding a last valid phase difference measurement voltage is used for a new phase difference measurement voltage.

8. A method generating a tracking error signal representing a location of a data sensor of a digital versatile disc, comprising:

receiving respective signals at least first and second portions of a photodetector array, said signals having phases representing a relative sensor location with respect to a desired track to be followed;

converting said signals to differential phase difference indicating signals of width dependent upon a location error of said sensor;

storing charges on respective first and second capacitors of magnitude proportional to said differential phase difference indicating signals;

and alternately switching the stored charges on said capacitors to an output to produce a tracking error signal.

9. The method of claim 8 further comprising filtering said tracking error signal to produce a filtered tracking error signal.

10. The method of claim 8 wherein said step of storing charges on respective first and second capacitors of magnitude proportional to said differential phase difference indicating signals comprises storing charges on capacitors of a ping-pong charge pump.

11. The method of claim 10 wherein an output of said charge pump is selected from a capacitor holding a last valid phase difference measurement voltage.

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12. The method of claim 8 further comprising producing a validation flag signal for determining whether the charge on an unconnected one of said capacitors should be allowed to be connected to the output.

13. The method of claim 12 further comprising, if said validation signal changes state, resetting unconnected one of said capacitors, skipping said alternately switching the stored charges on said capacitor to an output, and recharging said unconnected one of said capacitors.

14. The method of claim 12 wherein a capacitor not holding a last valid phase difference measurement voltage is used for a new phase difference measurement voltage.

15. A circuit for generating a tracking error signal representing a location of a data sensor of a digital versatile disc, comprising:

a pulse signal generator for producing pulses of width proportional to a tracking error of said data sensor;

first and second capacitors connected to respective charge values proportional to said widths of said pulse signal;

and a switch for alternately switching said capacitor charge values to an output to produce a tracking error signal.

16. The circuit of claim 15 further comprising a filter for filtering said tracking error signal to produce a filtered tracking error signal.

17. The circuit of claim 15 wherein said first and second capacitors are comprised in a ping-pong charge pump.

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18. The circuit of claim 17 further comprising a circuit to select an output of said charge pump from a capacitor holding a last valid phase difference measurement voltage.

19. The circuit of claim 15 further comprising a circuit to produce a validation flag signal when said pulse signals have an improper configuration.

20. The circuit of claim 19 further comprising a circuit to establish a reference voltage on said capacitors when said validation flag signal is asserted.

21. The circuit of claim 19 further comprising a circuit to use a capacitor not holding a last valid phase difference measurement voltage for a new phase difference measurement voltage.

