REPLACEMENT SHEET

- 9 MAY 2006

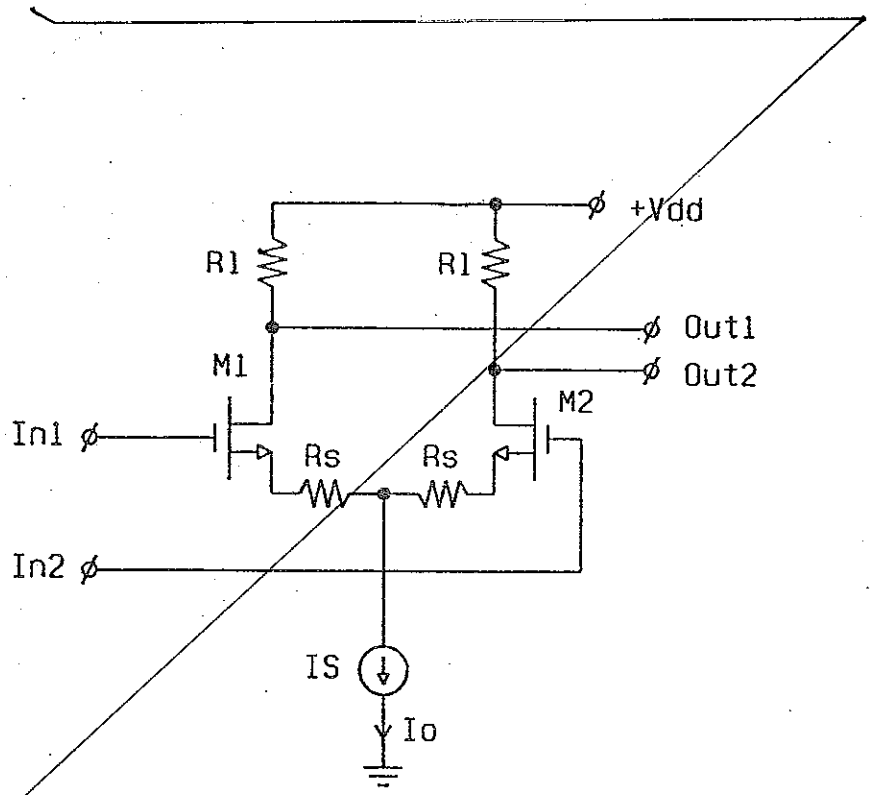


FIG. 1 — Prior Art

REPLACEMENT SHEET

- 9 MAY 2006

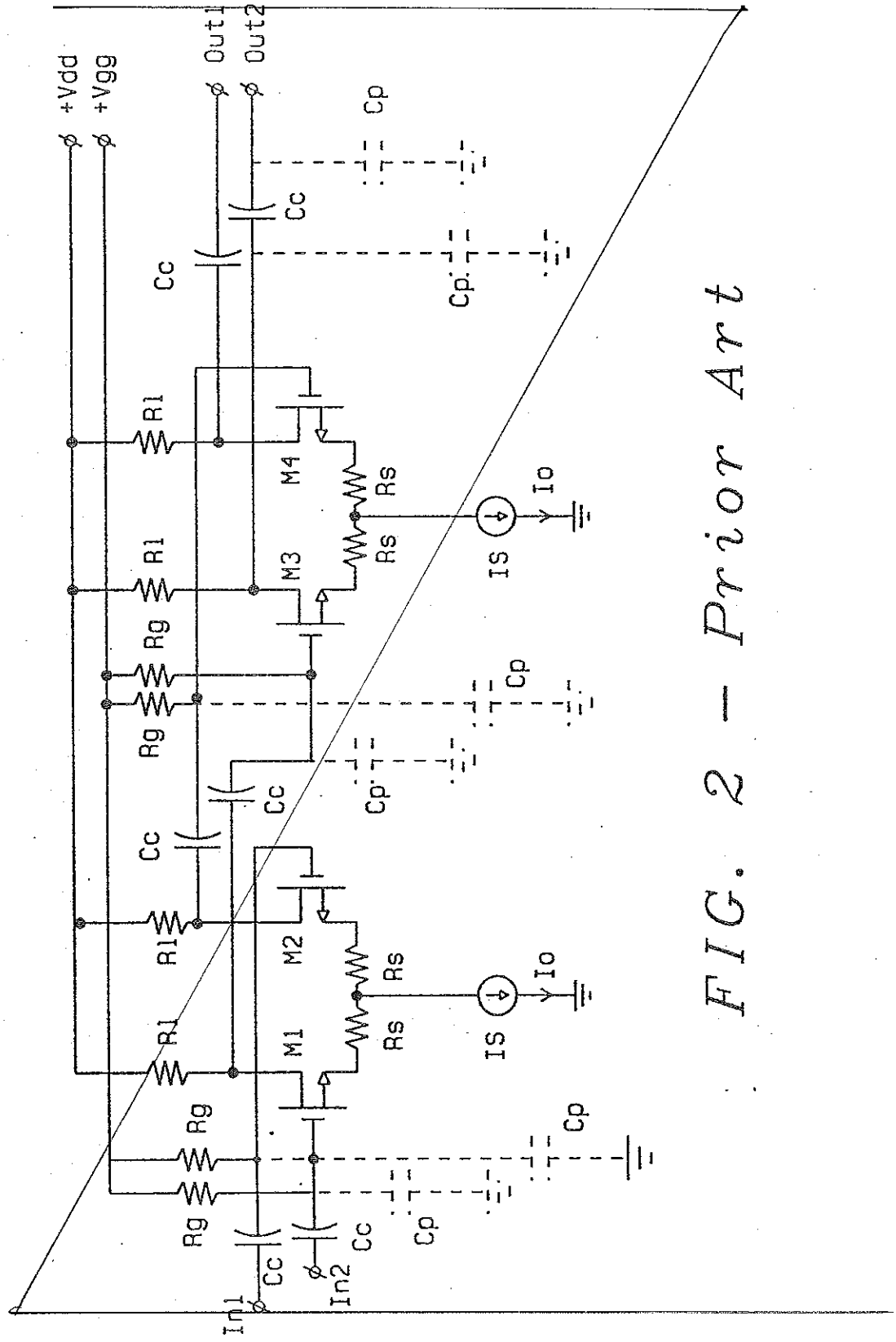


FIG. 2 - Prior Art

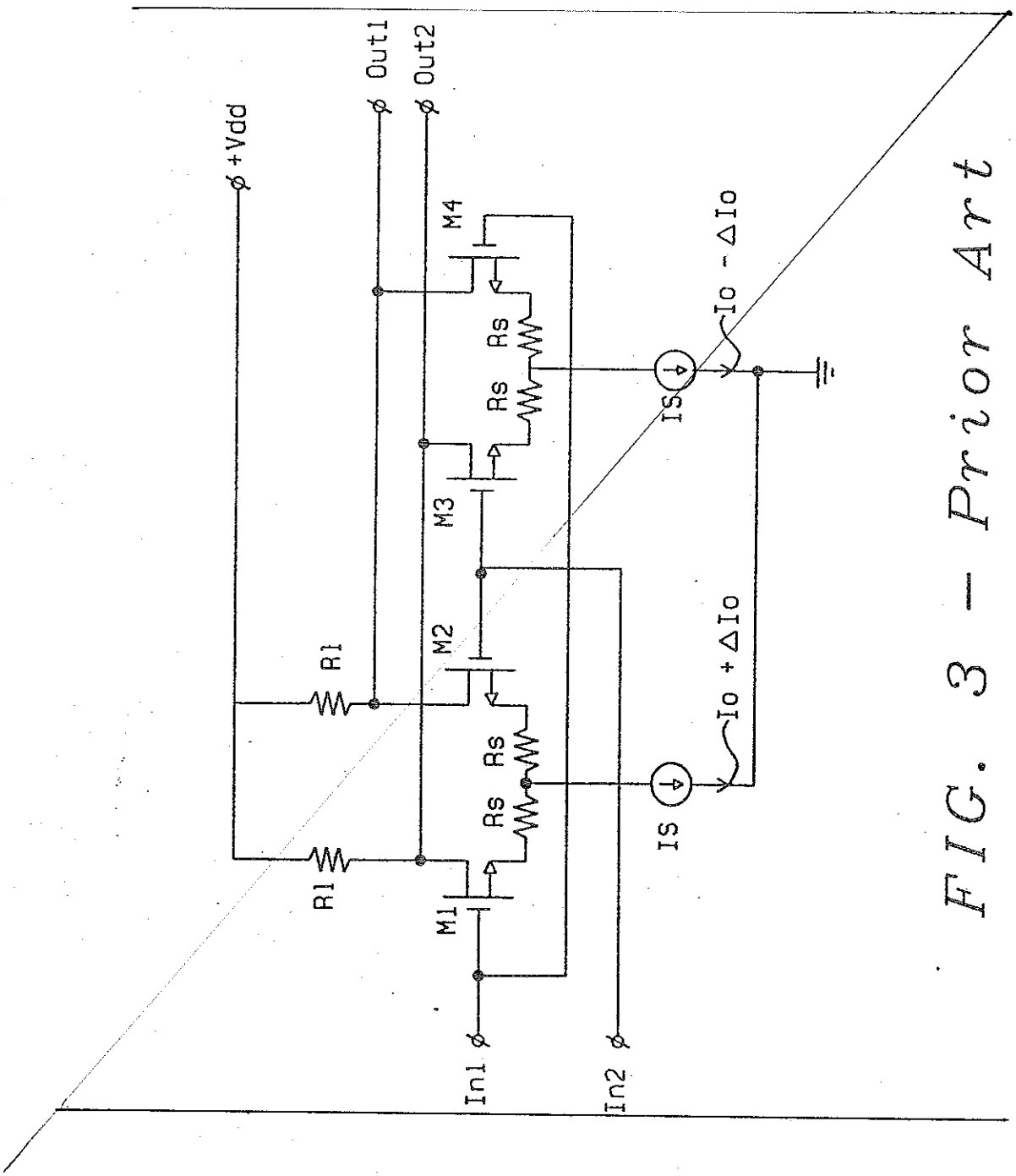


FIG. 3 – Prior Art

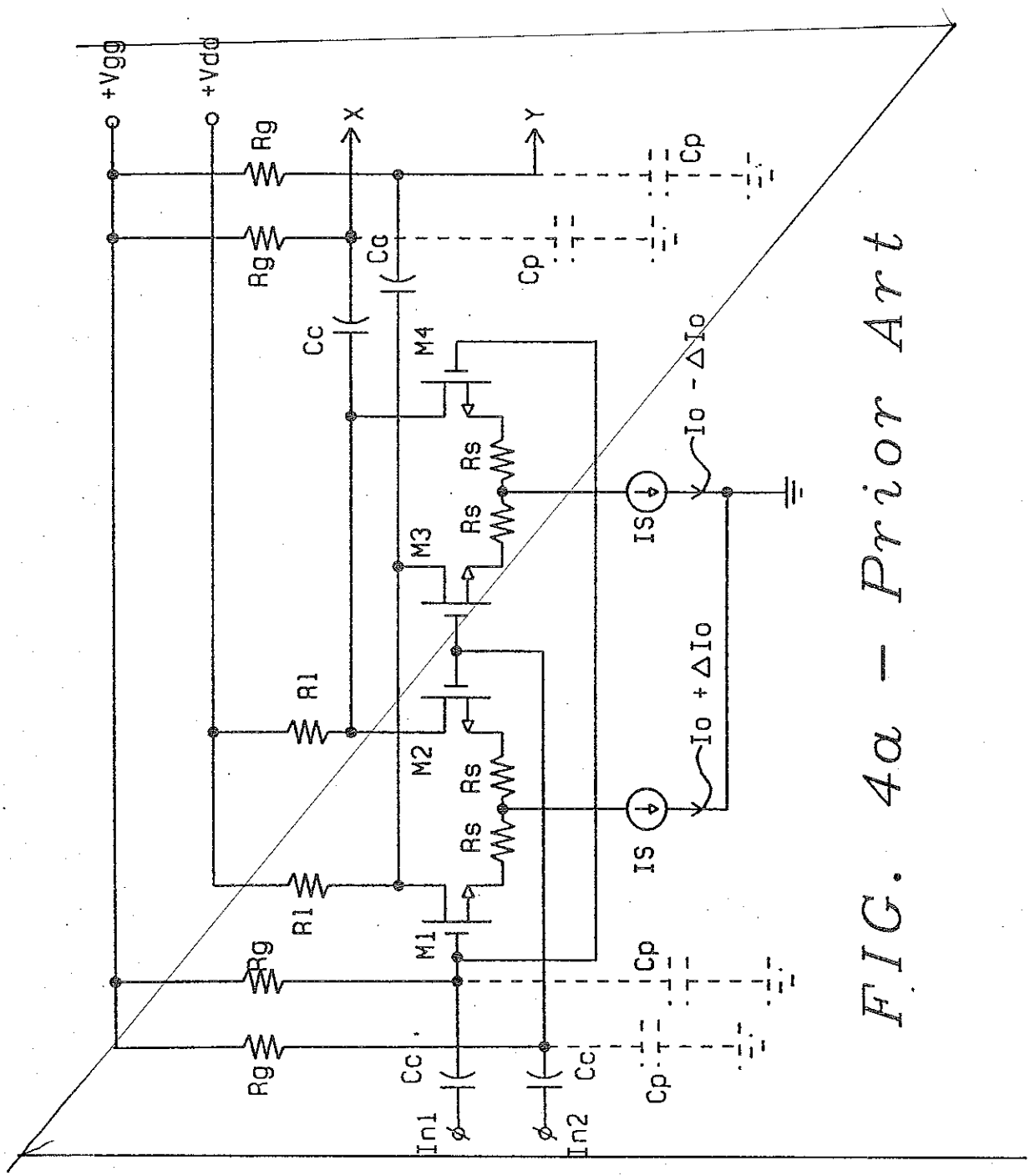


FIG. 4a – Prior Art

REPLACEMENT SHEET

- 9 MAY 2006

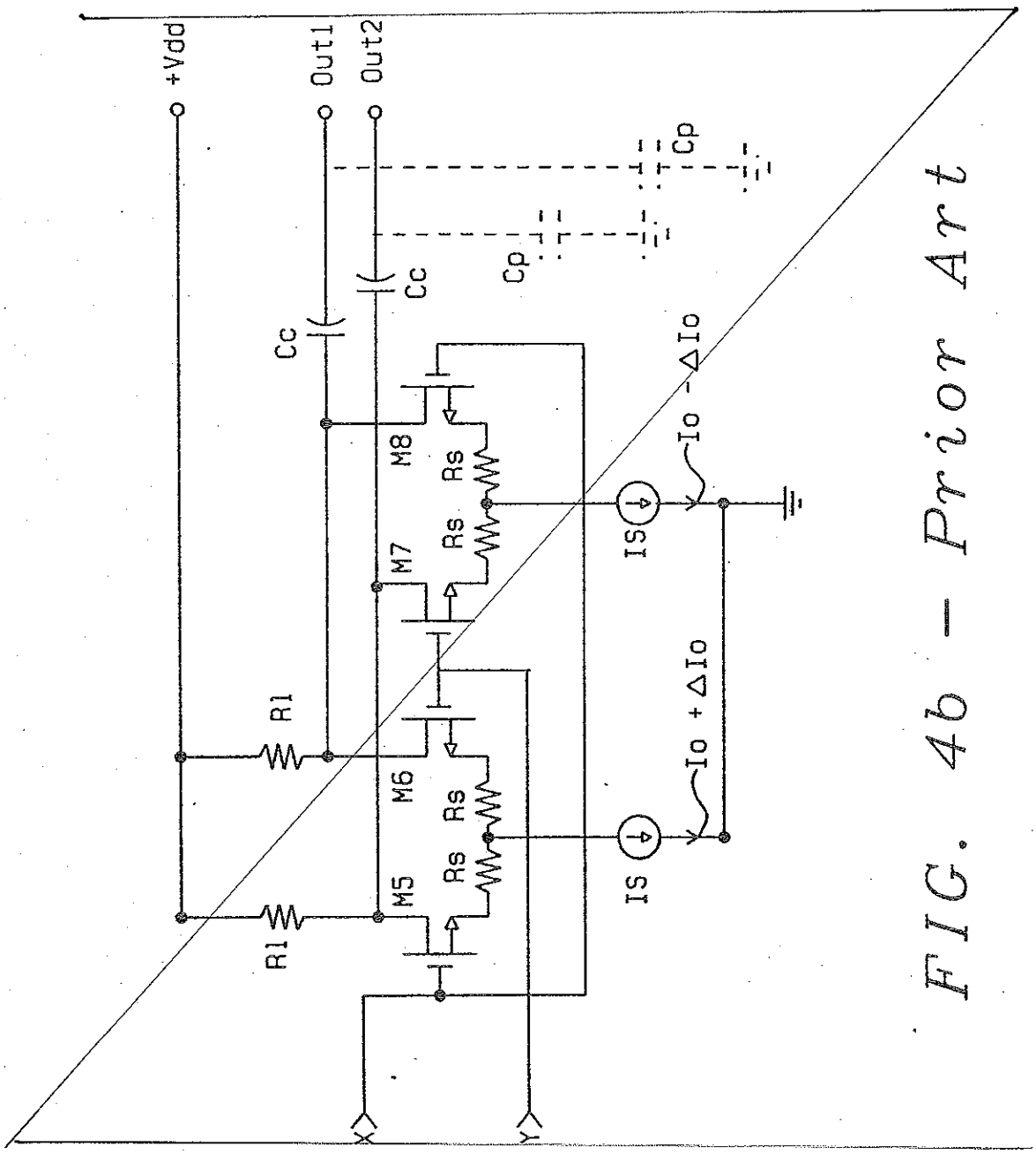


FIG. 4b – Prior Art

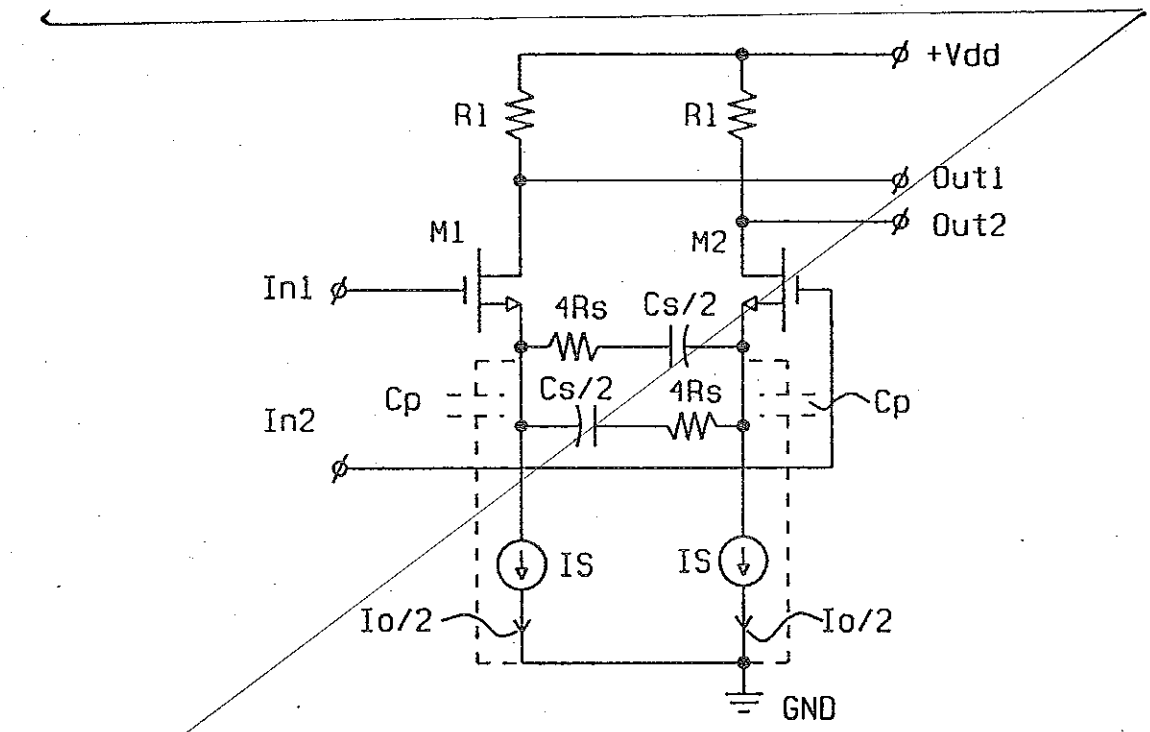

+Vdd
Rl
Rl
Out1
Out2
M1
M2
In1
4Rs
Cs/2
Cp
Cs/2
4Rs
Cp
In2
IS
IS
Io/2
Io/2
GND

FIG. 5

REPLACEMENT SHEET

- 9 MAY 2006

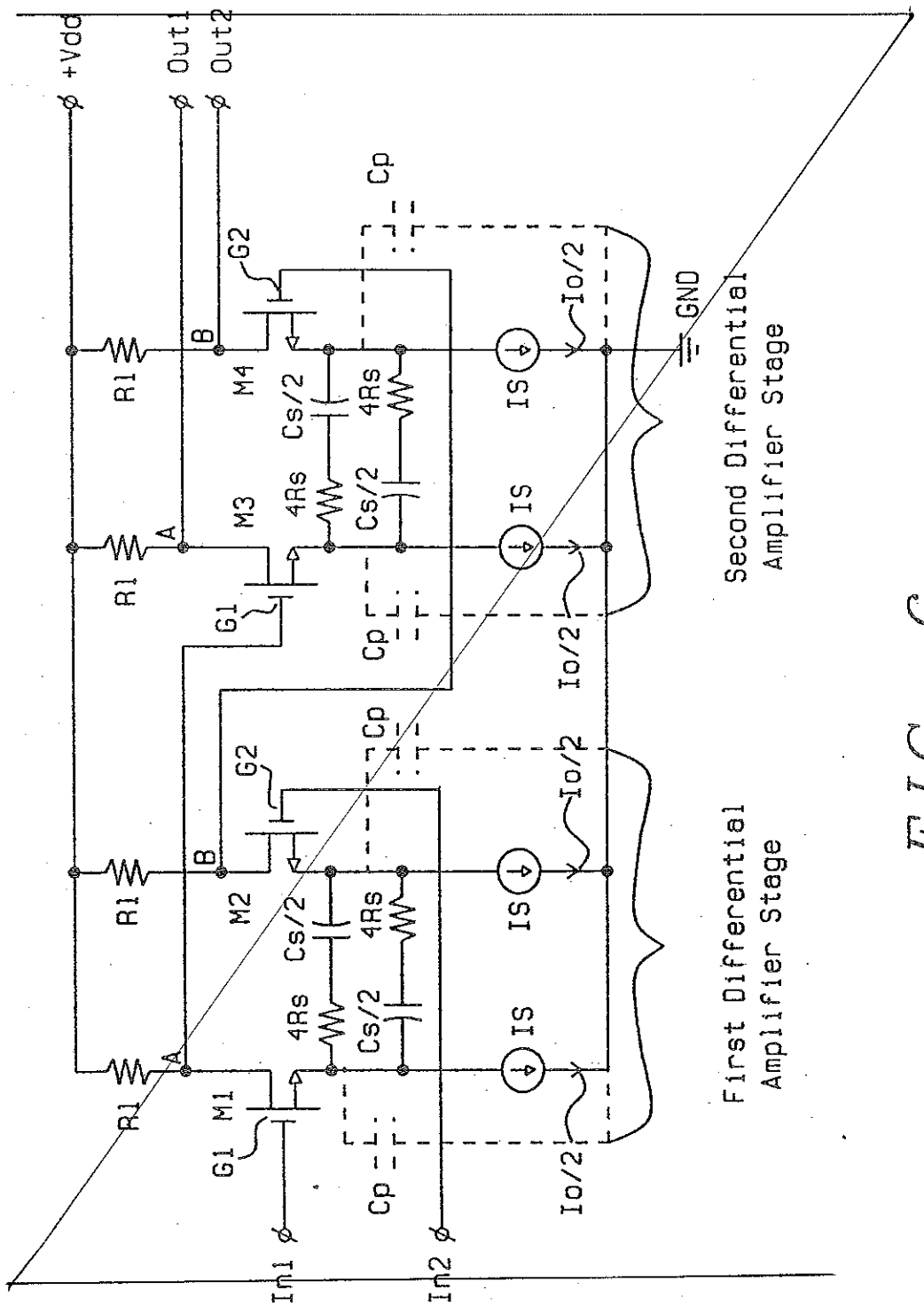


FIG. 6

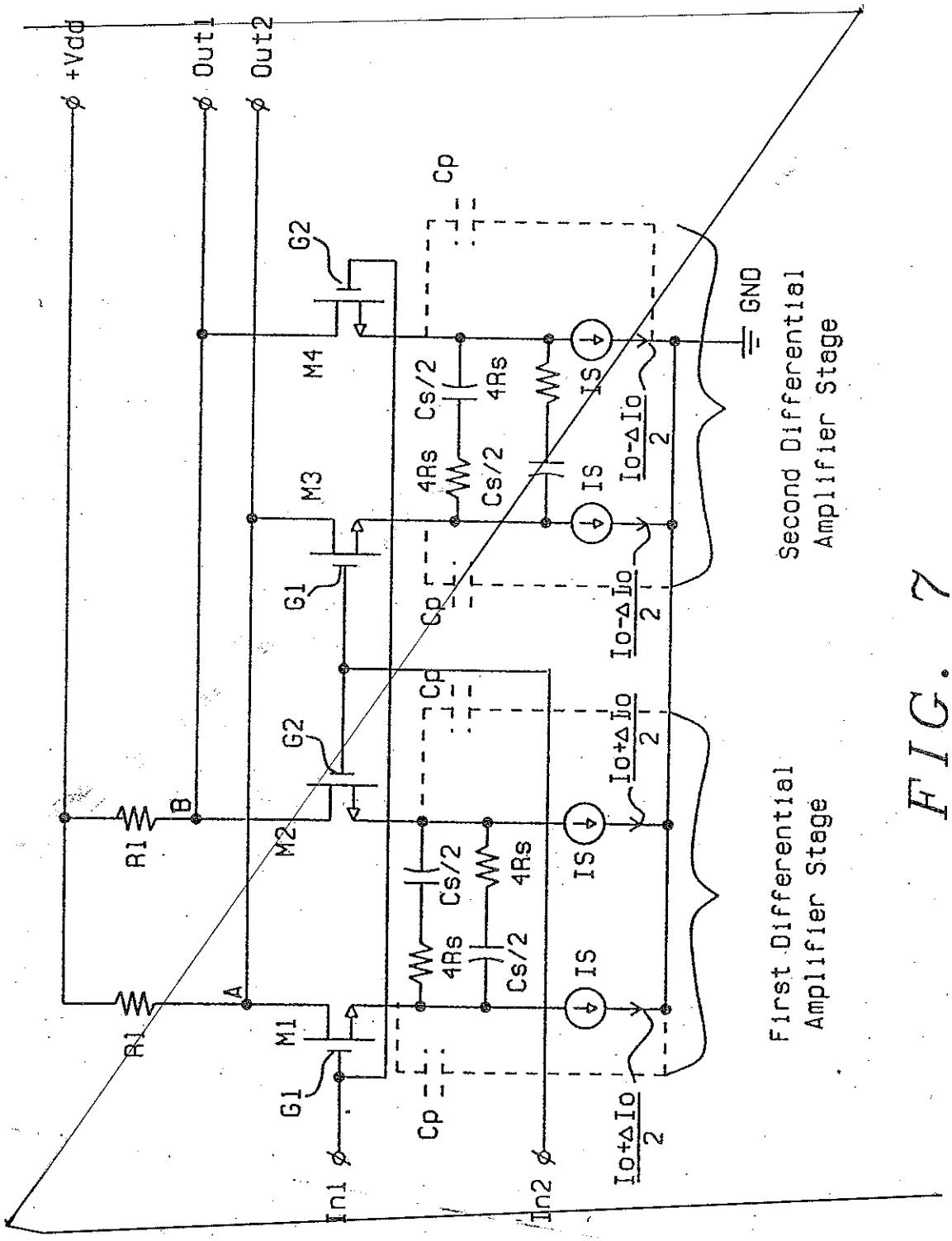

+Vdd
Out1
Out2
GND
M1
M2
M3
M4
G1
G2
R1
A
B
Cp
Cs/2
4Rs
IS
Io-ΔIo/2
Io+ΔIo/2
In1
In2
First Differential Amplifier Stage
Second Differential Amplifier Stage

FIG. 7

REPLACEMENT SHEET

- 9 MAY 2006

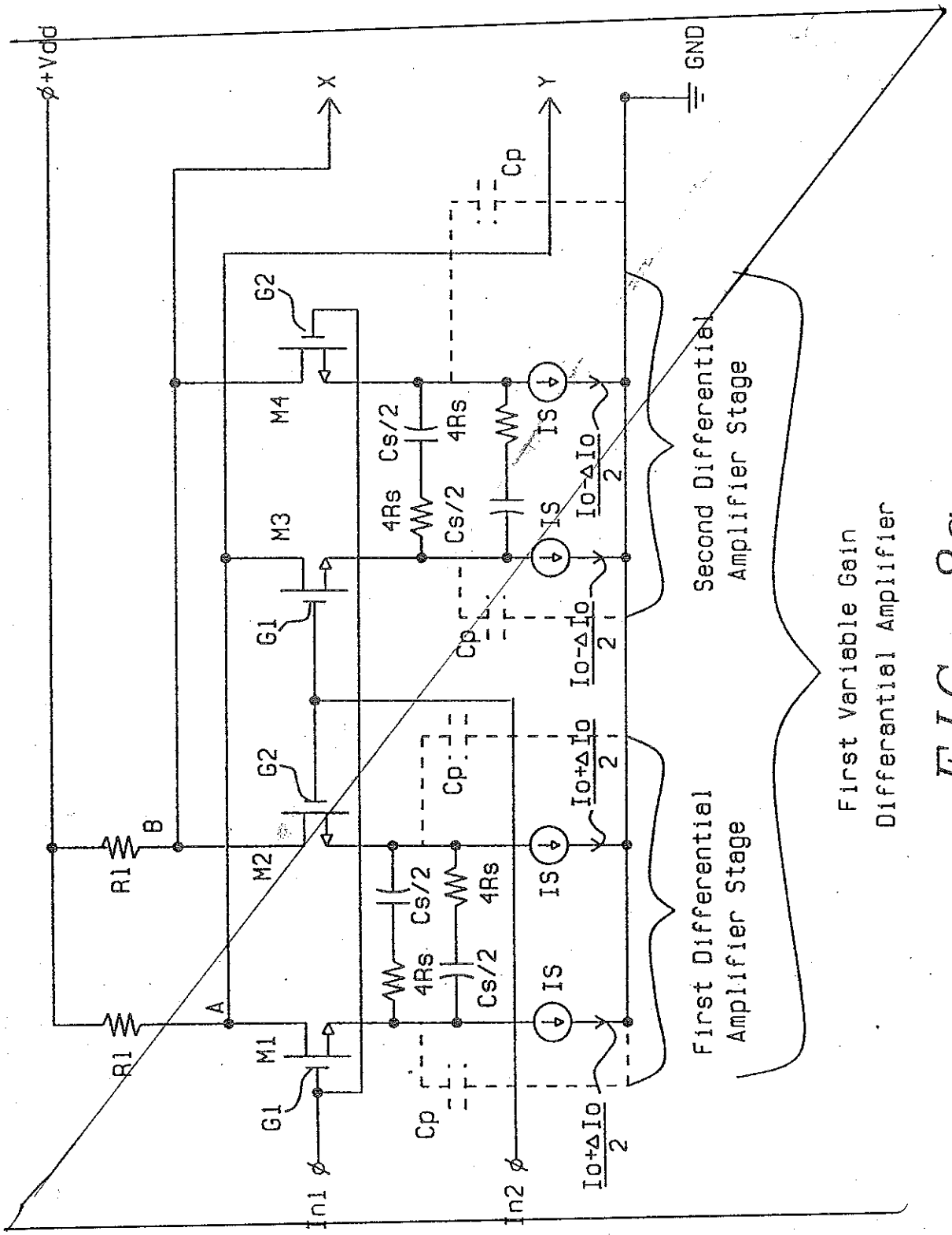


FIG. 8α

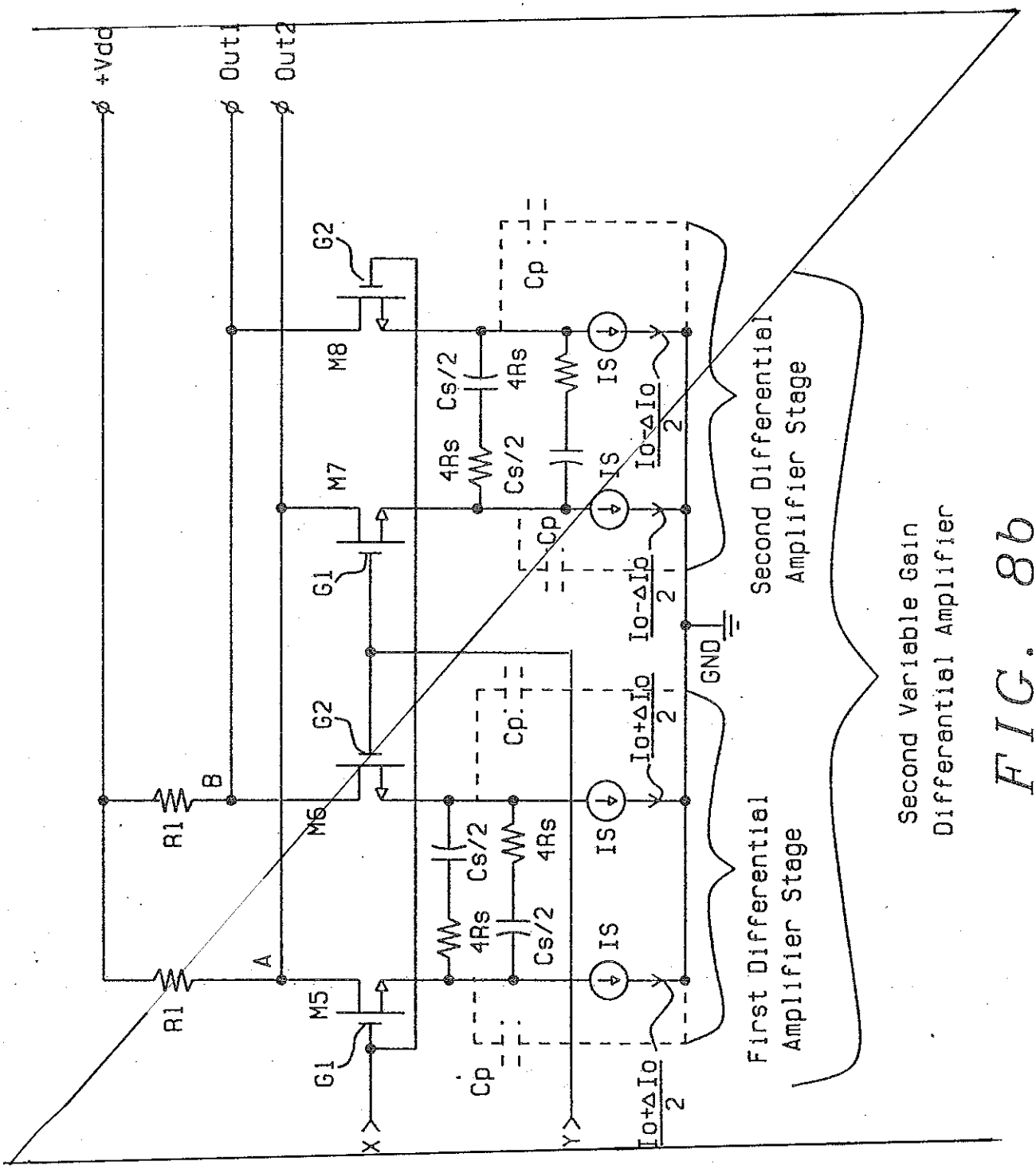

+Vdd
Out1
Out2
M8
M7
M6
M5
G2
G1
R1
A
B
X
Y
Cp
Cs/2
4Rs
IS
GND
Io+ΔIo/2
Io-ΔIo/2
First Differential Amplifier Stage
Second Differential Amplifier Stage
Second Variable Gain Differential Amplifier

FIG. 8b

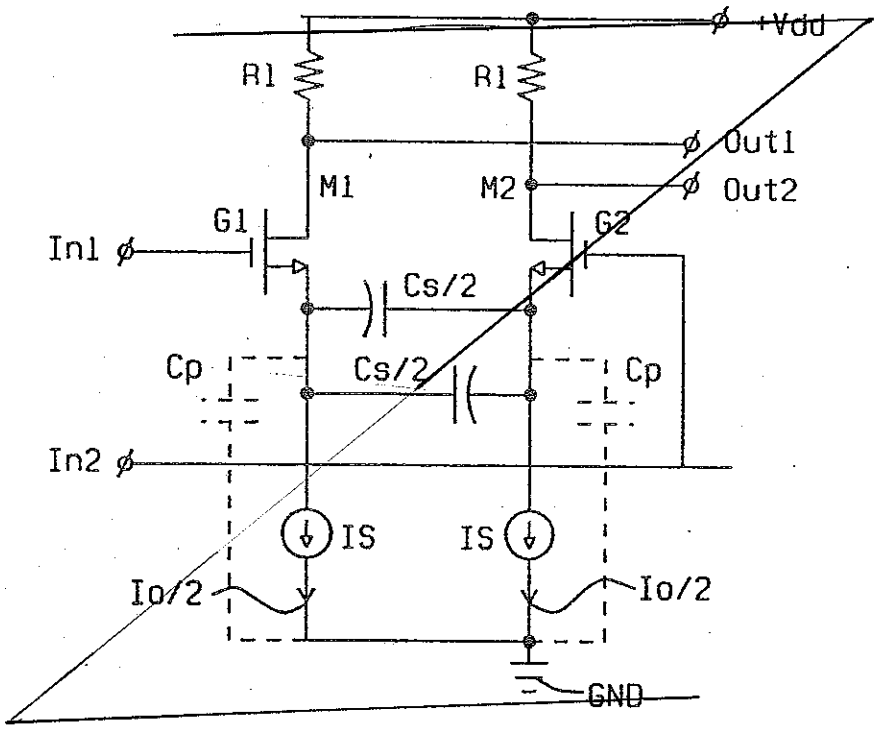

+Vdd
R1
R1
Out1
Out2
M1
M2
G1
G2
In1
Cs/2
Cp
Cs/2
Cp
In2
IS
IS
Io/2
Io/2
GND

FIG. 9

REPLACEMENT SHEET

9 MAY 2006

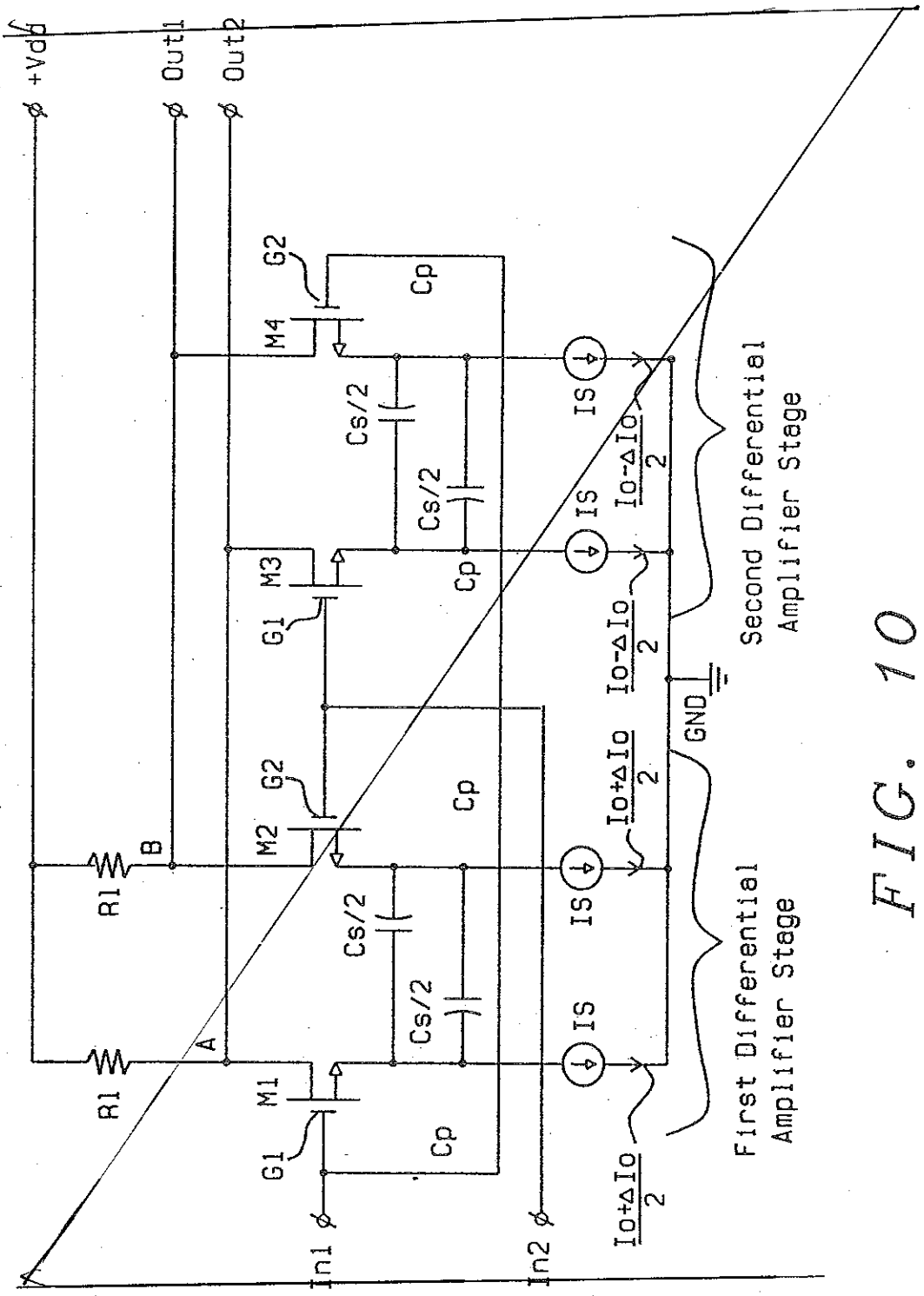


FIG. 10

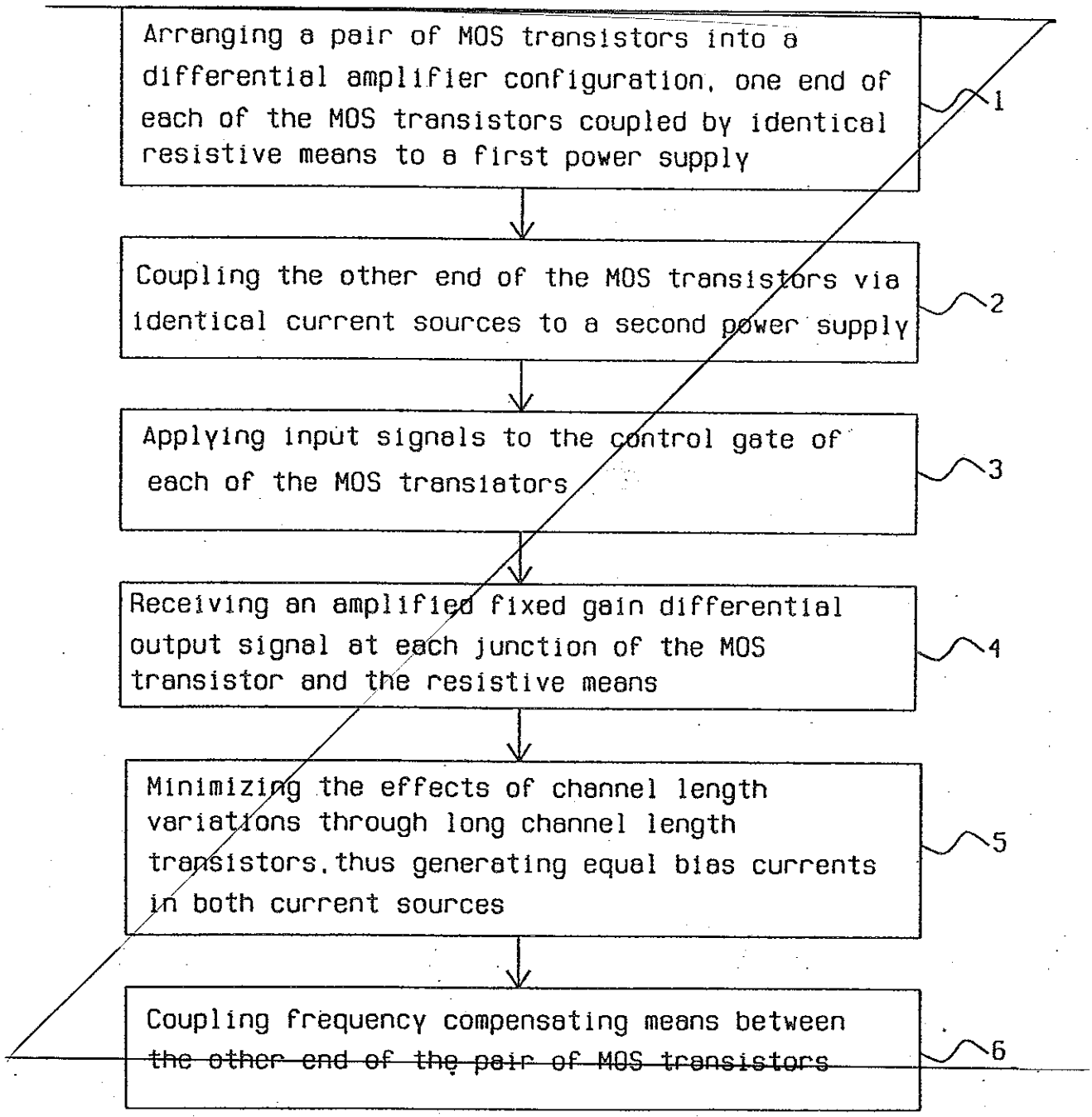

Arranging a pair of MOS transistors into a differential amplifier configuration, one end of each of the MOS transistors coupled by identical resistive means to a first power supply
1
Coupling the other end of the MOS transistors via identical current sources to a second power supply
2
Applying input signals to the control gate of each of the MOS transiators
3
Receiving an amplified fixed gain differential output signal at each junction of the MOS transistor and the resistive means
4
Minimizing the effects of channel length variations through long channel length transistors, thus generating equal bias currents in both current sources
5
Coupling frequency compensating means between the other end of the pair of MOS transistors
6

FIG. 11

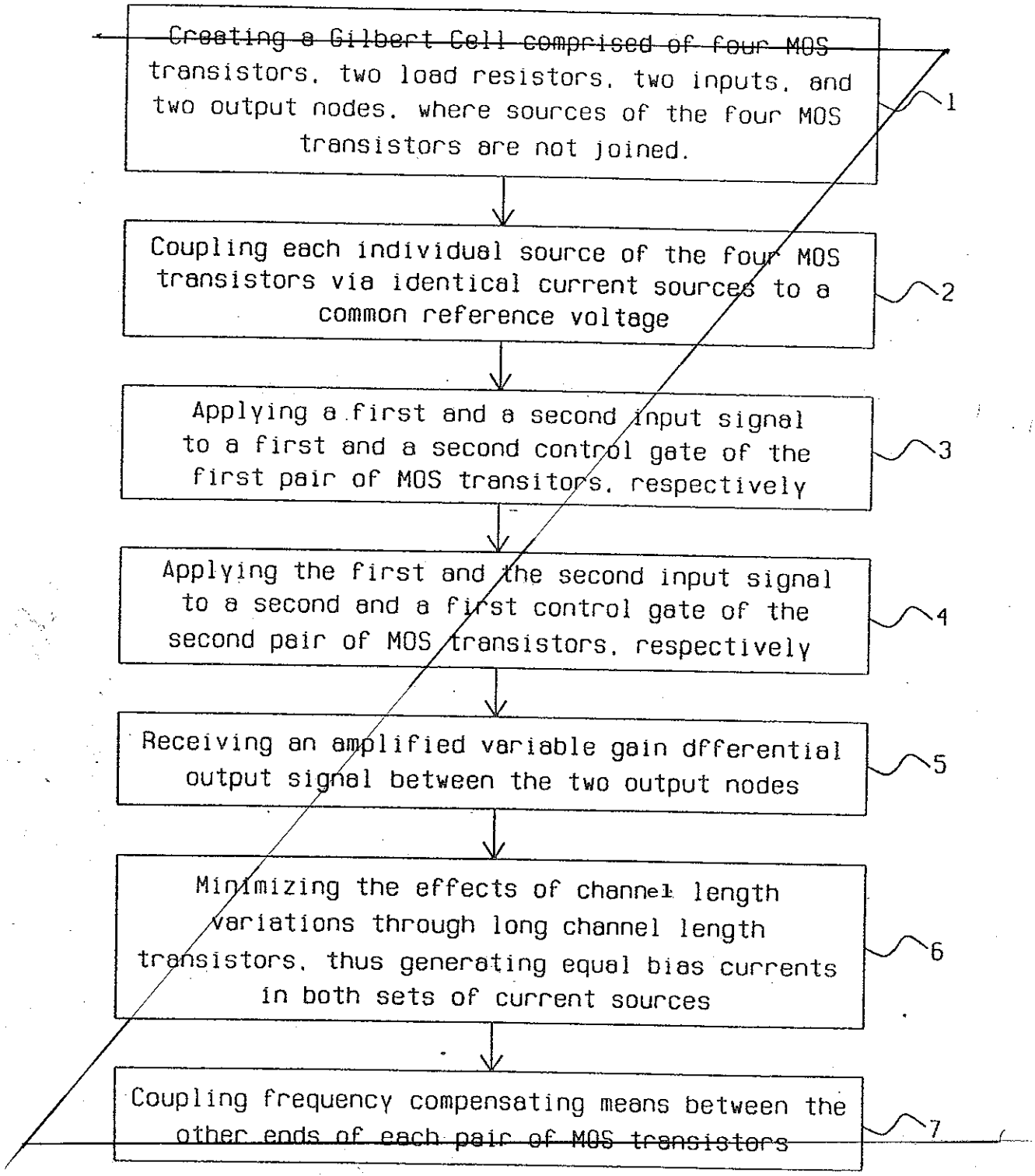

Creating a Gilbert Cell comprised of four MOS transistors, two load resistors, two inputs, and two output nodes, where sources of the four MOS transistors are not joined.
1
Coupling each individual source of the four MOS transistors via identical current sources to a common reference voltage
2
Applying a first and a second input signal to a first and a second control gate of the first pair of MOS transitors, respectively
3
Applying the first and the second input signal to a second and a first control gate of the second pair of MOS transistors, respectively
4
Receiving an amplified variable gain dfferential output signal between the two output nodes
5
Minimizing the effects of channel length variations through long channel length transistors, thus generating equal bias currents in both sets of current sources
6
Coupling frequency compensating means between the other ends of each pair of MOS transistors
7

FIG. 12

REPLACEMENT SHEET

- 9 MAY 2006

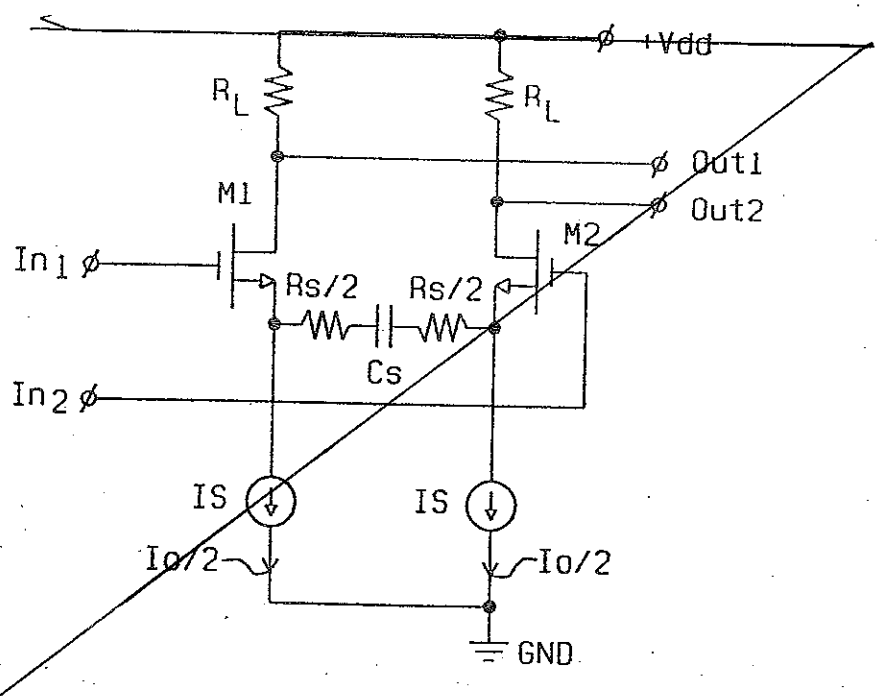


FIG. 13

REPLACEMENT SHEET

9 MAY 2006

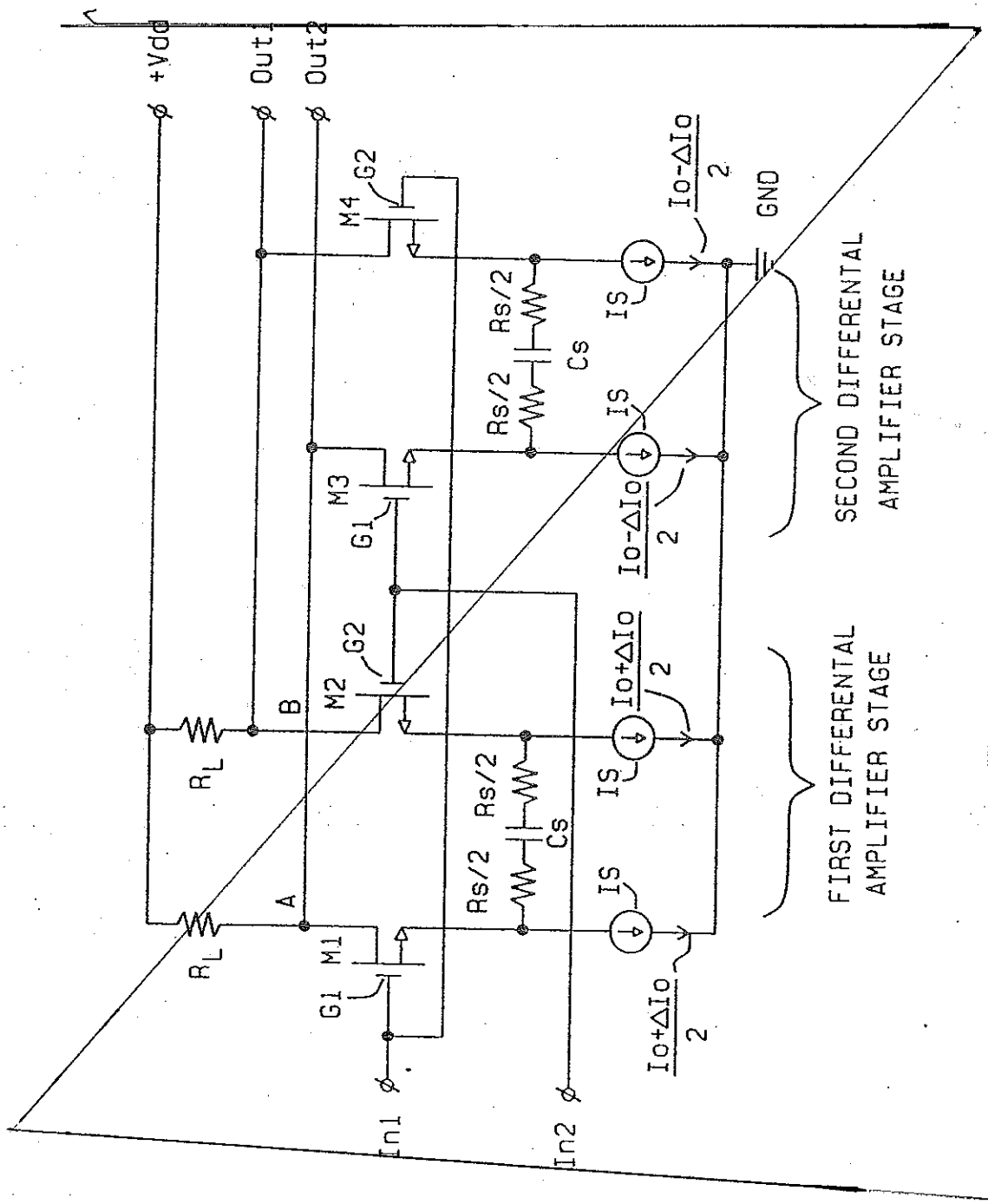


FIG. 14

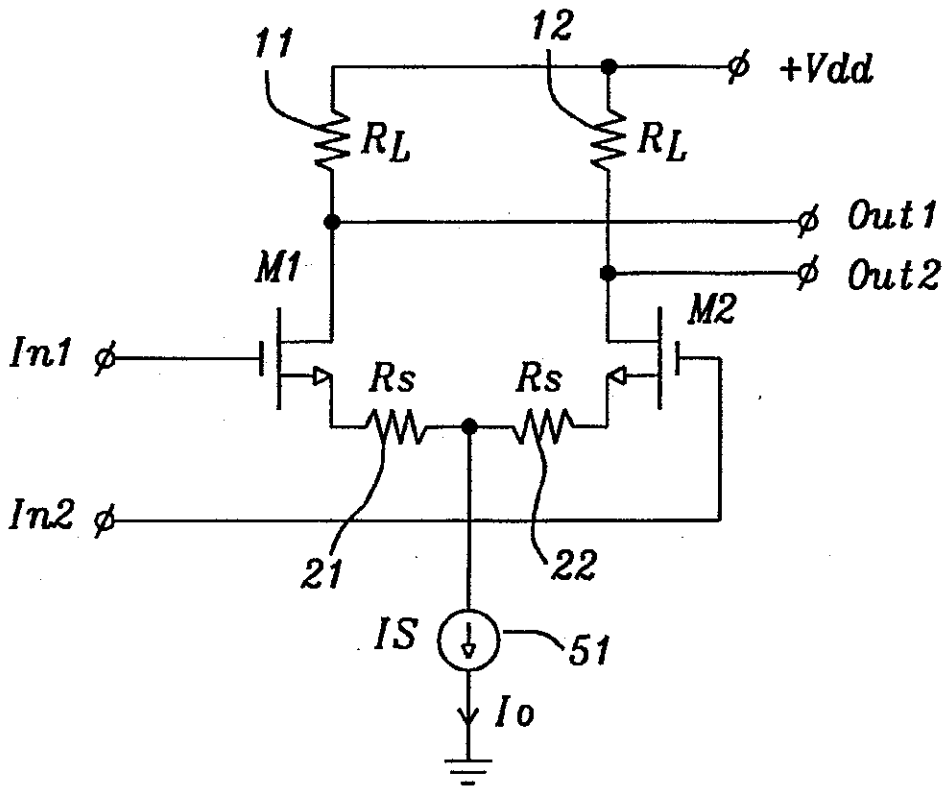


FIG. 1 – Prior Art

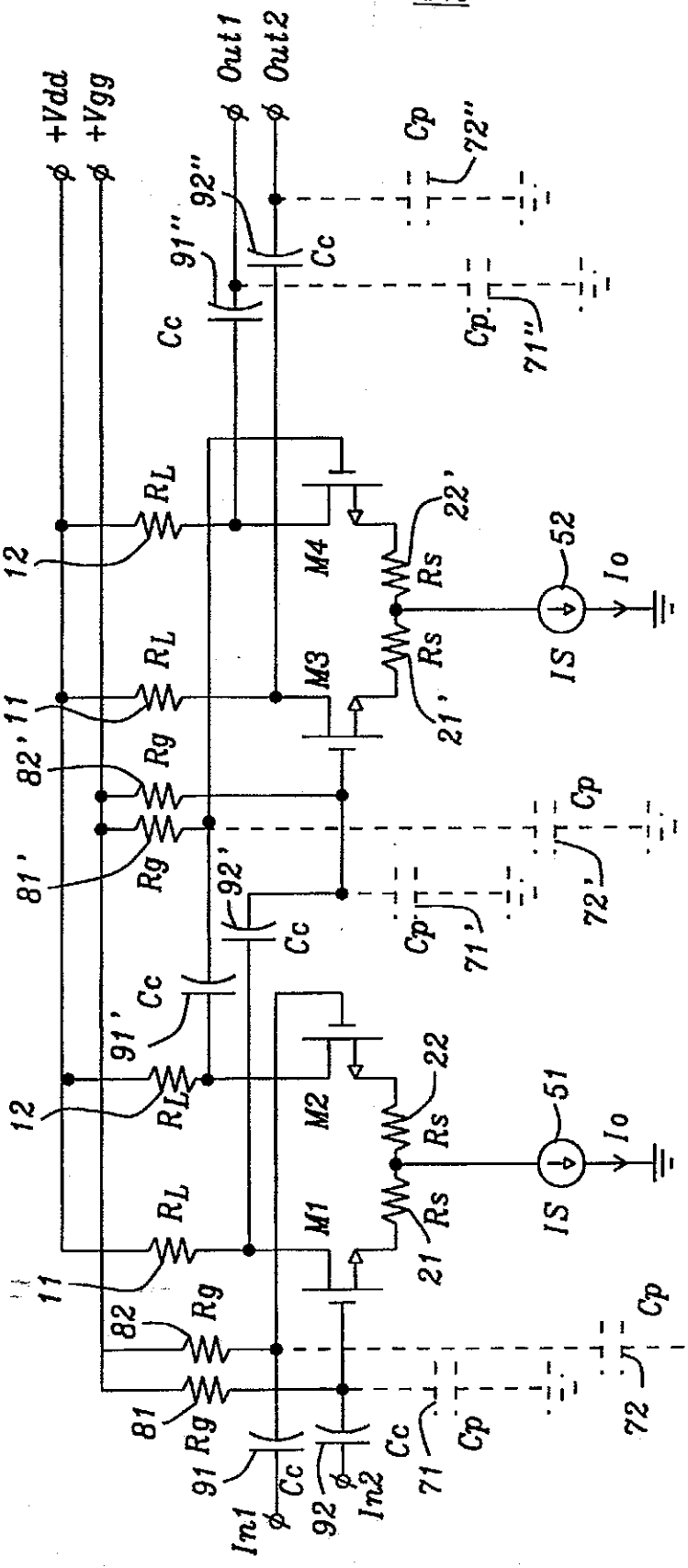


FIG. 2 – Prior Art

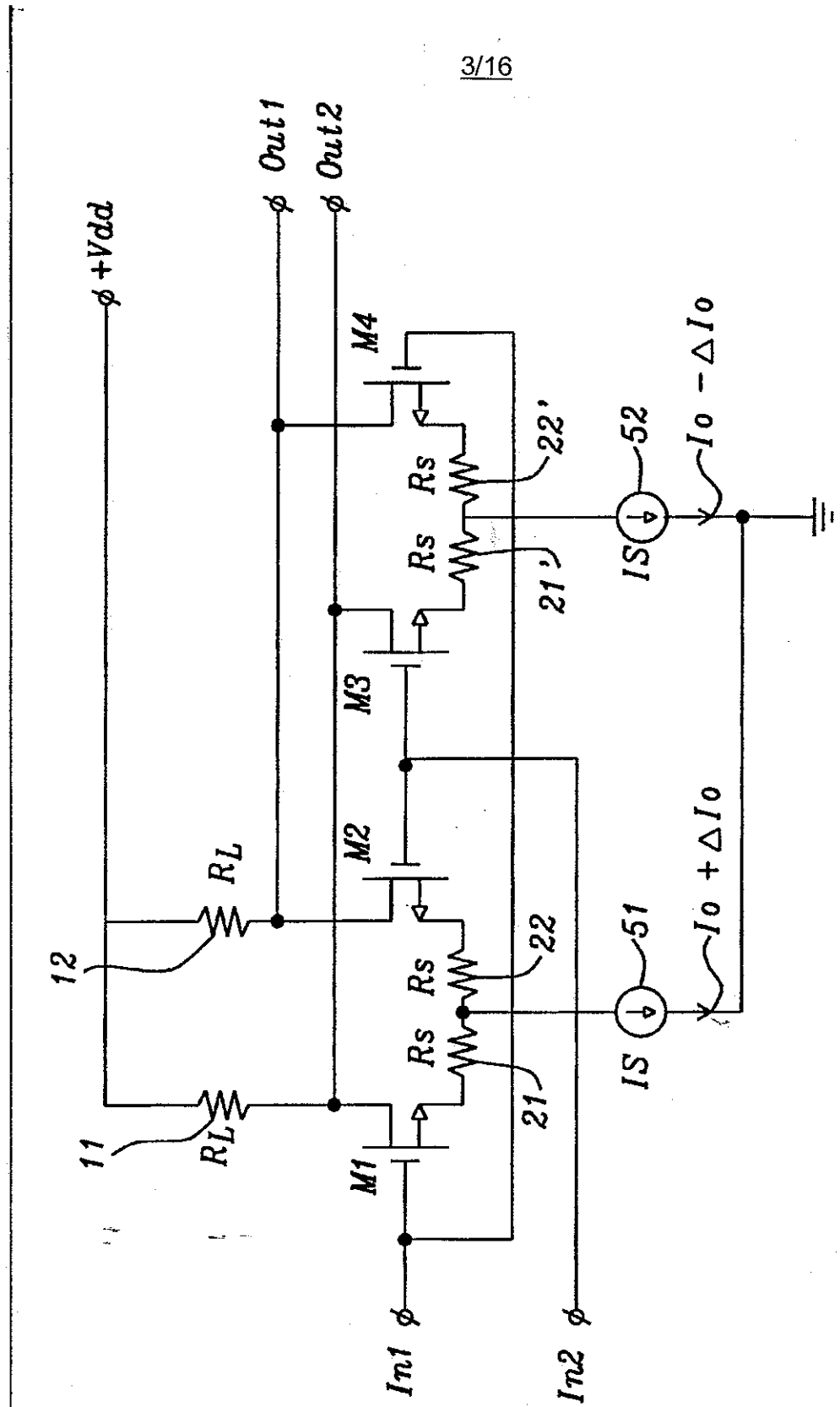


FIG. 3 - Prior Art

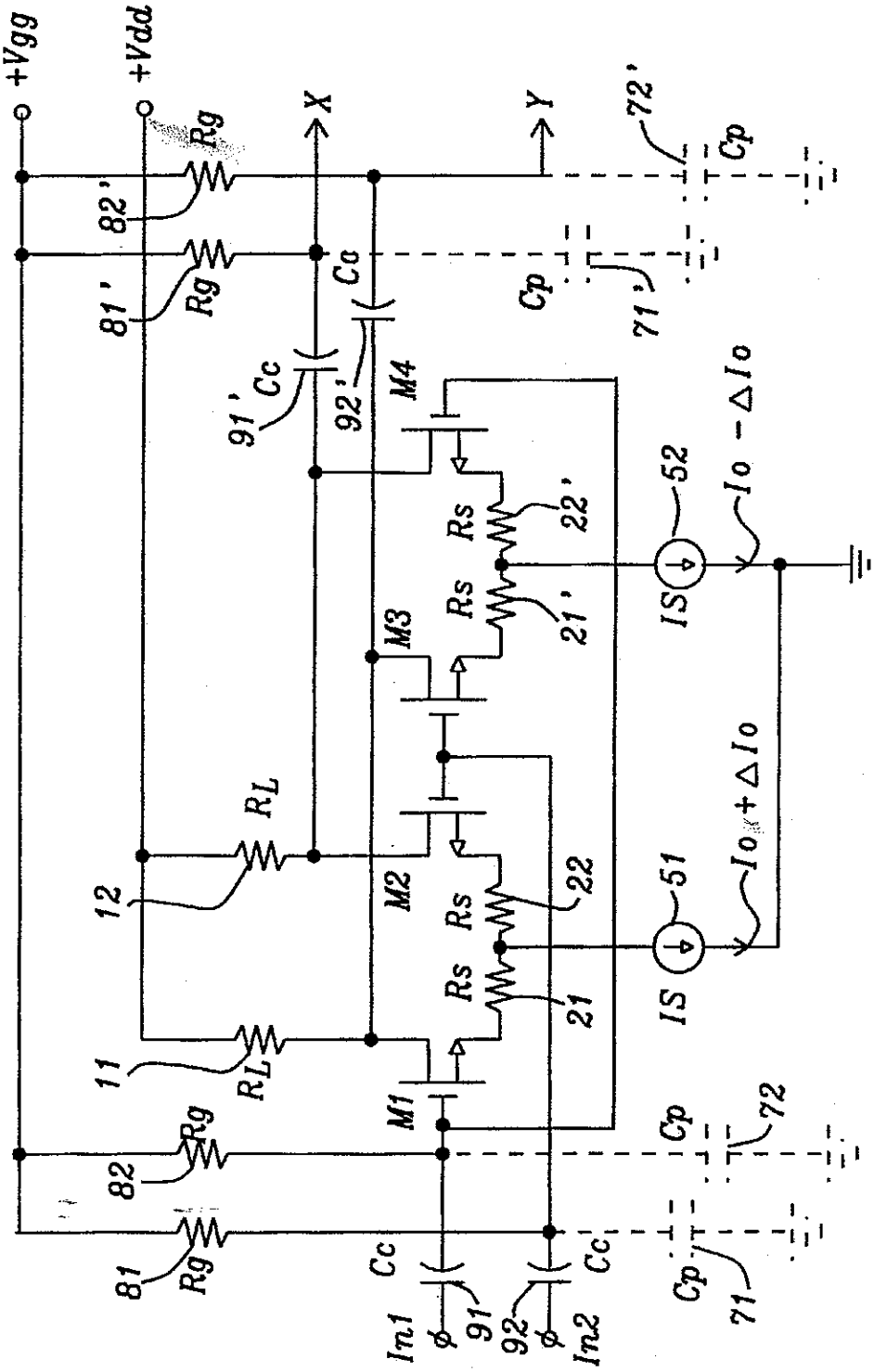


FIG. 4a - Prior Art

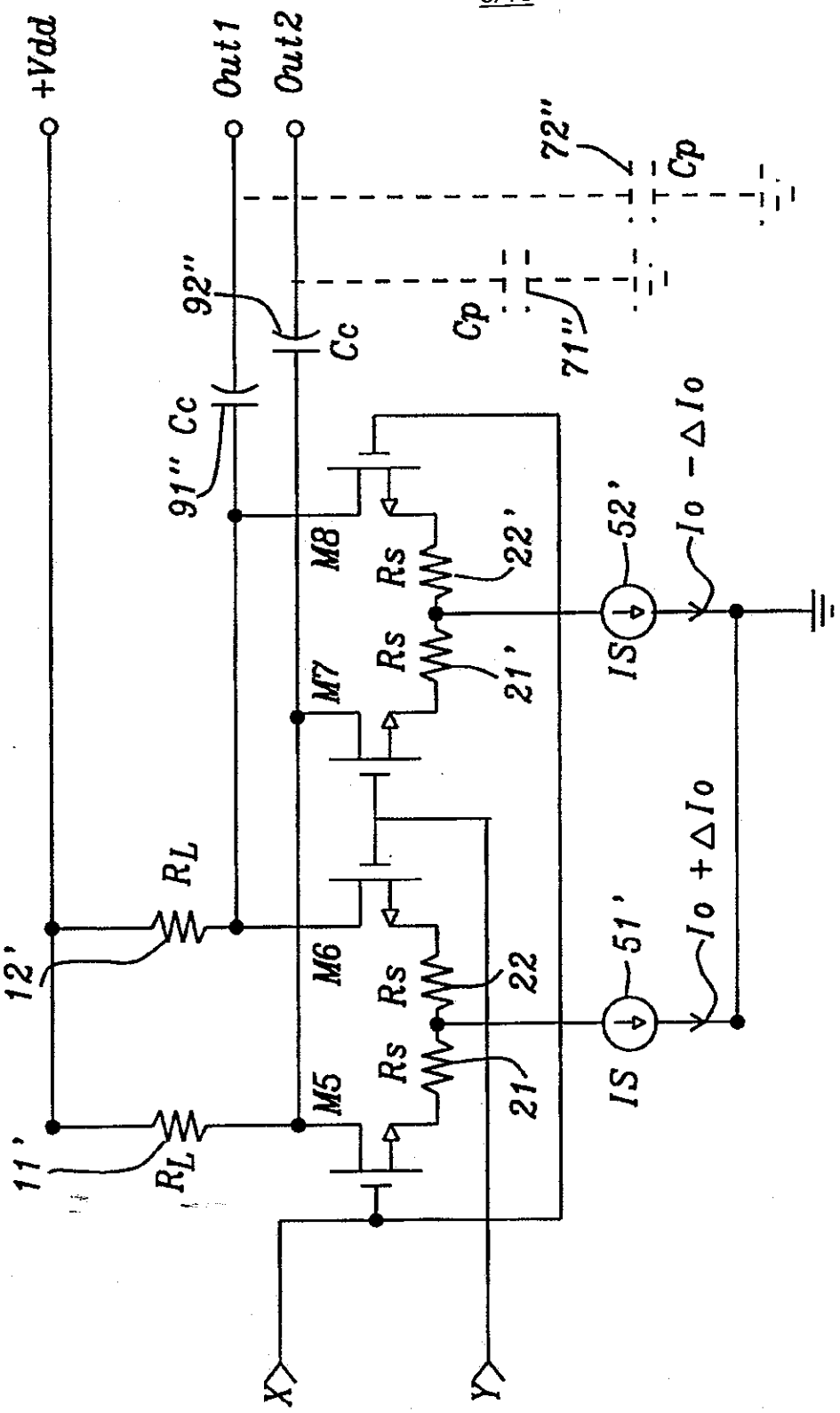


FIG. 4b - Prior Art

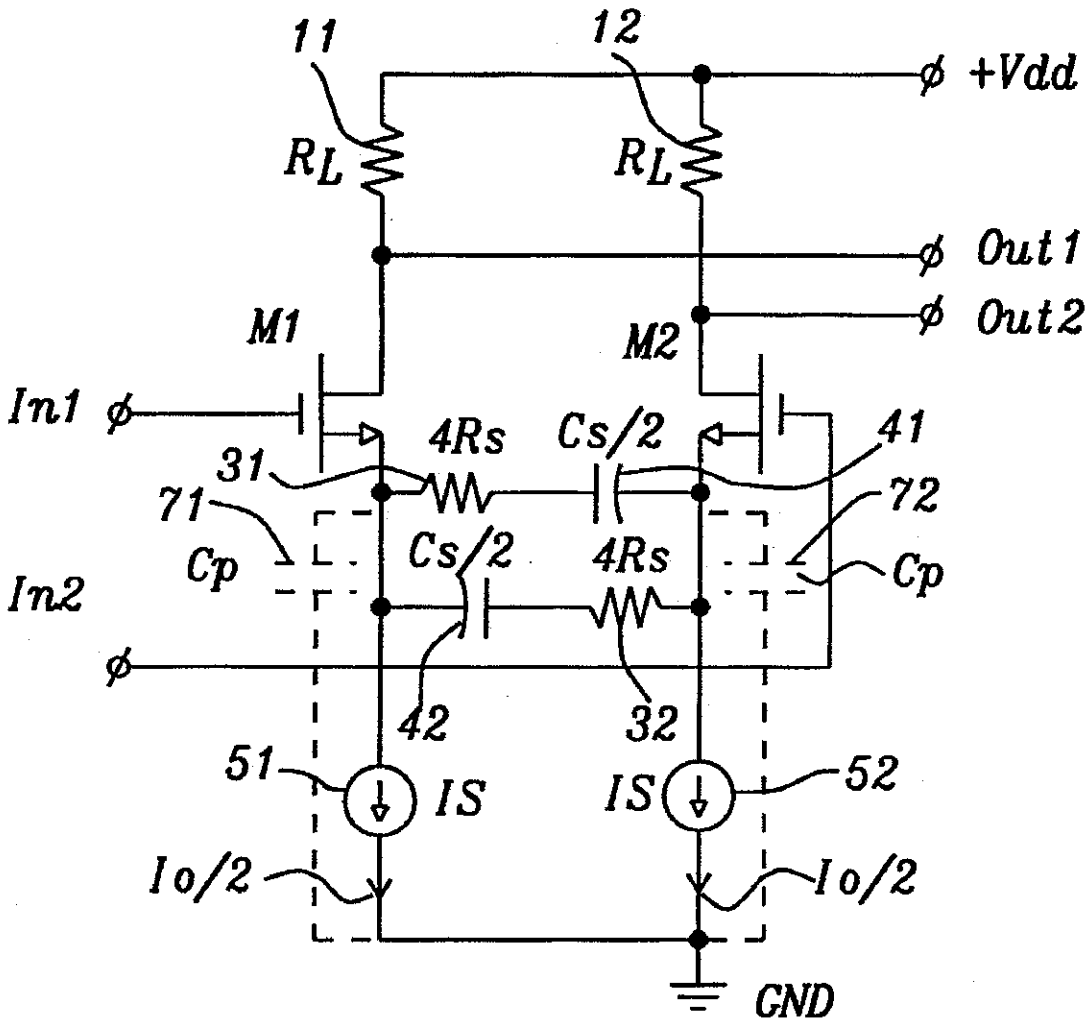

11
12
ø +Vdd
RL
RL
ø Out1
ø Out2
M1
M2
In1 ø
4Rs
Cs/2
41
31
71
72
Cp
Cs/2
4Rs
Cp
In2
ø
42
32
51
IS
IS
52
Io/2
Io/2
GND

FIG. 5

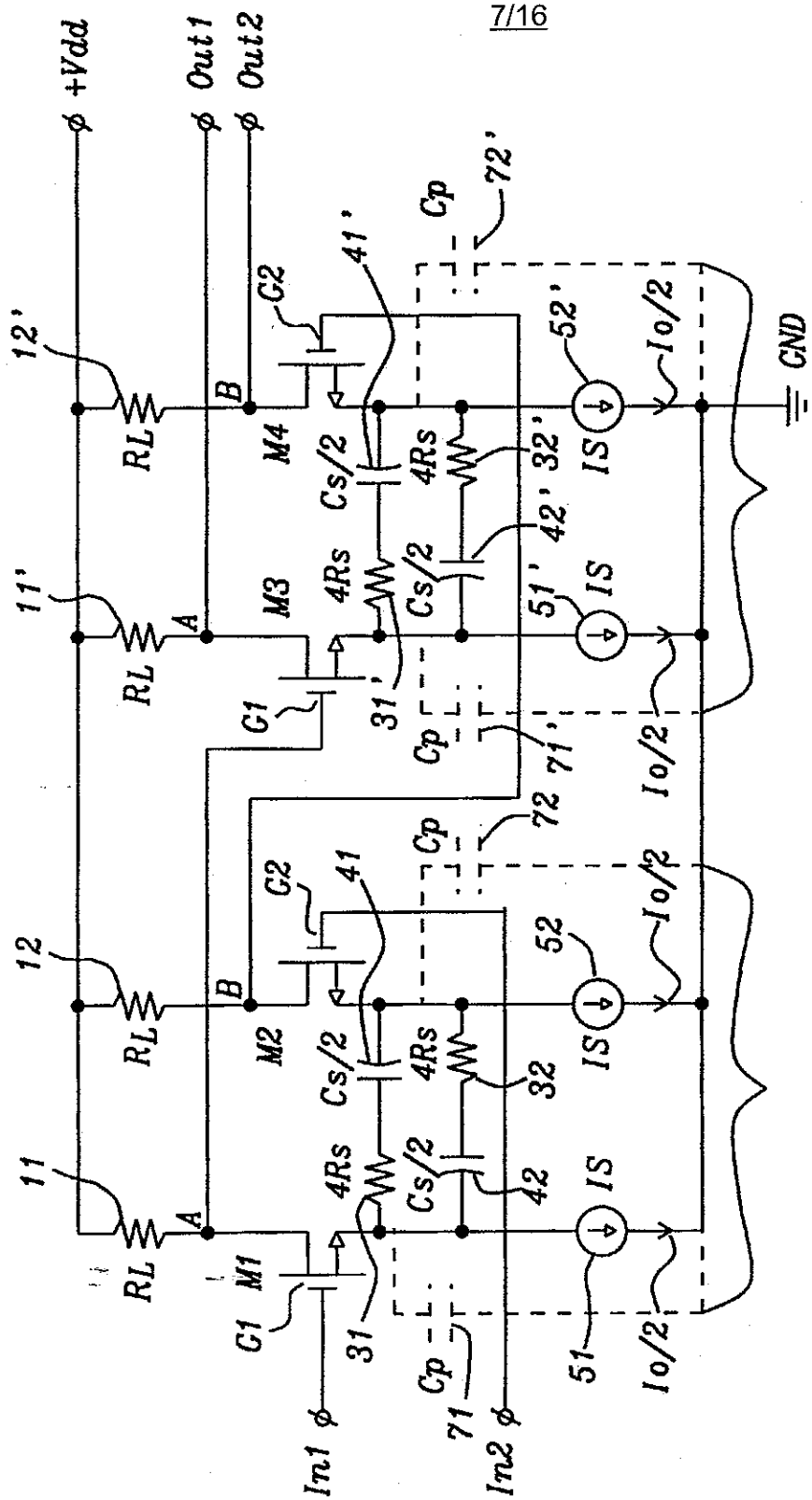

+Vdd
Out1
Out2
12'
11'
12
11
RL
A
B
M1
M2
M3
M4
C1
C2
Cs/2
4Rs
Cp
IS
Io/2
GND
In1
In2
31
31'
32
32'
41
41'
42
42'
51
51'
52
52'
71
71'
72
72'
First Differential Amplifier Stage
Second Differential Amplifier Stage

FIG. 6

REPLACEMENT SHEET
- 9 MAY 2006

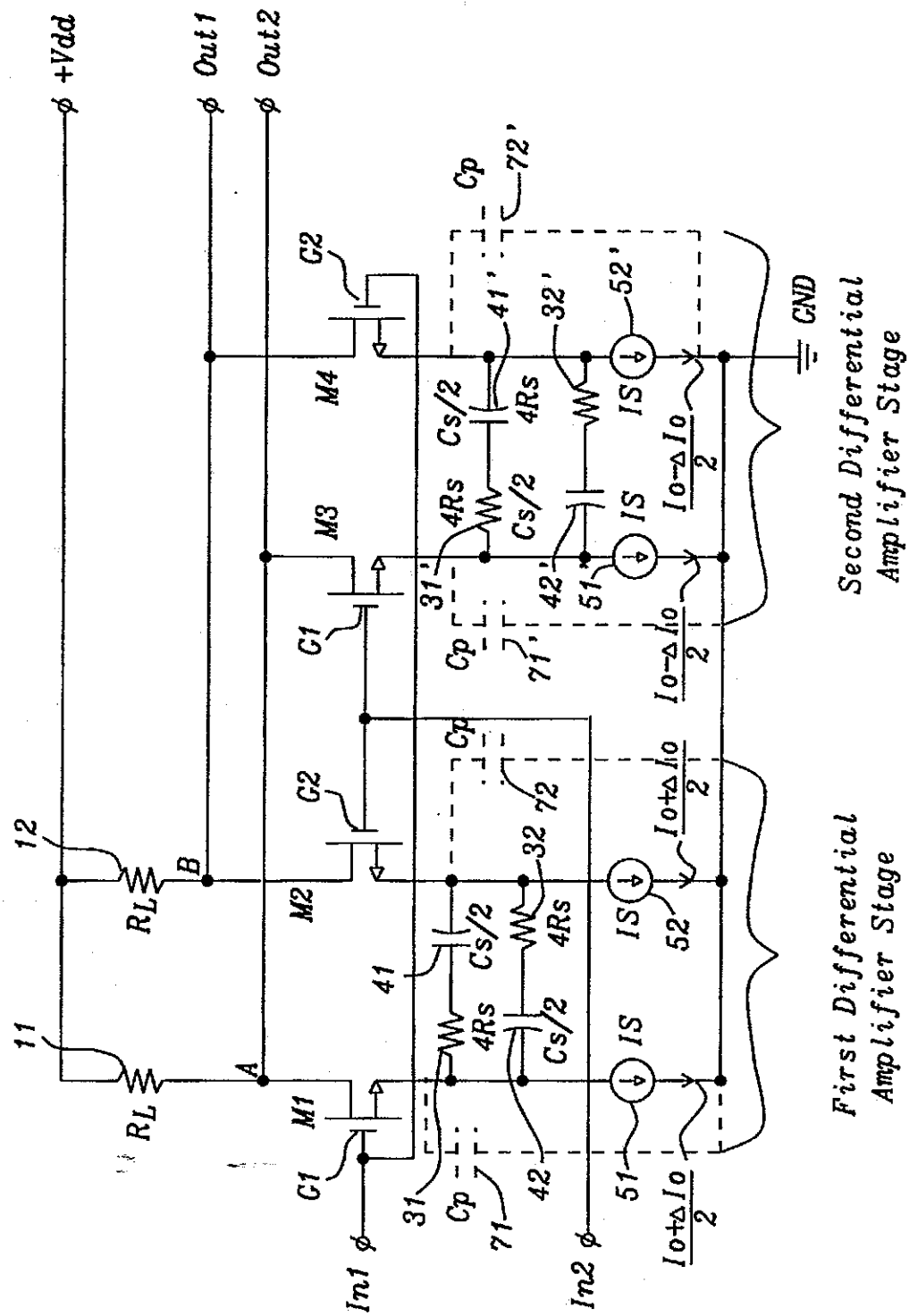


FIG. 7

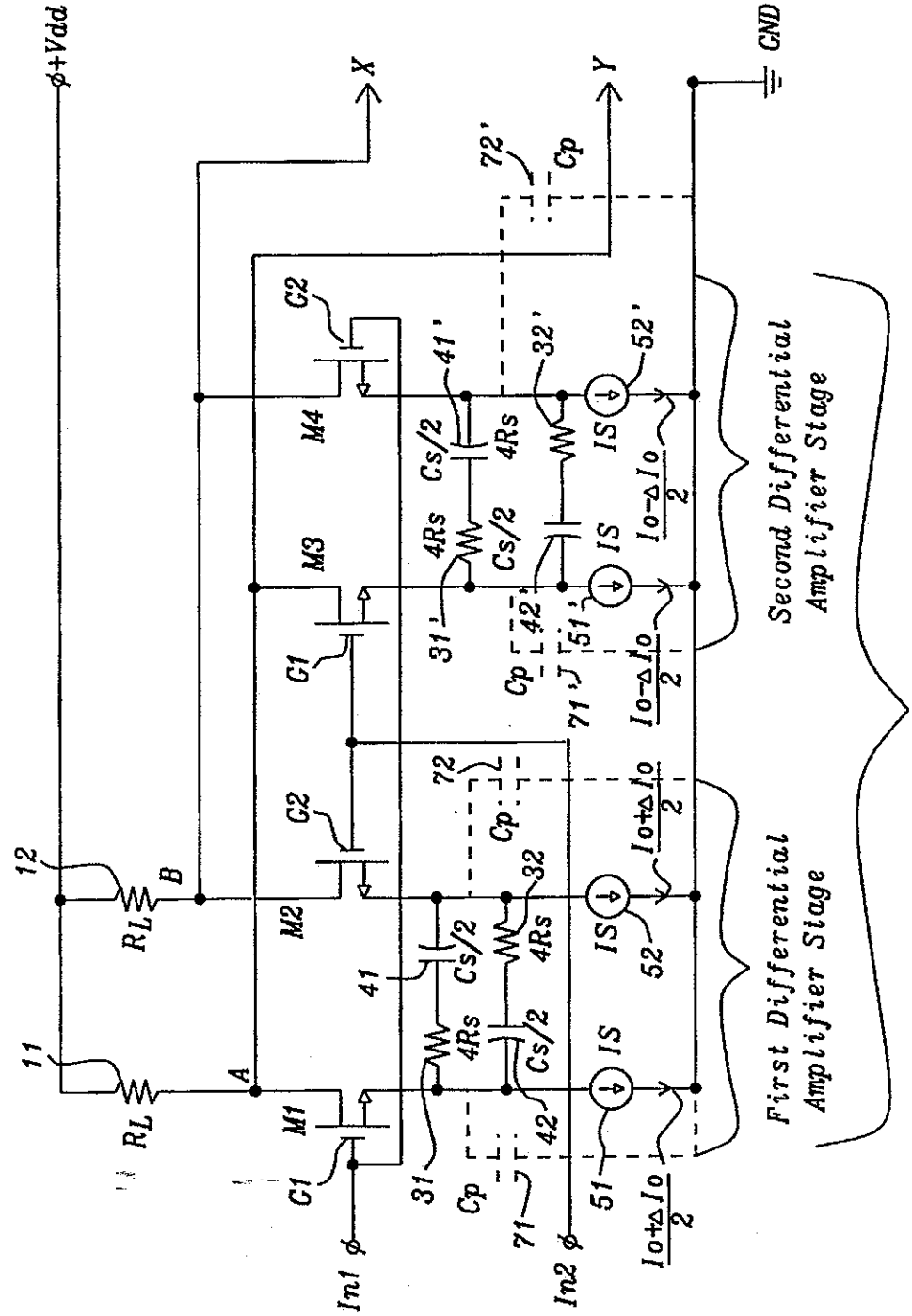

φ+Vdd
GND
X
Y
12
11
RL
B
A
M1
M2
M3
M4
C1
C2
In1 φ
In2 φ
41
41'
42
42'
31
31'
32
32'
51
51'
52
52'
71
71'
72
72'
Cp
Cs/2
4Rs
IS
Io+ΔIo/2
Io-ΔIo/2
First Differential Amplifier Stage
Second Differential Amplifier Stage
First Variable Gain Differential Amplifier

FIG. 8a

REPLACEMENT SHEET

9 MAY 2006

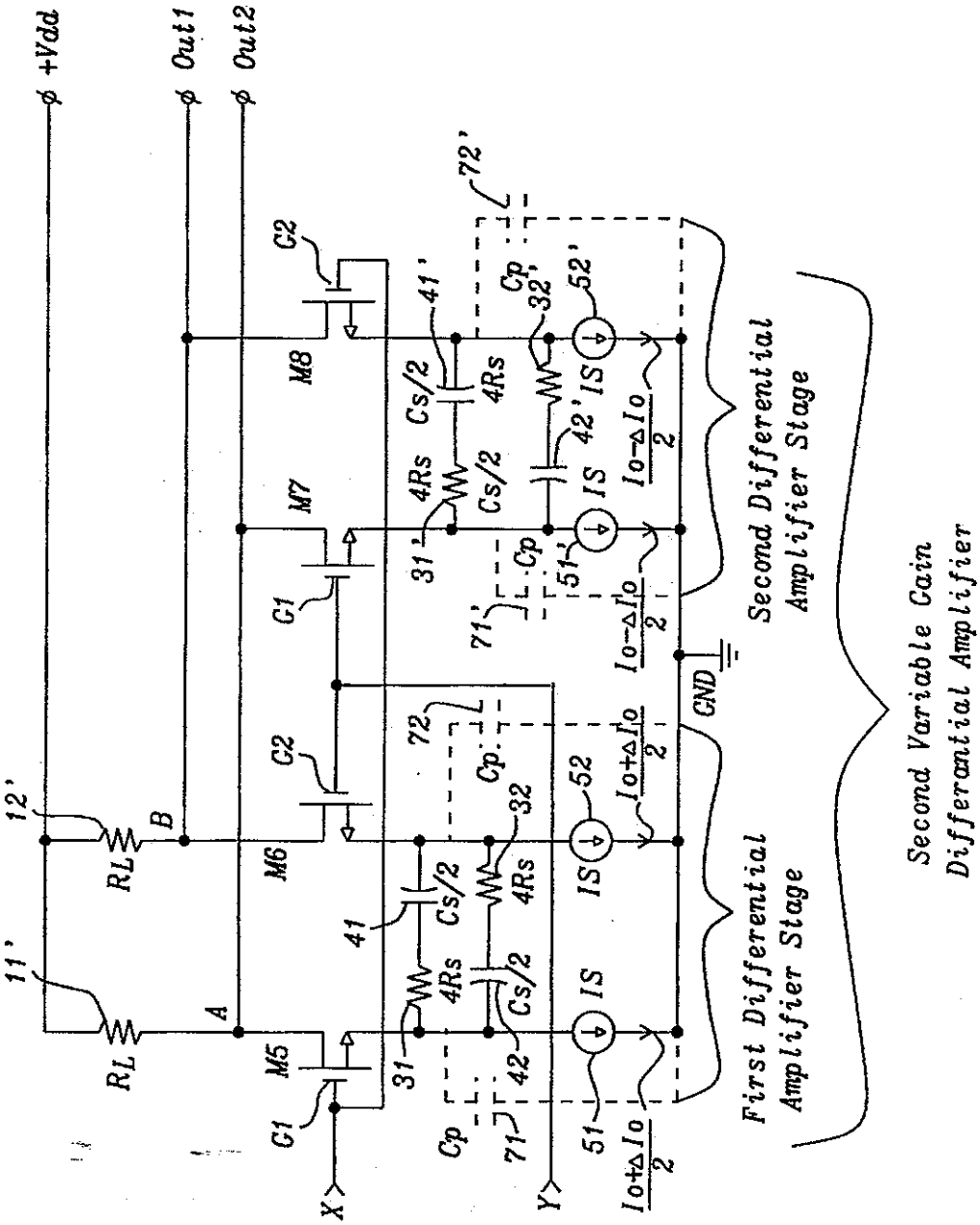


FIG. 8b

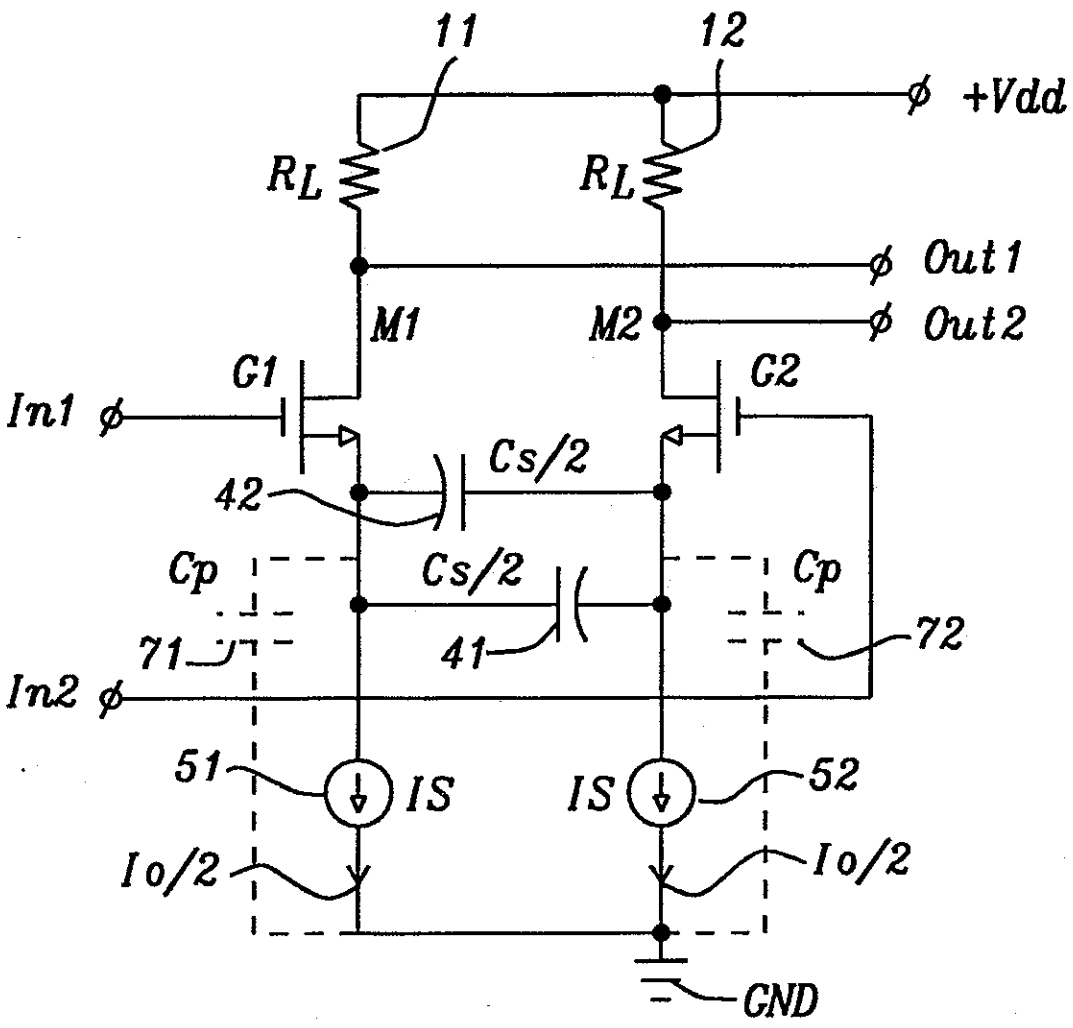

11
12
+Vdd
RL
RL
Out1
Out2
M1
M2
G1
G2
In1
Cs/2
42
Cp
Cs/2
Cp
71
41
72
In2
51
IS
IS
52
Io/2
Io/2
GND

FIG. 9

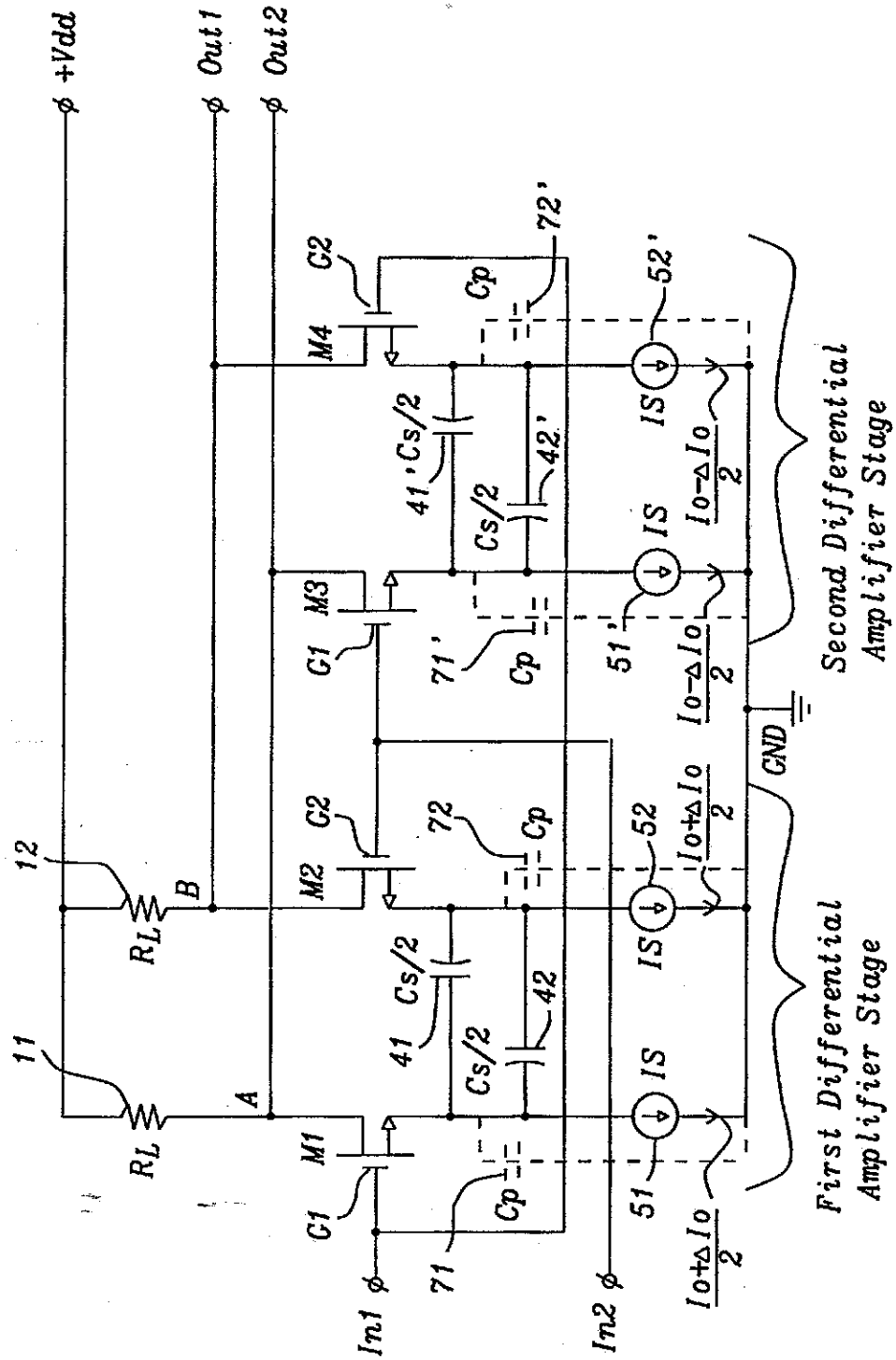
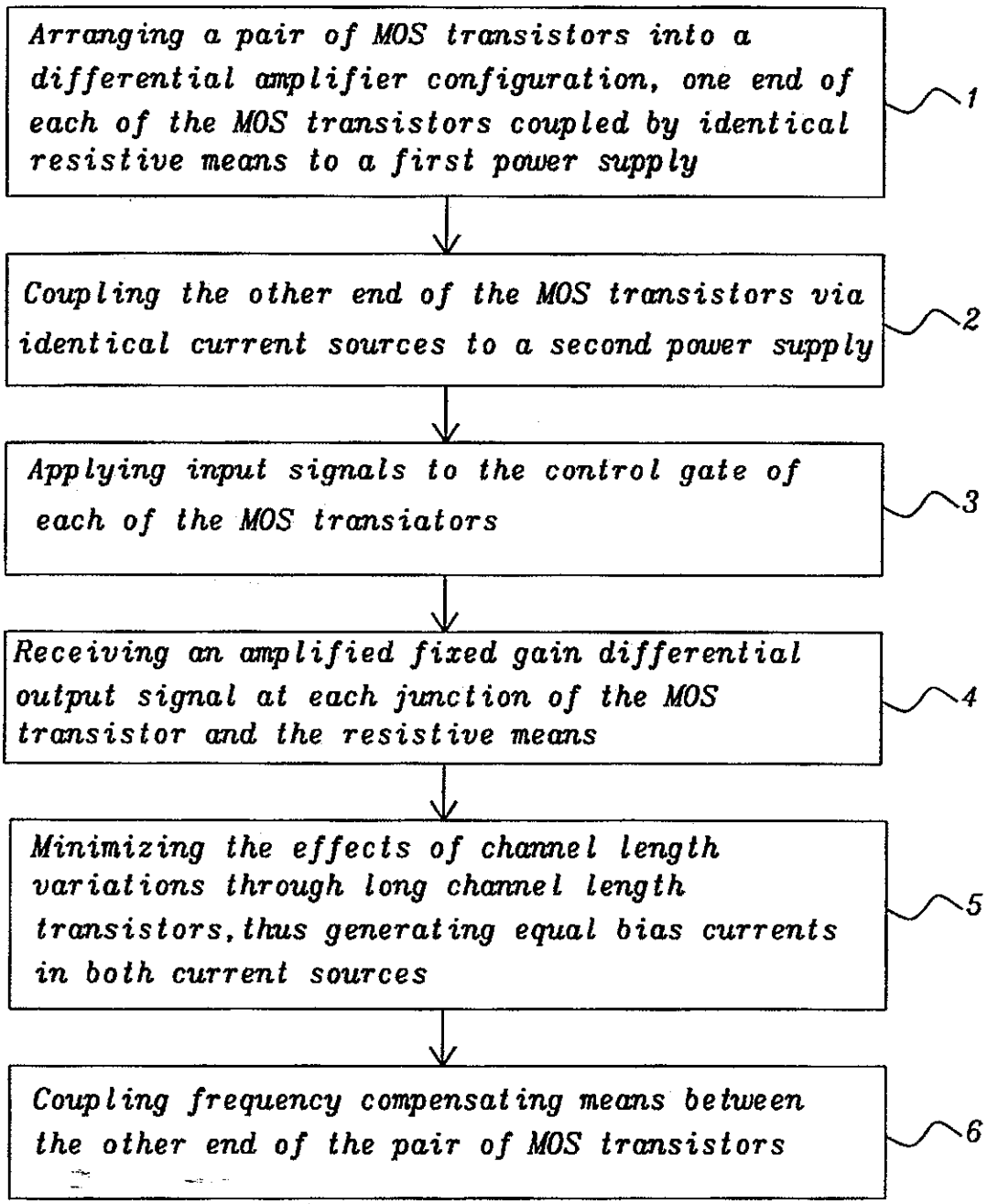

φ +Vdd
φ Out1
φ Out2
12
11
RL
RL
B
A
M1
M2
M3
M4
C1
C2
C1
C2
Cp
Cp
Cp
Cp
71
72
71'
72'
41
42
41'
42'
Cs/2
Cs/2
Cs/2
Cs/2
51
52
51'
52'
IS
IS
IS
IS
Io+ΔIo/2
Io-ΔIo/2
Io-ΔIo/2
Io+ΔIo/2
GND
In1 φ
In2 φ
First Differential Amplifier Stage
Second Differential Amplifier Stage

FIG. 10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1
Coupling the other end of the MOS transistors via identical current sources to a second power supply
2
Applying input signals to the control gate of each of the MOS transiators
3
Receiving an amplified fixed gain differential output signal at each junction of the MOS transistor and the resistive means
4
Minimizing the effects of channel length variations through long channel length transistors, thus generating equal bias currents in both current sources
5
Coupling frequency compensating means between the other end of the pair of MOS transistors
6

FIG. 11

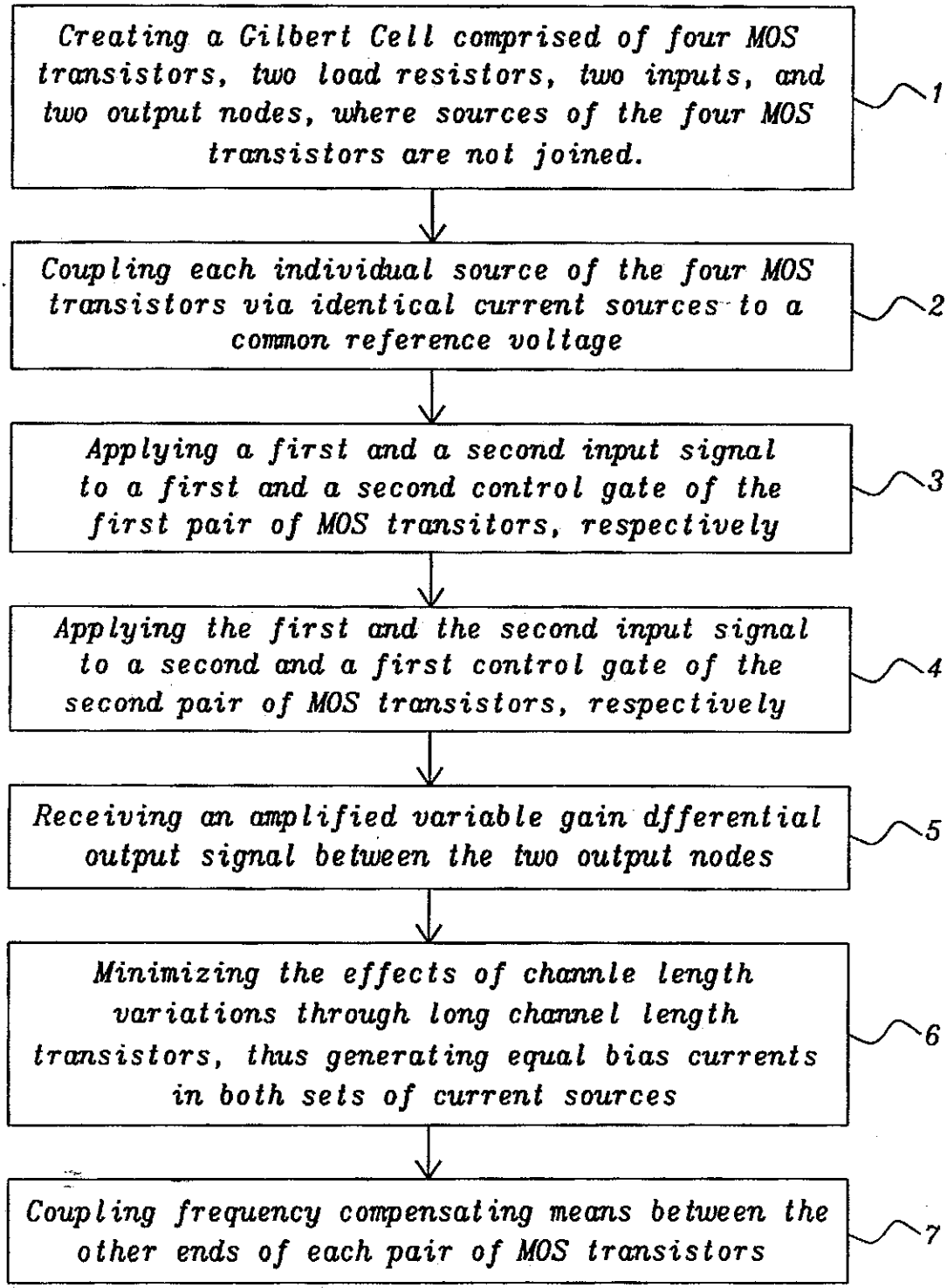
Creating a Gilbert Cell comprised of four MOS transistors, two load resistors, two inputs, and two output nodes, where sources of the four MOS transistors are not joined.
1
Coupling each individual source of the four MOS transistors via identical current sources to a common reference voltage
2
Applying a first and a second input signal to a first and a second control gate of the first pair of MOS transitors, respectively
3
Applying the first and the second input signal to a second and a first control gate of the second pair of MOS transistors, respectively
4
Receiving an amplified variable gain dfferential output signal between the two output nodes
5
Minimizing the effects of channle length variations through long channel length transistors, thus generating equal bias currents in both sets of current sources
6
Coupling frequency compensating means between the other ends of each pair of MOS transistors
7

FIG. 12

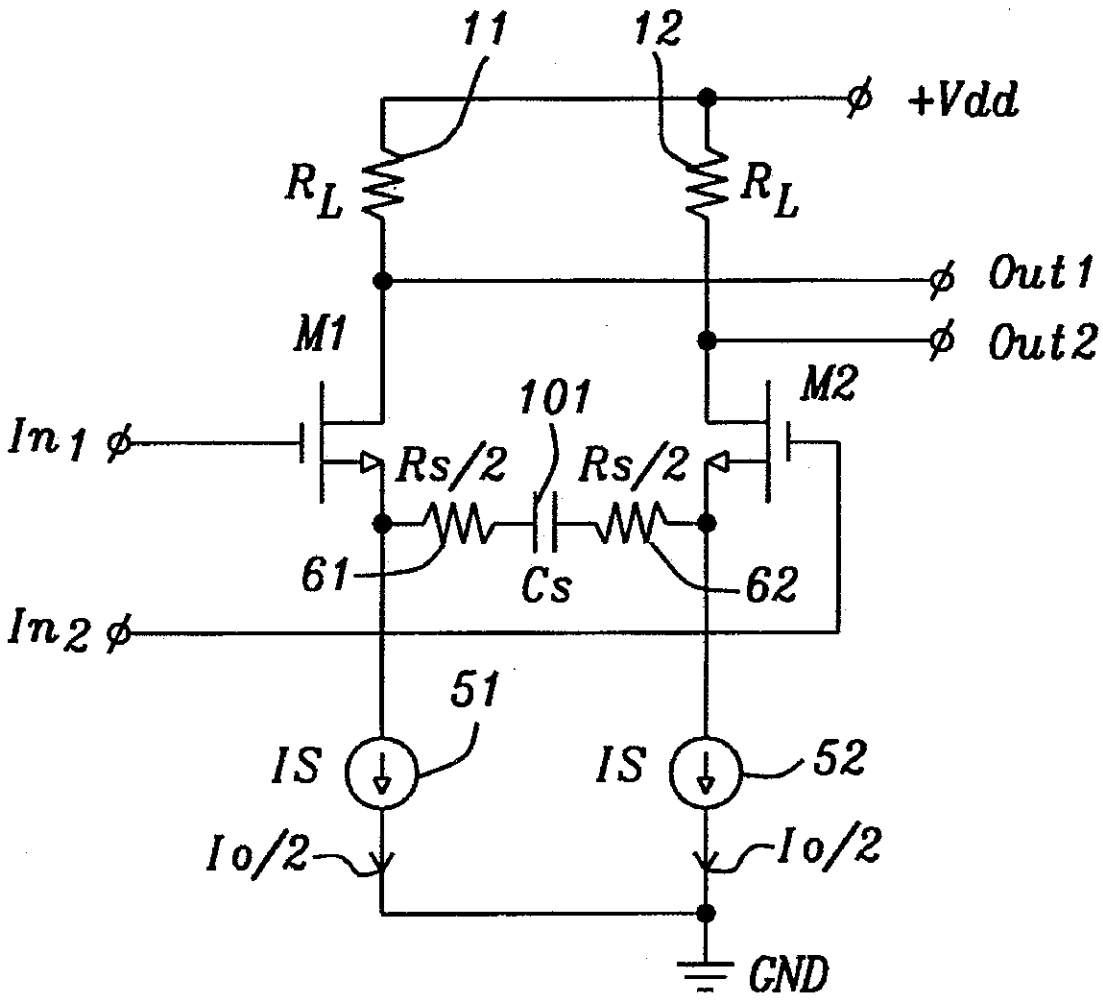
11
12
+Vdd
R_L
R_L
Out1
Out2
M1
M2
101
In1
Rs/2
Rs/2
61
Cs
62
In2
51
IS
IS
52
Io/2
Io/2
GND

FIG. 13

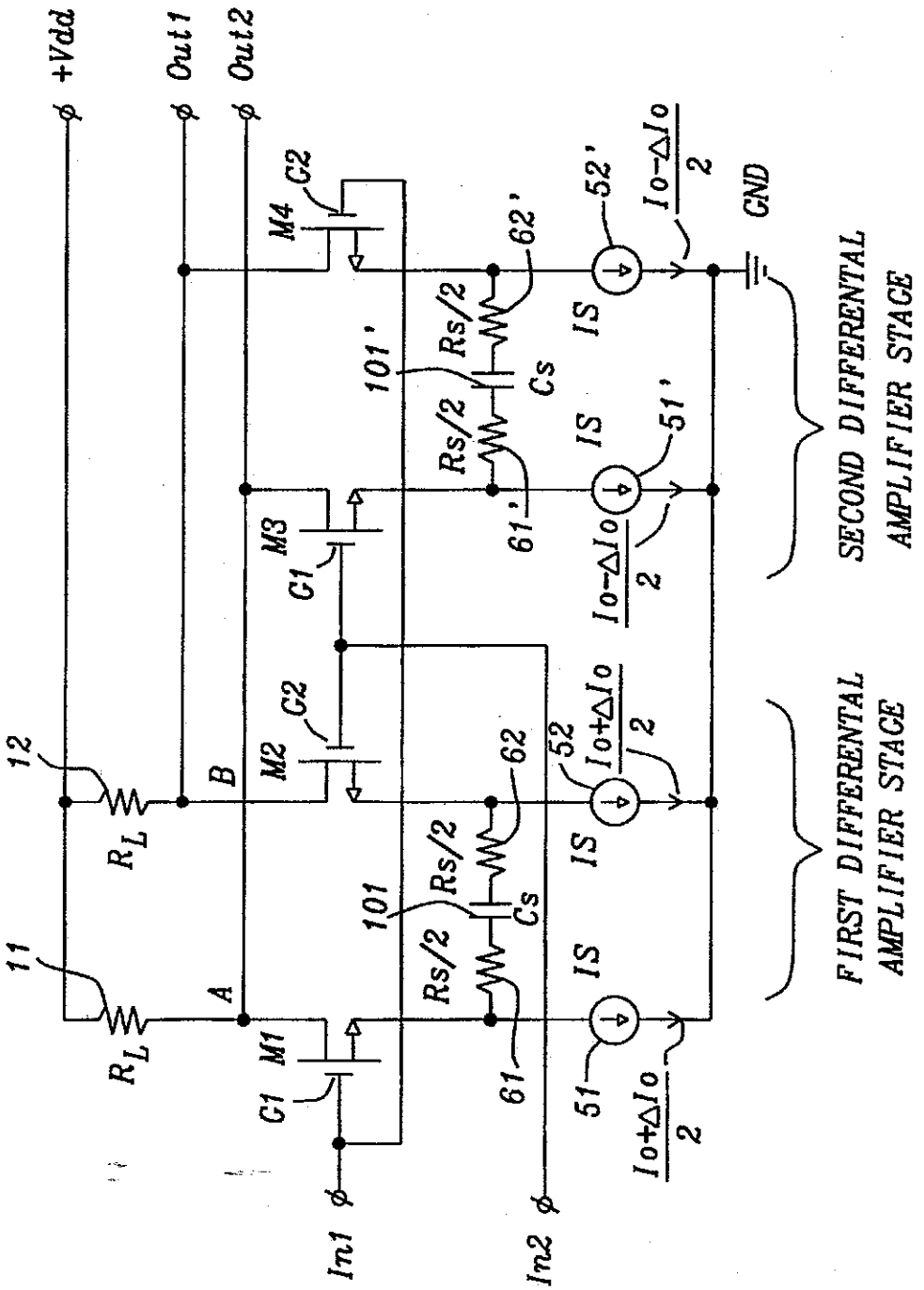
+Vdd
Out1
Out2
M4
C2
M3
C1
M2
C2
M1
C1
12
11
R_L
R_L
A
B
101
101'
Rs/2
Rs/2
Rs/2
Rs/2
Cs
Cs
62'
61'
62
61
52'
51'
52
51
IS
IS
IS
IS
$\frac{I_o-\Delta I_o}{2}$
$\frac{I_o-\Delta I_o}{2}$
$\frac{I_o+\Delta I_o}{2}$
$\frac{I_o+\Delta I_o}{2}$
GND
Im1
Im2
SECOND DIFFERENTAL AMPLIFIER STAGE
FIRST DIFFERENTAL AMPLIFIER STAGE

FIG. 14