FIG. 1

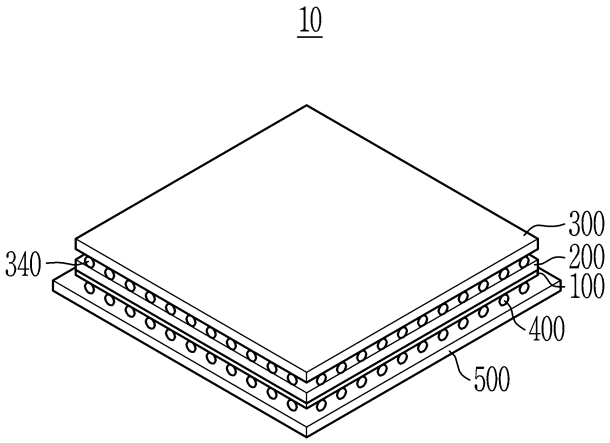


FIG. 2

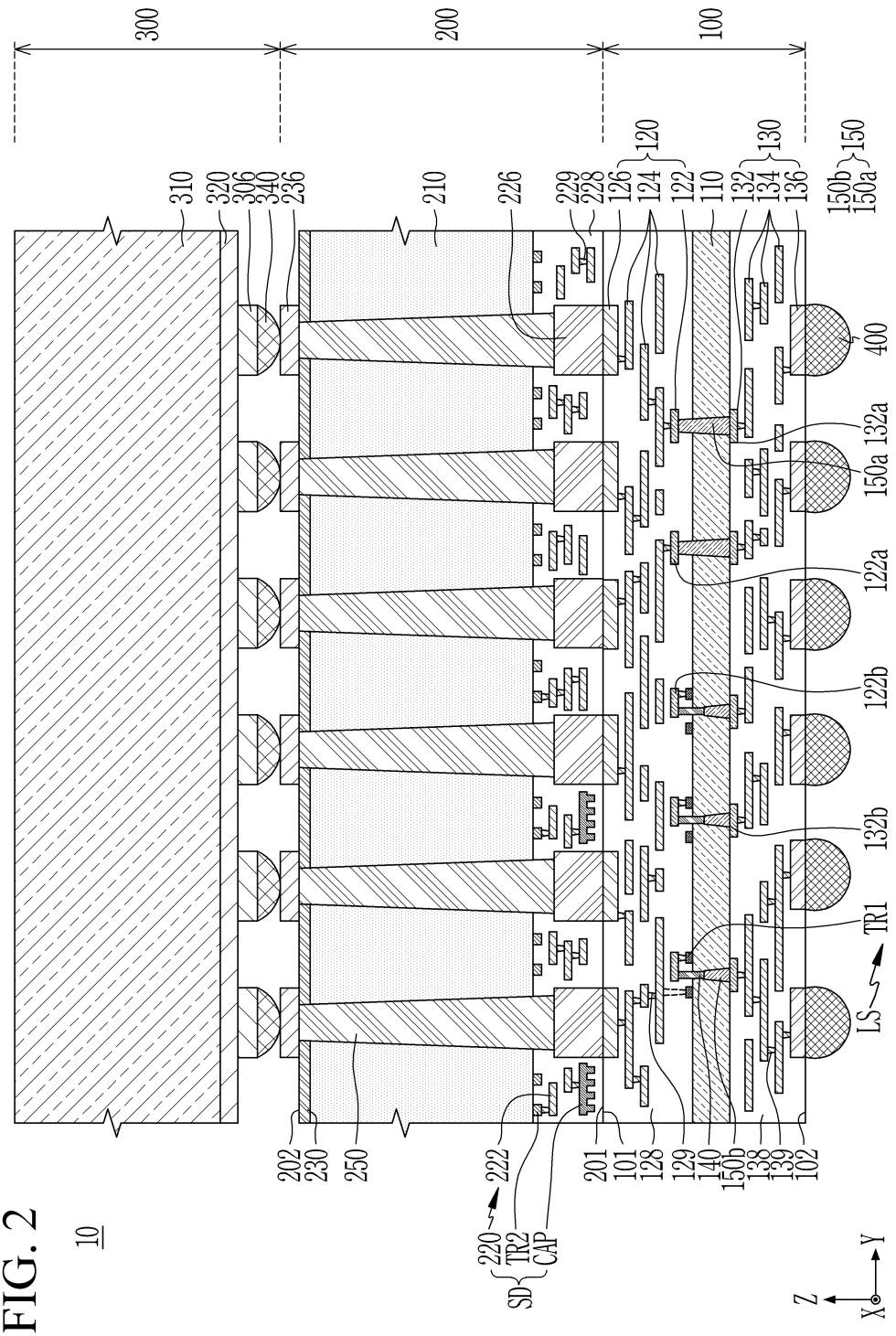

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FIG. 3

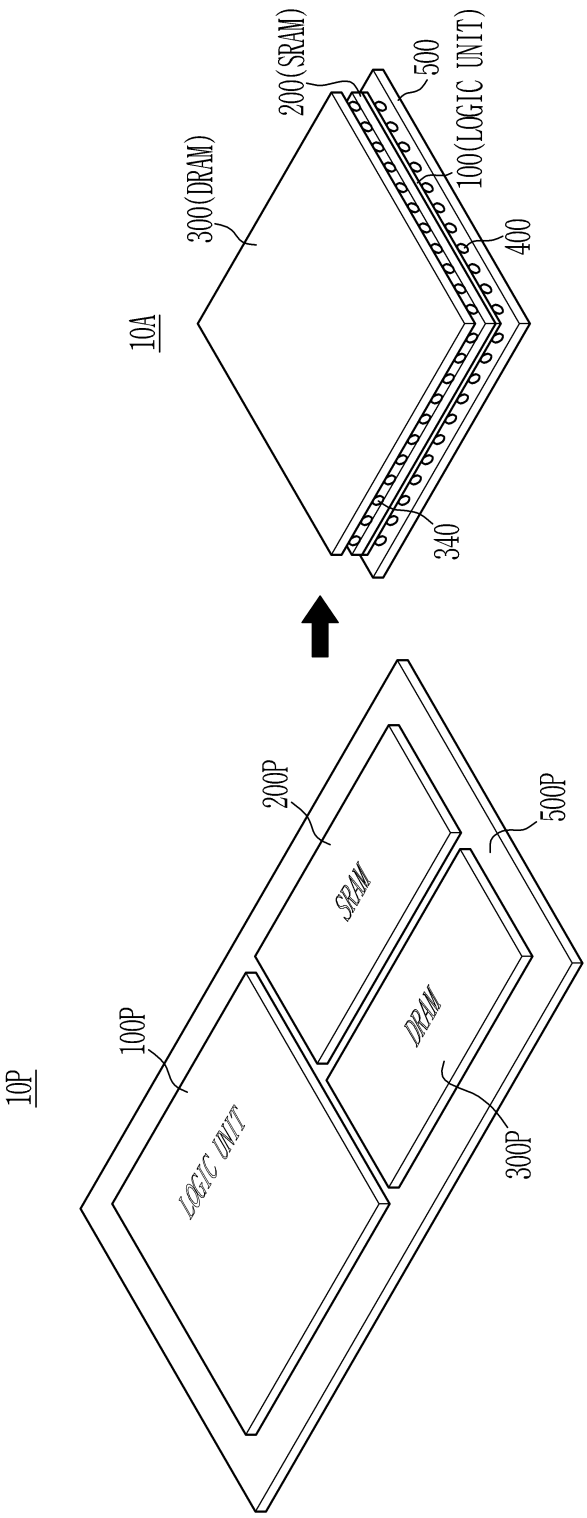

10A
300(DRAM)
200(SRAM)
500
100(LOGIC UNIT)
400
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10P
100P
LOGIC UNIT
200P
SRAM
DRAM
500P
300P

FIG. 4

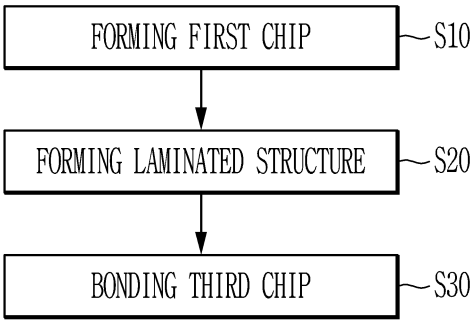

FORMING FIRST CHIP
S10
FORMING LAMINATED STRUCTURE
S20
BONDING THIRD CHIP
S30

FIG. 5A

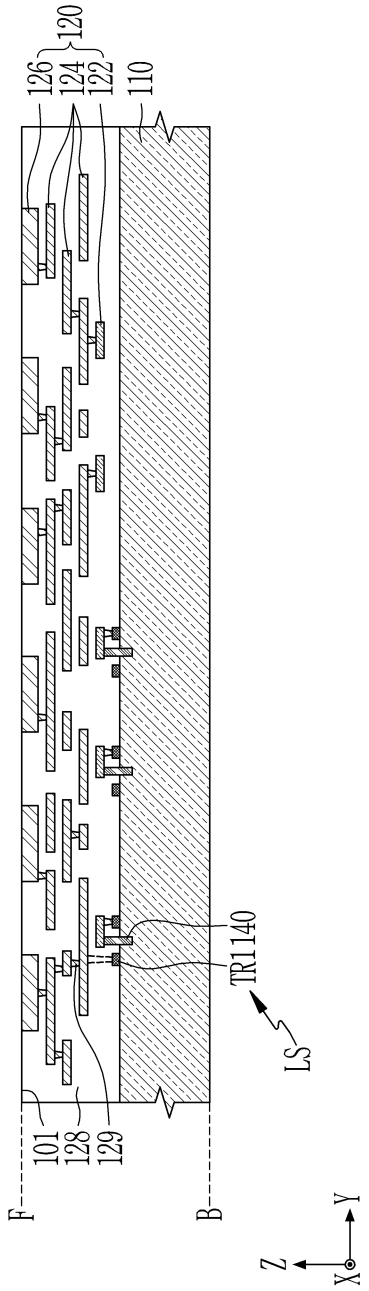


FIG. 5B

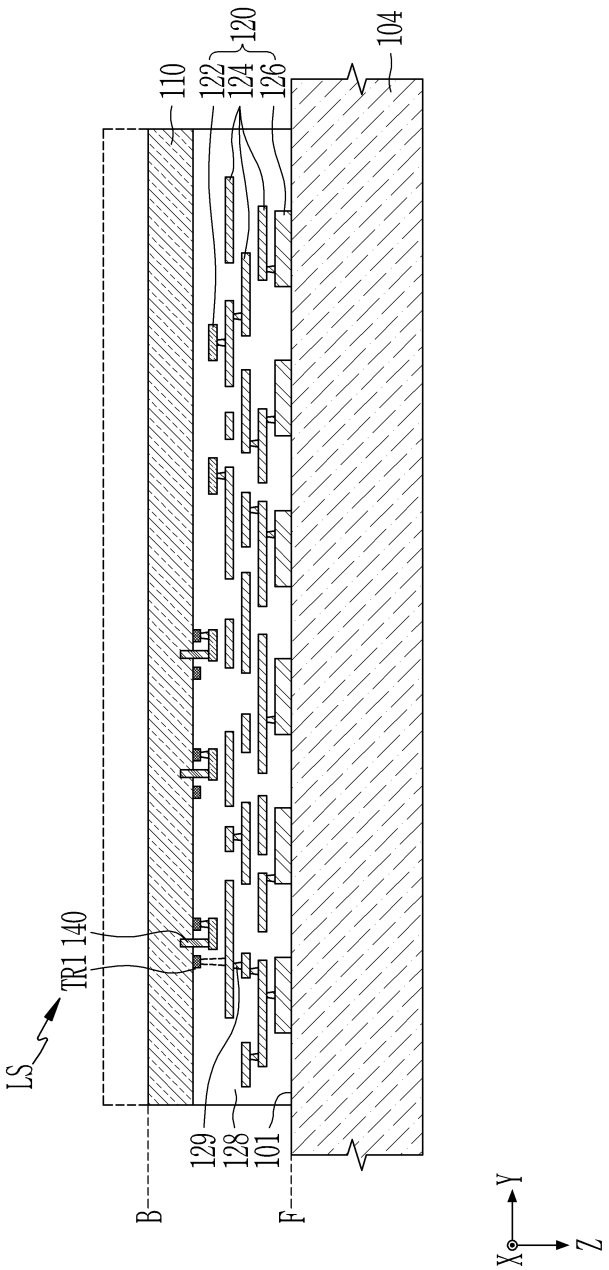


FIG. 5C

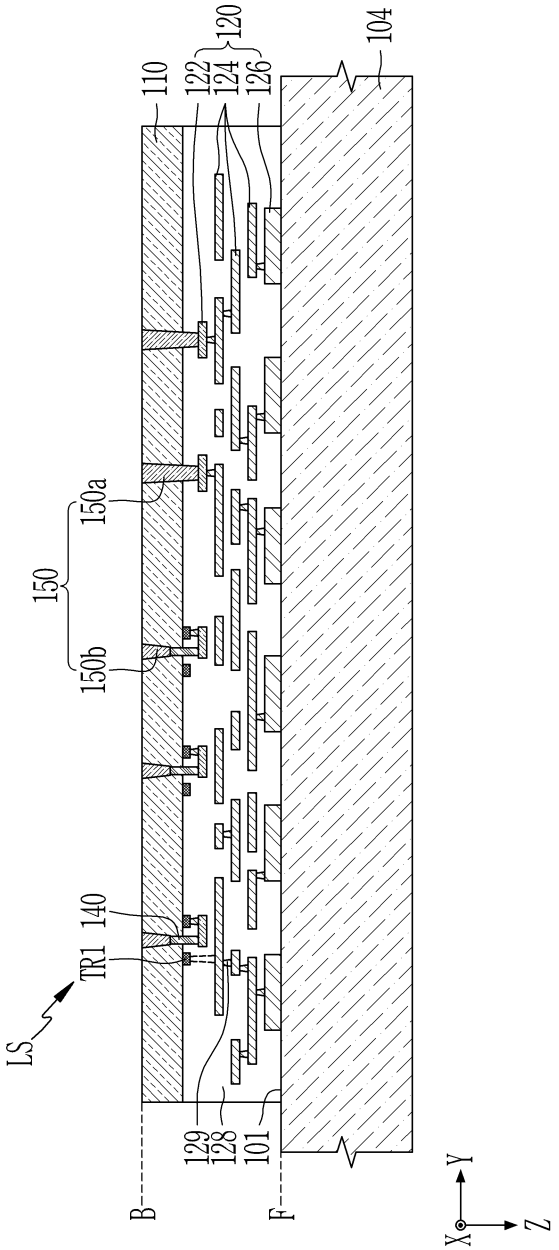

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FIG. 5D

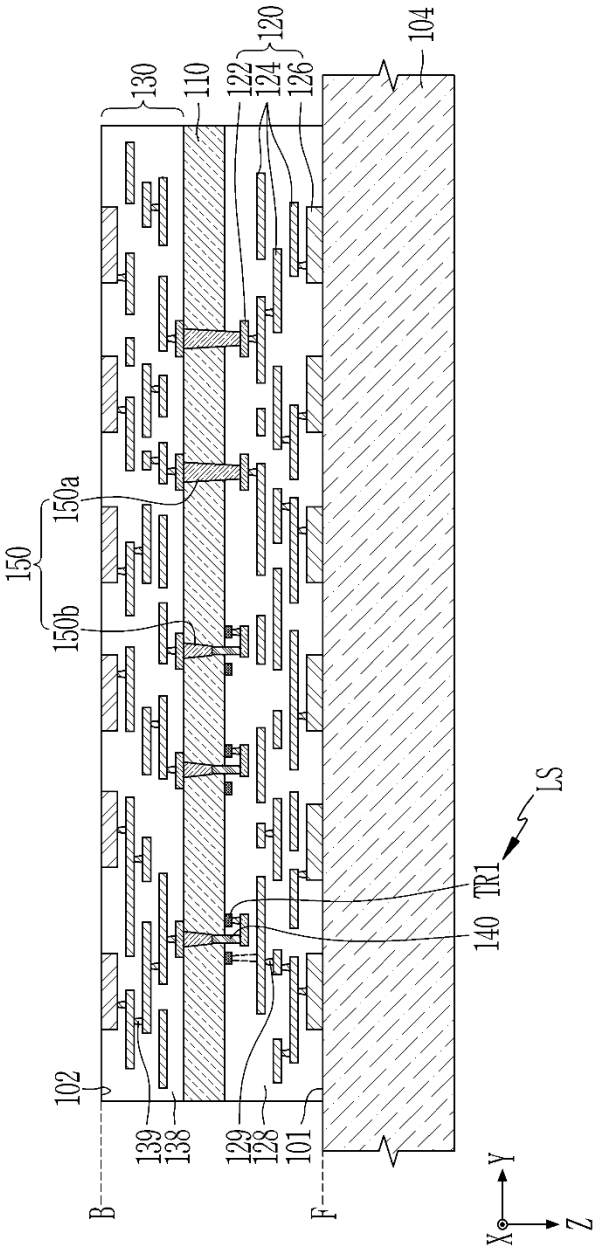

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FIG. 5E

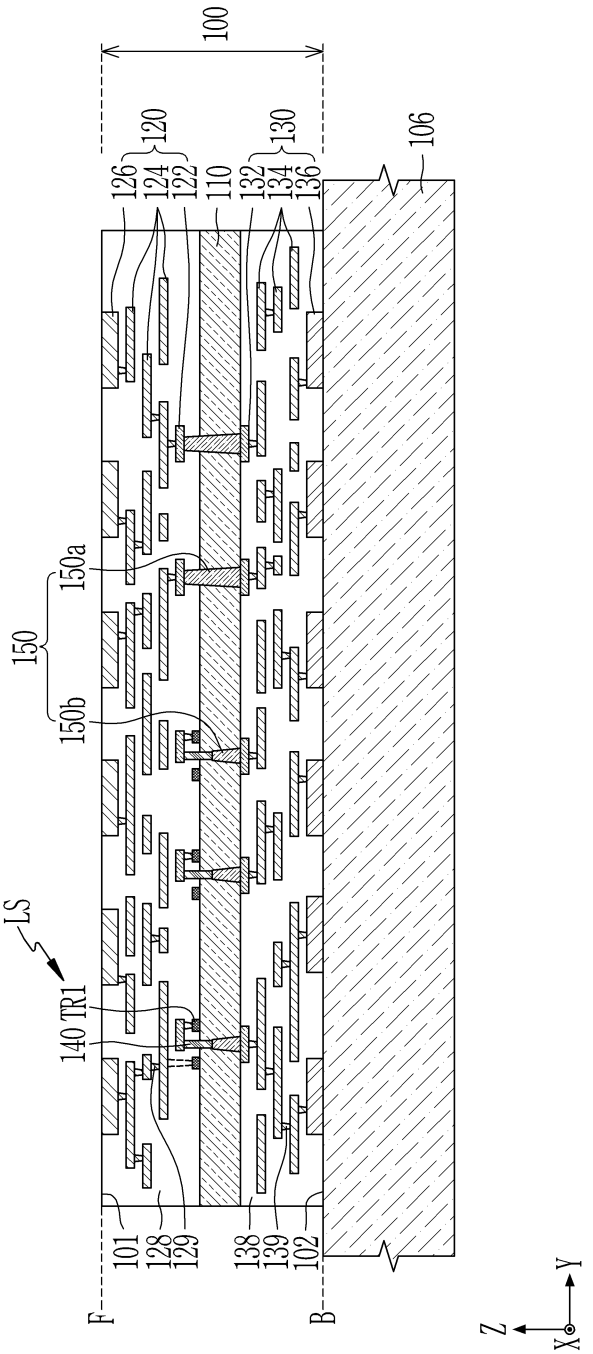

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FIG. 6A

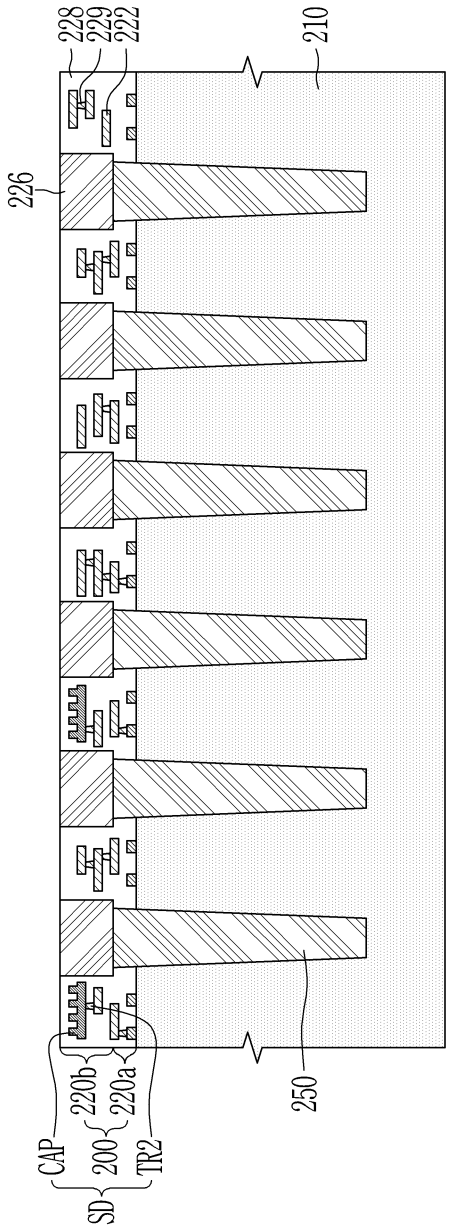


FIG. 6B

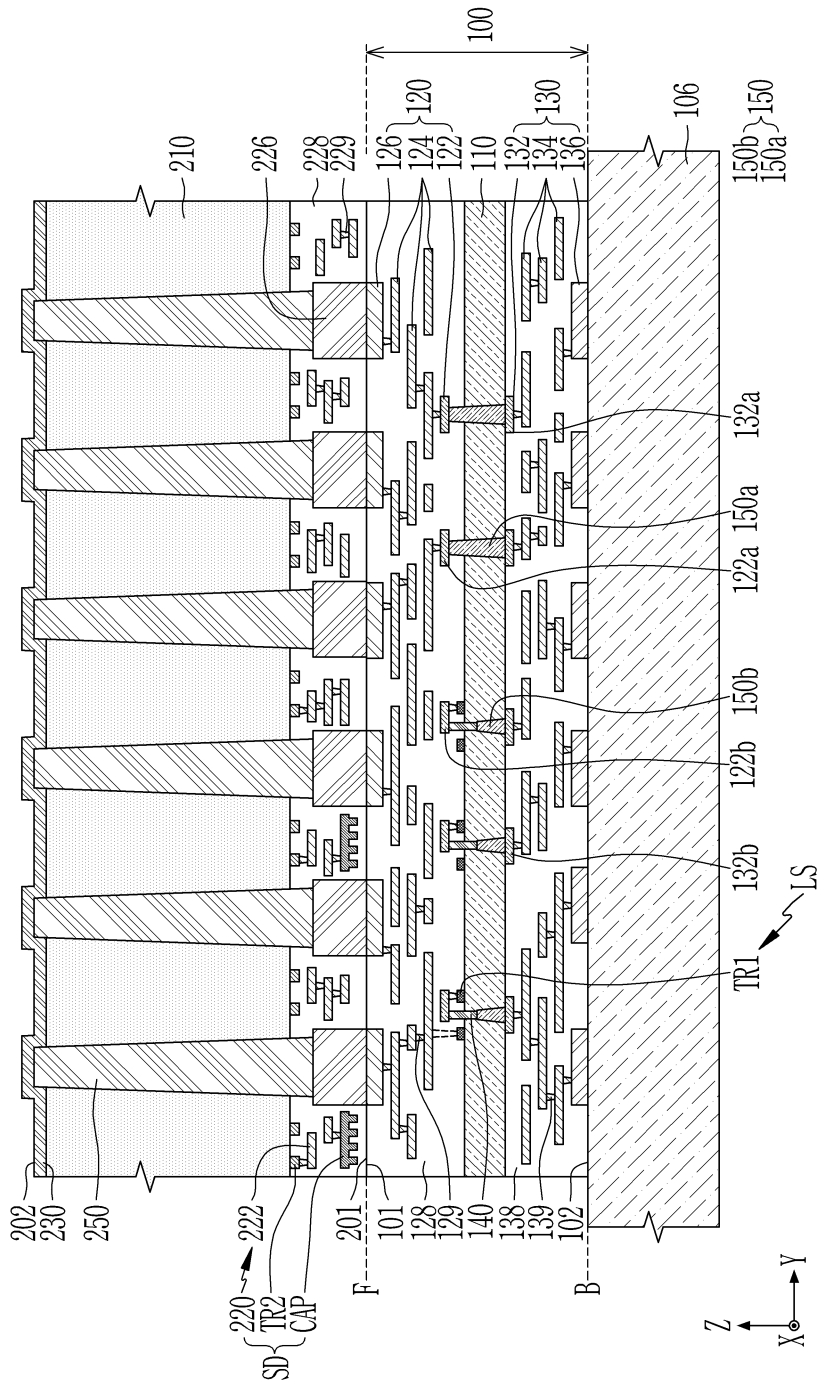

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FIG. 6C

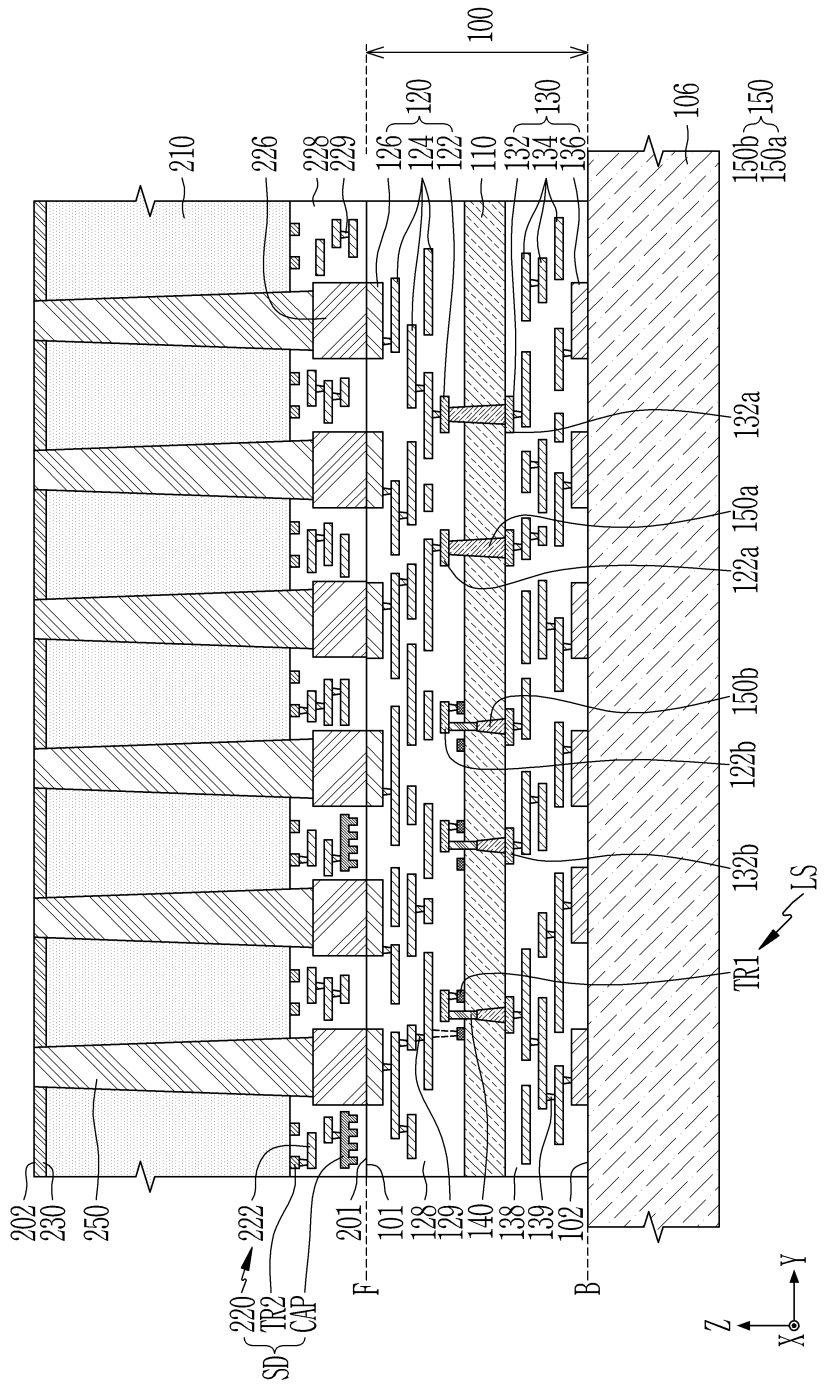

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FIG. 6D

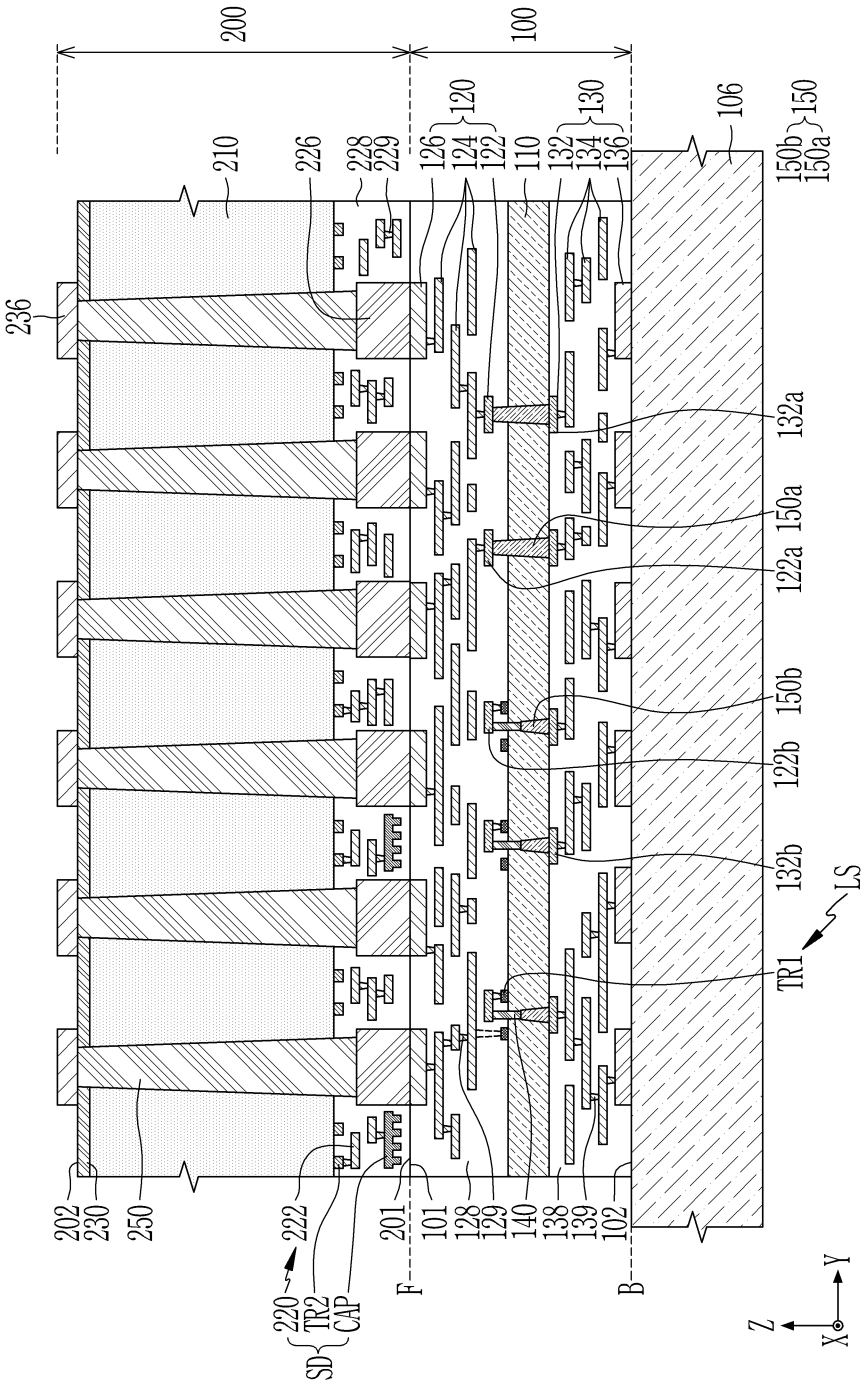

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FIG. 7

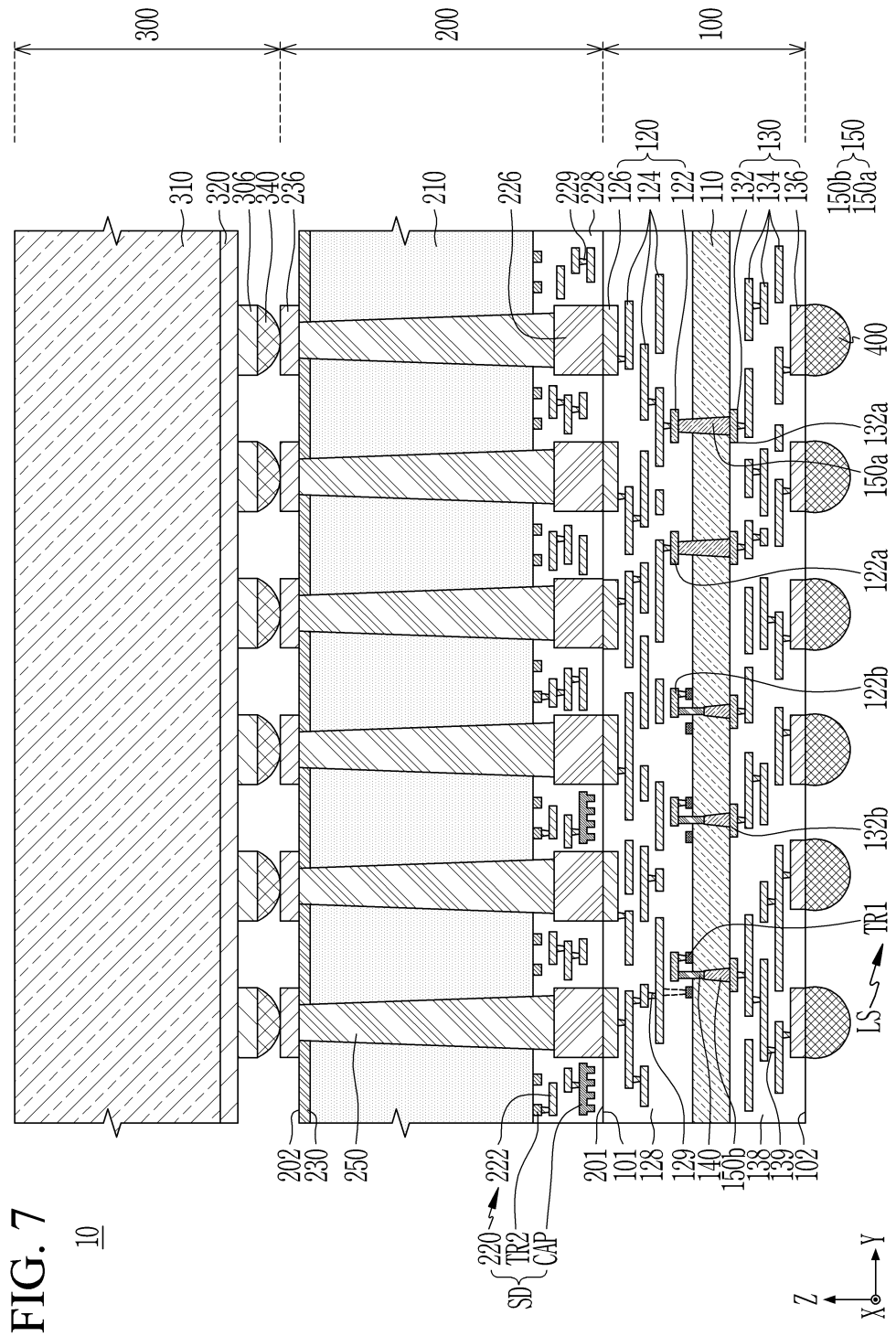

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FIG. 8

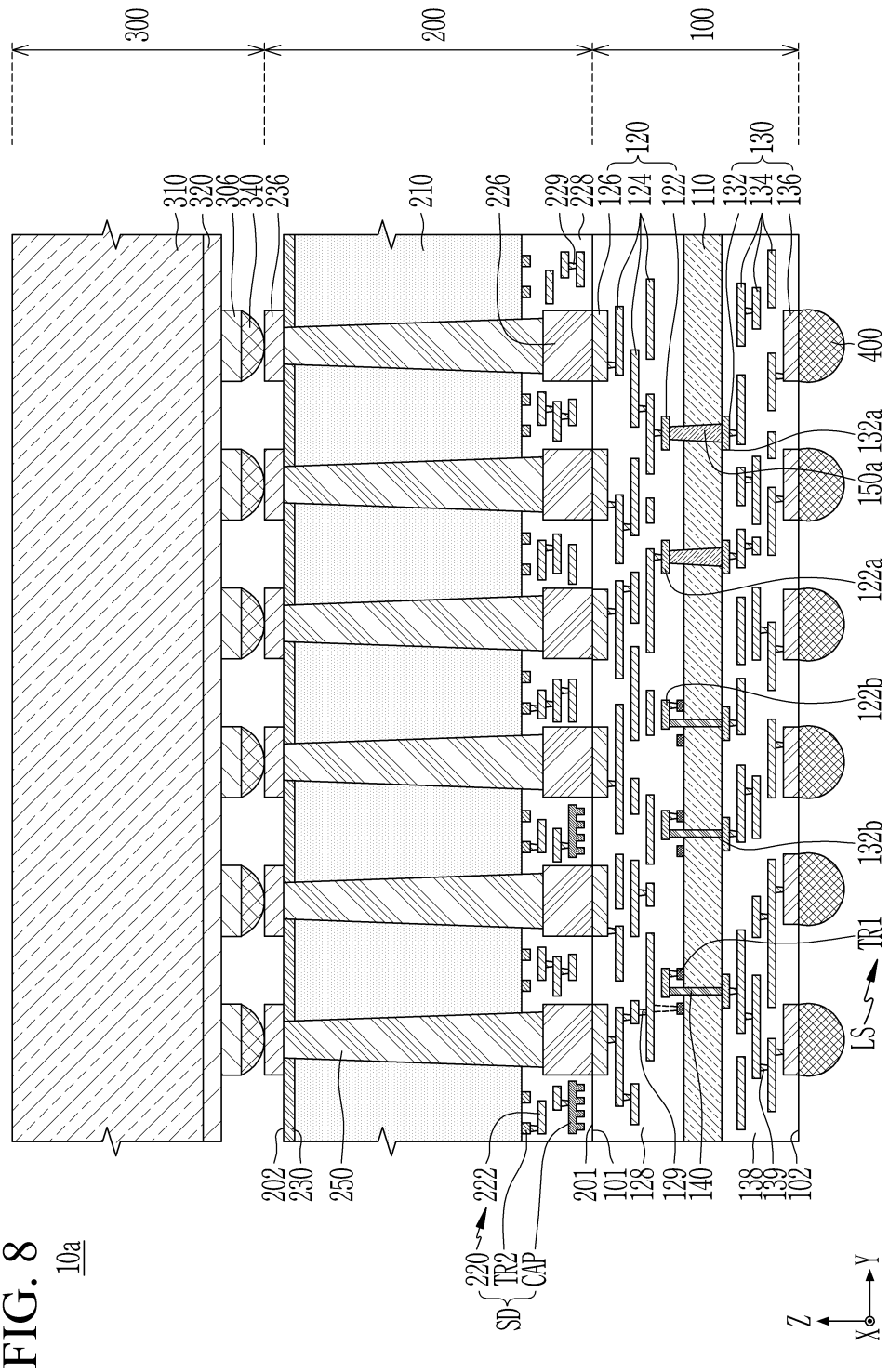

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FIG. 9

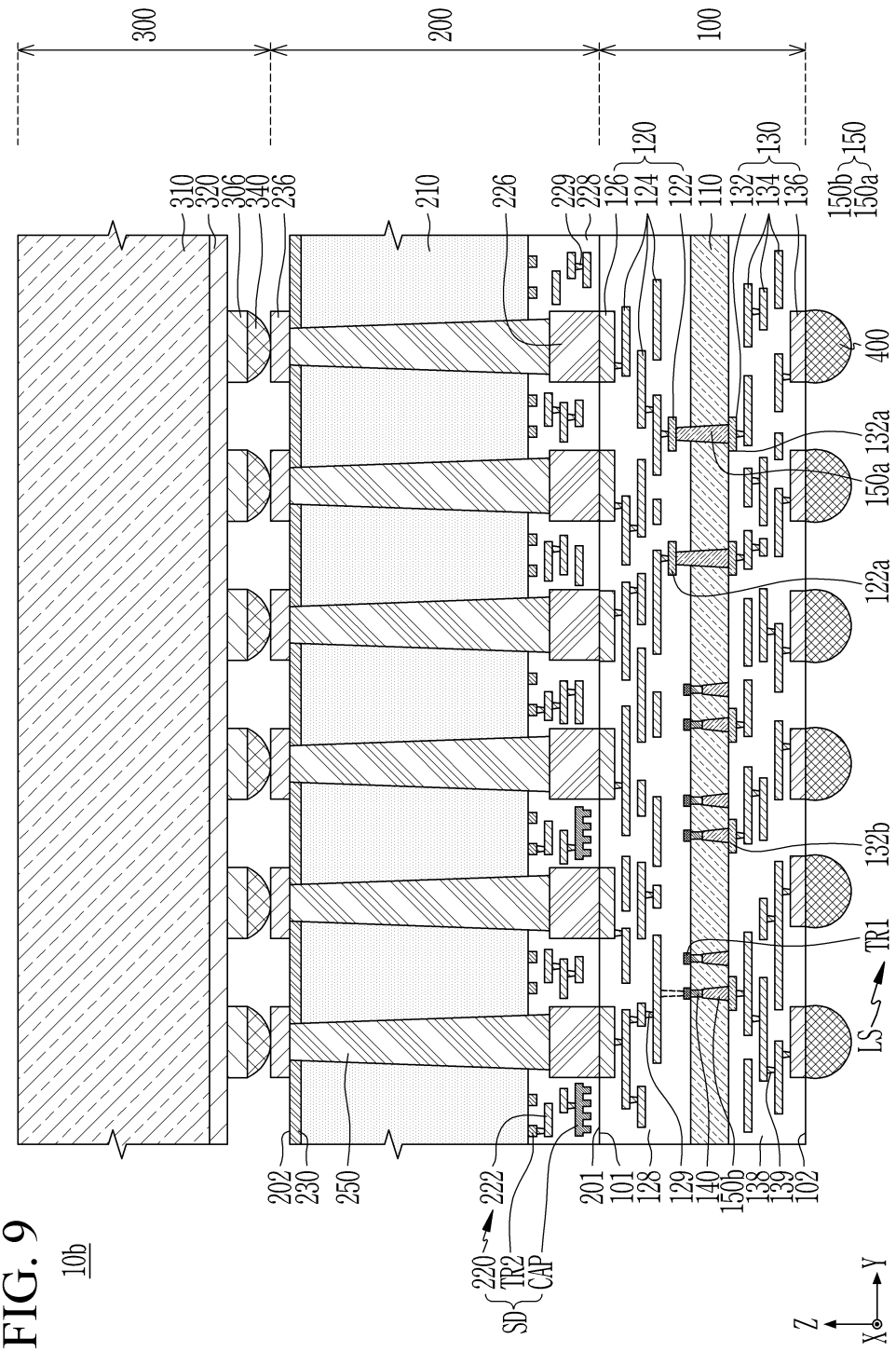

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FIG. 10

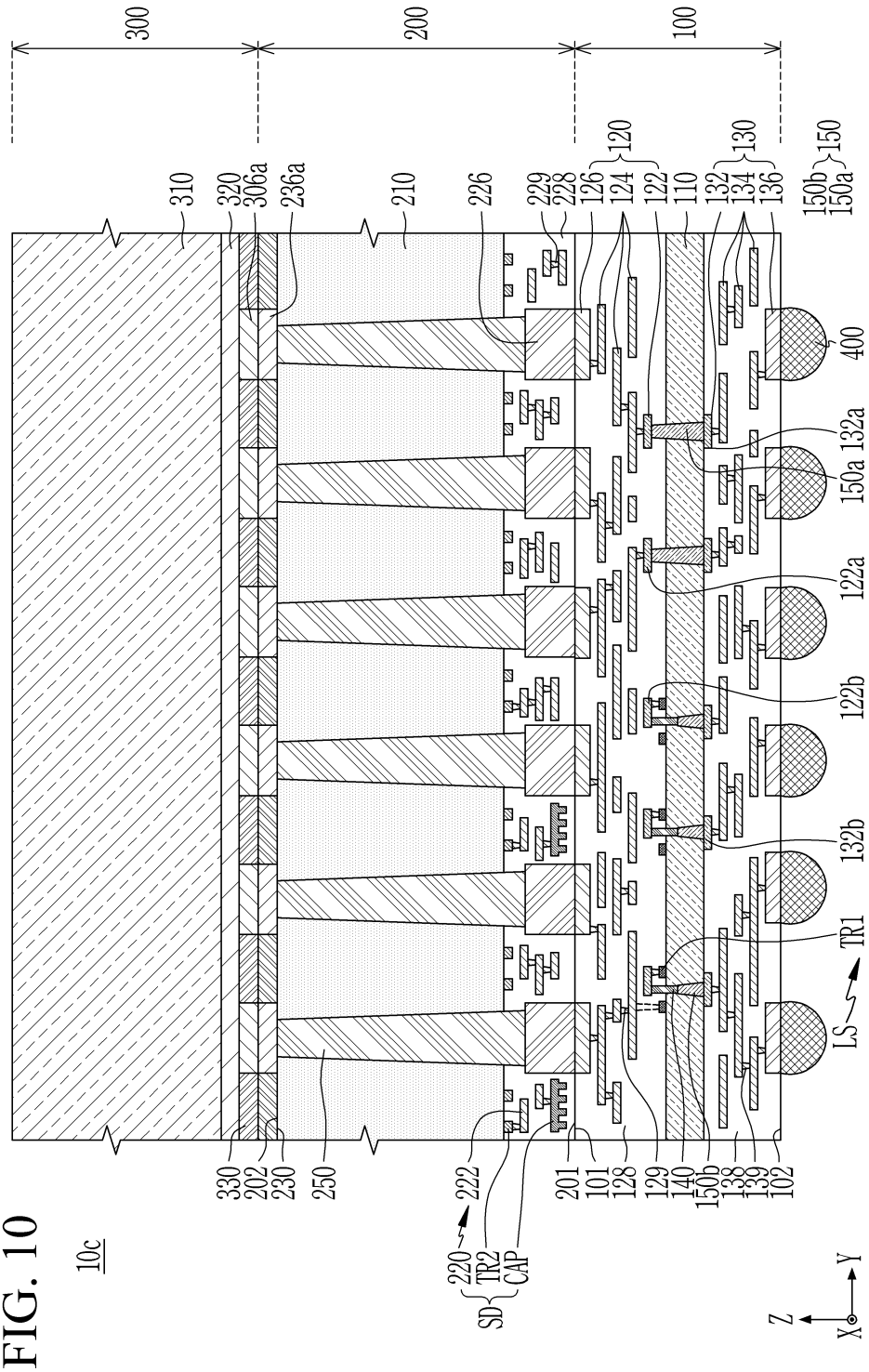

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FIG. 11

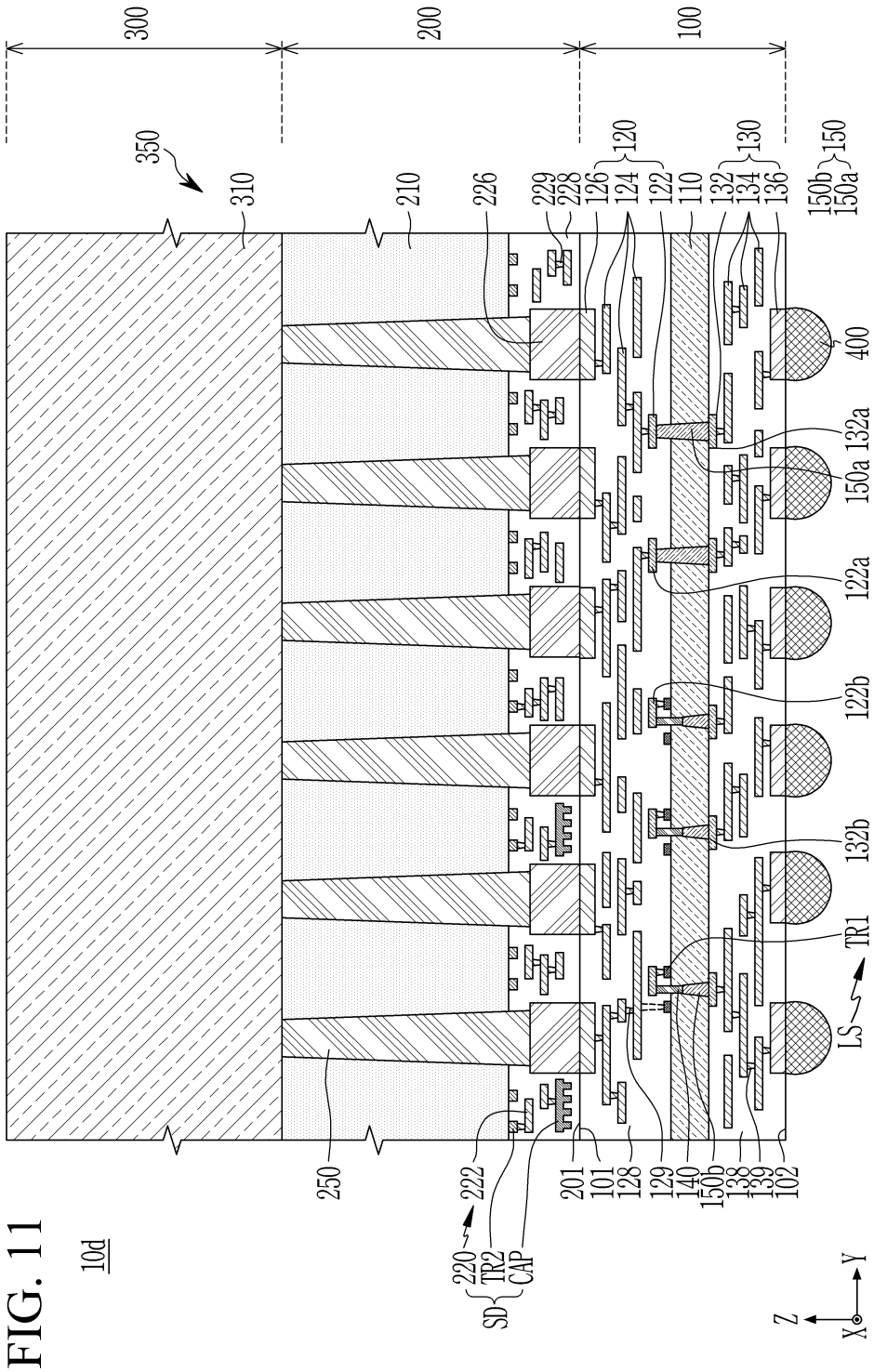
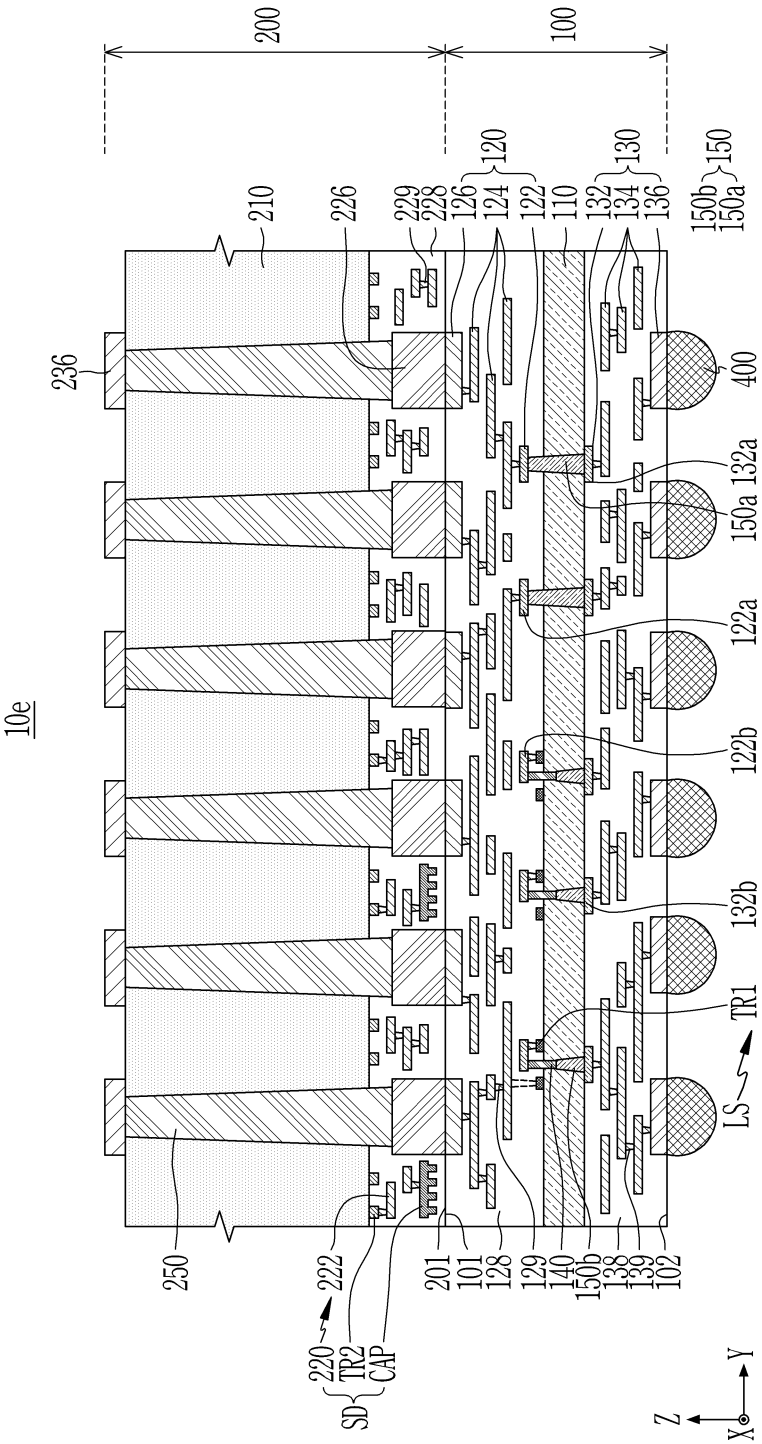

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FIG. 12


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