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(71) Applicant (for all designated States except US): **MI-CRON TECHNOLOGY, INC.** [US/US]; 8000 South Federal Way, Boise, ID 83716-9632 (US).

(72) Inventor; and

(75) Inventor/Applicant (for US only): **LABERGE, Paul, A.** [US/US]; 5772 Ridge Creek Road Court, Shoreview, MN 55126 (US).

(74) Agents: **ENG, Kimton, N.** et al.; Dorsey & Whitney LLP, 1420 Fifth Avenue, Suite 3400, Seattle, WA 98101 (US).

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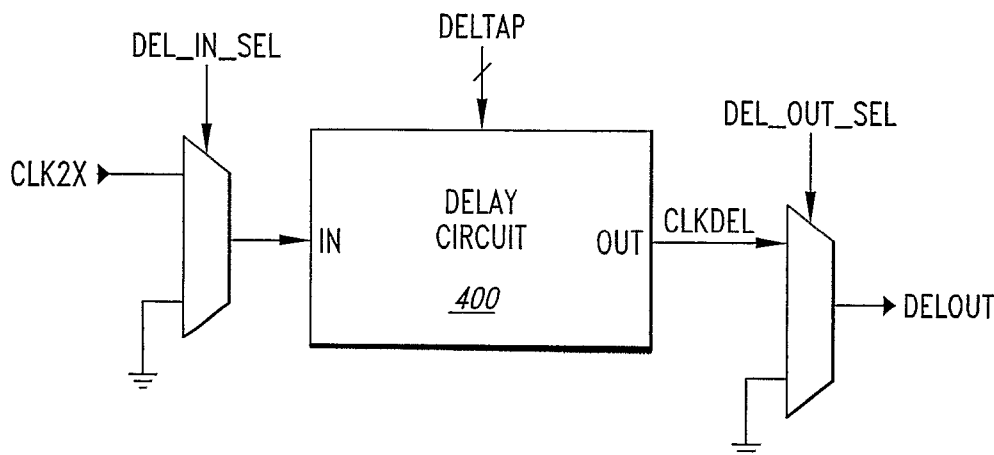
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(54) Title: DELAY LINE SYNCHRONIZER APPARATUS AND METHOD



(57) Abstract: A synchronizer system and method that can be used with a conventional adjustable delay circuit to preserve a pseudo-synchronous phase relationship between clock signals of different clock domains when the time delay of the adjustable delay circuit from which one of the clock signals is output is changed.

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