CLAIMS

1. A preparation method for a semiconductor structure, comprising:

providing a structure to be processed, wherein the structure to be processed comprises a substrate, and an etching target layer, a bottom mask layer and a first mask layer stacked on the substrate;

patterning the first mask layer to form a first pattern, the first pattern exposing parts of the bottom mask layer;

forming spacers with vertical sidewall morphology on sidewalls of the first mask layer;

removing the first mask layer;

filling a gap between the spacers with a filling layer,

wherein an etching selectivity ratio of a material of the spacers to a material of the filling layer is greater than or equal to 100;

removing the spacers;

forming a second mask layer on the filling layer;

etching the second mask layer to form a second pattern, the second pattern exposing parts of the filling layer; and

patterning the filling layer with the second mask layer as a mask to form a filling layer mask.

2. The preparation method according to claim 1, wherein, after forming the filling layer mask, the method further comprises:

patterning the bottom mask layer with the filling layer mask as a mask to form a third pattern, the third pattern exposing parts of the etching target layer; and

patterning the etching target layer with the bottom mask layer as a mask.

3. The preparation method according to claim 1, wherein, the material of the spacers has a Young's modulus greater than or equal to 25GPa.

4. The preparation method according to claim 1, wherein, the material of the filling layers comprises oxide.

5. The preparation method according to claim 1, wherein, the material of the spacers comprises polysilicon, silicon nitride or metal oxide.

6. The preparation method according to claim 1, wherein, forming spacers with vertical sidewall morphology on sidewalls of the first mask layer comprises:

forming a spacer layer covering the first mask layer and a surface of the bottom mask layer; and

removing the spacer layer covering a top of the first mask layer and the spacer layer covering the surface of the bottom mask layer, and retaining the spacer layer on the sidewalls of the first mask layer to form the spacers with vertical sidewall morphology.

7. The preparation method according to claim 1, wherein, removing the spacers comprises:

removing the spacers by an etching process with gas, wherein the gas comprises chlorine and hydrogen bromide.

8. The preparation method according to claim 1, wherein, removing the first mask layer comprises:

removing the first mask layer by an ashing process.

9. The preparation method according to claim 1, wherein, patterning the first mask layer comprises:

depositing a third mask layer on the first mask layer;

patterning the third mask layer and the first mask layer; and

removing the third mask layer and retaining the first mask layer.

10. The preparation method according to claim 9, wherein, patterning the third mask layer and the first mask layer comprises:

forming a photoresist layer on the third mask layer;

patterning the photoresist layer to form a first patterned photoresist layer, the first patterned photoresist layer exposing the third mask layer; and

etching the third mask layer and the first mask layer with the first patterned photoresist layer as a mask.

11. The preparation method according to claim 1, wherein, filling the gap between the spacers with the filling layer comprises:

forming the filling layer on the bottom mask layer, the filling layer filling the gap between two adjacent ones of the spacers and covering the spacers; and

planarizing the filling layer such that an upper surface of the filling layer is flush with upper surfaces of the spacers.

12. The preparation method according to claim 1, wherein,

the bottom mask layer comprises a first bottom mask layer and a second bottom mask

layer, and the second bottom mask layer is located on the first bottom mask layer.

13. A semiconductor structure prepared by the preparation method for a semiconductor structure according to anyone of claims 1 to 12.