

THREE-DIMENSIONAL CIRCUIT MODULES

Field of the Invention

This invention relates to electronic-circuit assemblies and more particularly to electronic-circuit modules that can be assembled in three-dimensional configurations.

Background of the Invention

Printed circuit boards are widely used for mounting and interconnecting components in circuit assemblies. Such circuit boards are fabricated in many varieties, including single-sided boards, double-sided boards and multi-layer boards, and with conductors and connecting arrangements compatible with the number and spacing of terminals on the most complex electronic devices, such as integrated circuits embodying microprocessors, memory, digital controllers and the like.

To conserve space, it is often desirable to arrange printed circuit boards in a three-dimensional structure. This can be accomplished by plugging circuit boards into connectors mounted in a backplane, mounting circuit boards perpendicular or parallel to other boards and various other arrangements.

Mounting circuit boards parallel to each other can be a particularly effective way of achieving a three-dimensional structure, provided that the necessary connections can be made between adjacent boards. Various means are available for making such connections, for example, the interconnecting spacers described in the article entitled "A 3-D System for Interconnection Meets the Challenge of High Density Packaging" beginning on page 84 of the April, 1985 issue of Electronic Packaging and Production, stacking connectors made by suppliers such as Teledyne Kinetics, Solana Beach, California and Cinch, Chicago, Illinois and elastomeric connectors made by suppliers such as PCK Elastomerics, Inc., Hatboro, Pennsylvania and AT&T, Richmond, Virginia. Both the stacking connectors and the elastomeric connectors have the advantage that they can be positioned to connect areas anywhere on the circuit boards being connected and do not have to be located at the edges of the boards.

Once a decision has been made to use parallel circuit boards with interconnecting means between the boards, the connections on the boards must be configured so that the necessary circuits can be routed from the connecting areas to the proper destinations on the various boards. It is sometimes the case that some circuits can be "bussed" (connected in multiple) to adjacent boards, while others must be routed individually to specific boards. For example, in a semiconductor memory having individual memory chips arranged on parallel circuit boards,

address, data and power circuits can be bussed to all the boards, but read and write circuits must be routed separately to each board. The kinds of connectors described above are all suitable for bussed connections as well as individually routed circuits, for example, as described in the final paragraph of the article referred to above.

5 It is desirable to minimize the number of different circuit board designs necessary when configuring a system using circuit boards stacked parallel to each other and even more desirable to be able to use the same design for each board in a stack. However, if it is necessary to route individual circuits to specific boards, as in the semiconductor memory described above, some arrangement must be devised by
10 which such circuits can be routed from a source to a destination using identical boards. The invention to be described provides a solution to this problem.

Summary of the Invention

This invention provides an arrangement by which individual circuits can be routed to destinations in a parallel stack of identical circuit modules or boards.
15 This is accomplished by providing staggered terminals on the circuit boards whereby an individual circuit connected to such a terminal on one side of the board is shifted to a different position on the other side of the board. The invention further provides arrangements whereby such circuit modules or boards can be stacked on one or both sides of a "mother" board to which such individual circuits are all routed. These and
20 other aspects of the invention will become apparent from consideration of the drawings and the following description.

Brief Description of the Drawing

Fig. 1 is a diagrammatic representation of an exemplary circuit module having circuit connections configured in accordance with the invention.

25 Fig. 2 is a diagrammatic representation of a mother board configured in accordance with the invention on which the modules shown in Fig. 1 can be mounted.

Figs. 3 and 4 are partial sections of through and staggered terminals used in the module of Fig. 1 and the mother board of Fig. 2.

30 Fig. 5 is a perspective view of the modules of Fig. 1 stacked on both sides of the mother board of Fig. 2.

Fig. 6 is a schematic side view of the stack shown in Fig. 5 to more clearly show the paths of one set of individual circuits.

For illustrative purposes, the invention will be described in terms of a
35 series of circuit modules for a simple semiconductor memory, for which the invention is particularly useful. However, as will become apparent, the invention is

not limited to such an application and can be used in modular design of any type of circuit requiring individual circuits to be routed to identical modules.

Fig. 1 shows a semiconductor memory module 10 configured in accordance with the invention. Memory chip 11 is mounted on circuit board 12 with terminals on chip 11, such as terminal 13, connected to conductors, such as conductor 14, on board 12 in the conventional manner. For clarity, a much simplified module is shown with a single memory chip having only four address leads, four data leads, two power leads, a read lead and a write lead. Such simplified module is adequate to describe the invention. However, it will become clear that the invention can be used advantageously with modules having many more connections, with more than one chip per module, chips on both sides of the module and many other module configurations.

Leads that are to be connected in a bus configuration to corresponding leads in other modules, such as the address, data and power leads from chip 11, are connected to terminals such as 15 on board 12 that provide connecting areas at the same location on opposite sides of the board. Such terminals are referred to herein as through terminals. Fig. 3 is a sectional view showing through terminals 15 in more detail.

Leads that are to be connected independently, such as the read and write leads from chip 11, are connected to terminals such as 16 on board 12 that provide connecting areas at different locations on opposite sides of the board. Such terminals are referred to herein as staggered terminals. Fig. 4 is a sectional view showing staggered terminals 16, and a typical arrangement of such terminals.

Fig. 2 shows a mother board 20 on which modules of the type shown in Fig 1 can be mounted. A memory chip 21 can also be mounted on mother board 20, and the various leads from chip 21 are connected to through terminals such as 25 and staggered terminals such as 26 in exact correspondence to the equivalent connections on module 10 shown in Fig. 1. However, mother board 20 has additional conductors 22, which connect the bussed address, data and power leads to appropriate circuitry and power sources (not shown), and additional leads 23, which connect the individual read and write leads for memory chip 21 mounted on the mother board and, as will be seen, for memory chips 11 mounted on modules 12, to appropriate circuitry (not shown).

Mounting holes such as 17 on module 10 and 27 on mother board 20 are used for mounting modules 10 in a stack on mother board 20.

A typical memory arrangement might call for the various selection, driving and register circuits for the memory to also be located on mother board 20. Alternatively, such circuits could be placed elsewhere and connected to leads 22 and 23 on mother board 20 through additional connectors. Such arrangements are
5 familiar to those skilled in the art.

As can be seen from Fig. 3, through terminals 30 (15 in Fig. 1 and 25 in Fig. 2) have connecting areas 30a and 30b at the same location on opposite sides of circuit board 31. However, as shown in Fig. 4, staggered terminals 16 have connecting areas 16a and 16b at different locations on opposite sides of circuit board
10 31. In Fig. 4, staggered terminals 40 (16 in Fig. 1 and 26 in Fig. 2) are arranged so that the connecting area 40a of one terminal is opposite the connecting area 40b of an adjacent terminal. As will be seen, when modules having such staggered terminals are stacked, circuits routed through such terminals are shifted one position at each layer in the stack. However, other arrangements for interconnecting the
15 opposing connecting surfaces are useful, as will also be seen.

Fig. 5 is a perspective view of a stack comprising identical modules 10-1, 10-2, and 10-3 mounted on mother board 20, with connectors 50 serving both as spacers and as means for interconnecting opposing connecting areas on the modules and mother board. Such connectors can be the stacking connectors or elastomeric
20 connectors described above, or other suitable connectors. Note that modules 10-1 and 10-2 are mounted on one side of mother board 20 and module 10-3 is mounted on the other. As will become apparent, the modules can be mounted on whichever side of the mother board is most convenient; all can be on one side or all on the other if desired. Bolts such as 51 hold the stack together. Bolts 51 can also serve to feed
25 power from mother board 20 to modules 10, as an alternative to terminals such as 15, and as heat sinks to aid in dissipating heat generated by modules 10 and mother board 20. For these purposes, holes 17 and 27 would be fabricated as plated-through holes with appropriate electrical connection to the circuitry on modules 10 and mother board 20, respectively, and such holes would be sized for proper electrical
30 and thermal connection to bolts 51.

It will now be useful to describe the staggered terminals and their interconnections on modules 10 and mother board 20 in more detail. Referring back to Fig. 1, staggered terminal 16a is connected to the "read" terminal of chip 11 and has a back connecting area lined up with the front connecting area of staggered
35 terminal 16b. Correspondingly, the back connecting area of staggered terminal 16b lines up with the front connecting area of staggered terminal 16c and the back

connecting area of staggered terminal 16c lines up with the front connecting area of staggered terminal 16d. Finally, the back connecting area of staggered terminal 16d lines up with the front connecting area of staggered terminal 16a by means of an extended connection represented by dotted line 18. The connections associated with the "write" terminal of chip 11 are similar. This particular configuration of staggered terminals is arranged for a maximum of four layers in a stack (a mother board 20 plus three modules 10). As can be seen, the number of staggered terminals needed for a given circuit is equivalent to the number of layers in the stack. However, it is not necessary for all the possible layers in a stack to be present.

Referring now to Fig. 2, terminals 26a, 26b, 26c and 26d on mother board 20 are arranged similarly to terminals 16a, 16b, 16c and 16d on module 10 as just described, with additional leads 23 connecting such terminals to the appropriate circuits (not shown) for driving the "read" terminals of the various memory chips.

Because lead 28 for the "read" circuit for chip 21 on mother board 20 terminates on mother board 20 itself, there is no need to extend it to any of modules 10 in the stack. Thus, the connecting areas of staggered terminal 26a could be disconnected. However, if it is desired to mount all the memory chips on modules 10 and not have memory chip 21 on mother board 20, then lead 28 must be connected to the connecting areas of staggered terminal 26a as shown.

Referring now to Fig. 6, the various interconnections associated with the staggered terminals and the intervening connectors in the stack are shown diagrammatically as an aid in understanding the relationships involved. Four leads A, B, C and D are shown passing through the stack, which would connect respectively to leads 28a, 28b, 28c and 28d on mother board 20 as shown in Fig. 2.

Given that such modules and mother board are arranged as shown in Figs. 1 and 2, it can be seen that lead A connects to chip 21 on mother board 20, lead B connects to chip 11 on module 10-1, lead C connects to chip 11 on module 10-2 and lead D connects to chip 11 on module 10-3. If the stack were rearranged with module 10-3 placed on top of the stack, it can also be seen that lead D would still connect to chip 11 on such module.

In the example given above, three of the staggered terminals shift three of leads A, B, C and D one position in each layer of the stack and the fourth staggered terminal shifts the fourth lead back to the first position. Many other arrangements of staggered terminals are possible. For example, if it is desired to arrange leads in pairs, the staggered terminals can be arranged to shift all but one pair of leads two positions in each layer of the stack and the remaining pair back to

the first position.

It is understood that the embodiments described herein are only illustrative and that other arrangements may be devised without departing from the spirit and scope of the invention.



Claims:

1. A three-dimensional circuit structure comprising a plurality of circuit modules mounted in a stack and means for connecting terminals in adjacent circuit modules, each circuit module being a substantially planar circuit board having conductors, utilizing means and a plurality of said terminals thereon,

5 CHARACTERIZED IN THAT

each terminal comprises a first connecting area on one side of the circuit module connected to a second connecting area on the other side of the circuit module, at least some of the terminals are staggered terminals having the first connecting area opposite the second connecting area of a different staggered terminal and at least one of the staggered terminals on each module is connected by one of the
10 conductors to the utilizing means and

said connecting means connects opposing ones of the first and second connecting areas on adjacent circuit modules in the stack when said connecting means is placed between said adjacent modules.

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2. The circuit structure of Claim 1
FURTHER CHARACTERIZED IN THAT

at least one of the terminals on each circuit module is a through terminal having its first connecting area opposite the second connecting area of the same through terminal and at least one of the through terminals on each module is
20 connected by one of the conductors to the utilizing means.

3. The circuit structure of claim 2
FURTHER CHARACTERIZED IN THAT

the utilizing means is a semiconductor memory and at least one of the circuit modules has means for connecting at least one of the staggered terminals and/or the through terminals to means for reading, writing and powering semiconductor memories.

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4. A circuit module for use in a stack of similar modules in conjunction with connecting means placed between the modules in said stack, which comprises a substantially planar circuit board having conductors, utilizing means and a plurality of terminals thereon
CHARACTERIZED IN THAT

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each terminal comprises a first connecting area on one side of the circuit module connected to a second connecting area on the other side of the circuit module, at least some of the terminals are staggered terminals having the first connecting area opposite the second connecting area of a different staggered terminal and at least one of the staggered terminals on each module is connected by one of the conductors to the utilizing means, whereby the first connecting areas on one of the circuit modules will be connected to opposing second connecting areas on an adjacent circuit module when assembled with the connecting means in the stack.

10 **5. The circuit module of Claim 4
FURTHER CHARACTERIZED IN THAT**

at least one of the terminals is a through terminal having its first connecting area opposite the second connecting area of the same through terminal and at least one of the through terminals is connected by one of the conductors to the utilizing means.

15 **6. The circuit module of claim 5
FURTHER CHARACTERIZED IN THAT**
the utilizing means comprises a semiconductor memory.

20 **7. The circuit module of claim 6
FURTHER CHARACTERIZED IN THAT**
said circuit module also includes means for connecting at least one of the staggered terminals and/or the through terminals to means for reading, writing and powering semiconductor memories.

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