Claims

What is claimed:

1. A semiconductor device, comprising:

a semiconductor die including an active surface and a contact pad formed on the active surface;

an encapsulant deposited over the semiconductor die, wherein a surface of the encapsulant is coplanar with the active surface of the semiconductor die;

a masking layer formed in contact with a first portion of the active surface of the semiconductor die while leaving a second portion of the active surface including the contact pad devoid of the masking layer; and

a build-up interconnect structure formed in contact with the second portion of the active surface, wherein the build-up interconnect structure includes a conductive layer and an insulating layer formed over the conductive layer and terminates in a lateral direction across the semiconductor die at an edge of the masking layer with no portion of the build-up interconnect structure over the first portion of the active surface of the semiconductor die, and the insulating layer contacts the encapsulant.

2. The semiconductor device of claim 1, further including a second interconnect structure disposed over the build-up interconnect structure.

3. The semiconductor device of claim 2, wherein the second interconnect structure includes a bump.

4. The semiconductor device of claim 1, further including a conductive via formed through the semiconductor die.

5. The semiconductor device of claim 1, further including further including a conductive via formed through the encapsulant.

6. The semiconductor device of claim 1, further including a heat sink disposed over the semiconductor die.

7. A semiconductor device, comprising:

a semiconductor die including an active surface;

an encapsulant deposited over the semiconductor die;

a masking layer formed over a first portion of the active surface of the semiconductor die while leaving a second portion of the active surface devoid of the masking layer; and

a build-up interconnect structure formed over the second portion of the active surface, wherein the build-up interconnect structure includes a conductive layer and an insulating layer formed over the conductive layer and terminates at an edge of the masking layer with no portion of the build-up interconnect structure over the first portion of the active surface of the semiconductor die.

8. The semiconductor device of claim 7, further including a second interconnect structure disposed over the build-up interconnect structure.

9. The semiconductor device of claim 8, wherein the second interconnect structure includes a bump.

10. The semiconductor device of claim 7, further including a second interconnect structure disposed between the semiconductor die and build-up interconnect structure.

11. The semiconductor device of claim 7, further including a conductive via formed through the semiconductor die.

12. The semiconductor device of claim 7, further including a conductive via formed through the encapsulant.

13. The semiconductor device of claim 7, further including a heat sink disposed over the semiconductor die.

14. The semiconductor device of claim 7, wherein a surface of the encapsulant is coplanar with the active surface of the semiconductor die.

15. A semiconductor device, comprising:

a first semiconductor die including an active surface;

an encapsulant deposited over the semiconductor die;

a masking barrier formed over a first portion of the active surface of the semiconductor die; and

a build-up interconnect structure formed over a second portion of the active surface of the semiconductor die, wherein the build-up interconnect structure includes a conductive layer and an insulating layer formed over the conductive layer and terminates at an edge of the masking barrier with no portion of the build-up interconnect structure over the first portion of the active surface of the semiconductor die.

16. The semiconductor device of claim 15, further including a second interconnect structure disposed over the build-up interconnect structure.

17. The semiconductor device of claim 16, wherein the second interconnect structure includes a bump.

18. The semiconductor device of claim 15, further including a second interconnect structure disposed between the semiconductor die and build-up interconnect structure.

19. The semiconductor device of claim 15, further including a conductive via formed through the semiconductor die.

20. The semiconductor device of claim 15, wherein the masking barrier includes a dam wall.

21. The semiconductor device of claim 15, wherein the masking barrier includes a masking layer.

22. The semiconductor device of claim 15, further including a heat sink disposed over the semiconductor die.

23. The semiconductor device of claim 15, wherein a surface of the encapsulant is coplanar with the active surface of the semiconductor die.

24. The semiconductor device of claim 7, wherein the insulating layer of the build-up interconnect structure contacts the encapsulant.